SPAD array sensitivity improvement by diffractive microlens

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***Abstract*—In this paper we present sensitivity improvement of SPAD pixel using diffractive microlens. We designed microlens structures based on rigorous optical simulations, then we developed the process for thick optical spacer and thin amorphous silicon deposition, on which diffractive structures were defined by lithography and etching. These microlenses have been implemented two SPAD designs available on STMicroelectronics 40nm CMOS testchips (32×32 SPAD array). Circuits were characterized and we demonstrated, depending on SPAD design, high optical gain at 850*nm* (×2.7 to ×5.3) and significant gain at 940*nm* (×1.6 to ×2.4).**

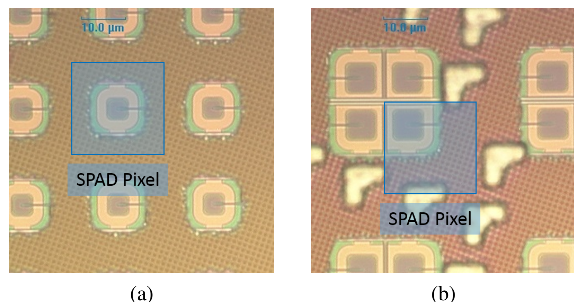
I. Introduction

Single Photon Avalanche Diode (SPAD) arrays are promising image sensors for applications requiring photon arrival timestamp with accuracy around hundreds of picoseconds or even less. From an optical point of view, the main limitation of SPAD pixels is their low optical fill-factor (ff_o), about 10% or below. This can be partially overcome by placing light concentrator in front of each pixel. External microlenses, either refractive or diffractive, have first been implemented [1] with limitation of alignment accuracy between microlens and SPAD arrays. More recently on-chip refractive microlens arrays, fabricated at wafer level with conventionnal reflow process, were demonstrated with success[2].

In this work, we present the development of wafer level diffractive microlens on top of SPAD for applications in near-infrared (between 850nm and 950nm). In the following, we detail the SPAD designs and the optical simulations performed to optimize the diffractive structures. Then, the specific process we developed is presented before summarizing electro-optical characterization results obtained on test-chips.

II. SPAD designs

In our work we considered two SPAD layouts, both on Front-Side Illumination (FSI) STMicroelectronics 40nm CMOS technology[3]. For each design, the pixel has a pitch of $21.6\mu m$ and is implemented in a 32×32 array. The first one has a conventional layout: diode with rounded square shape and metal shielding (see Fig. 1a).



(a) (b)

Fig. 1. Layout of SPAD pixels: (a) periodic design with fill-factor of 5%, (b) grouped design with fill-factor of 12%.

The optical fill-factor $ff_o = 5\%$ is defined by the size of the metal window $4.7 \times 4.7\mu m^2$. In the second design, the N-well of diodes are shared between 2×2 SPAD, improving the fill-factor $ff_o = 12\%$ with a size of metal window of $7.5 \times 7.5\mu m^2$, see Fig. 1b.

III. Optical simulations

To concentrate light onto SPAD photodiode, we considered Fresnel Zone Plate[4, 5] structures (FZP). It consists of rings diffracting the light to produce constructive interference at the focal point and size of rings are calculated using Fresnel zone concept[6, 7]. In order to take profit of all incident light, a phase shift of $(2k + 1) \times \lambda/2$ (with $k \in \mathbb{N}$) must be introduced by the material of the rings, so light diffracted in-between rings and by rings adds constructively at the lens focus.

We chose amorphous silicon (a:Si) for the rings as it presents advantageous properties: it is compatible with CMOS process, has very low absorption in the spectrum of interest and thanks to its high refractive index (see Fig. 2), the phase shift can be introduced while keeping the layer thickness low, further reducing the absorption and making the patterning easier. As the pitch of the SPAD is quite large ($21.6\mu m$) compared to the back-end of line (BEOL) thickness ($6.1\mu m$), we introduced an optical spacer between the FZP and the wafer. This pedestal has to be transparent and with a low refractive index, thus silicon oxide is an appropriate material.

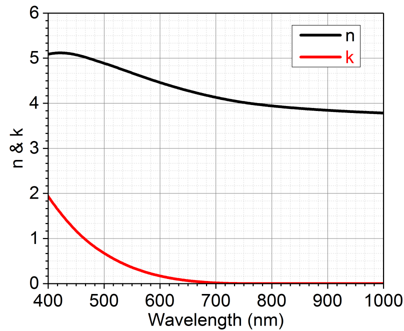


Fig. 2. Refractive and extinction indices of amorphous silicon.

The objective of the optical simulations is to identify the parameters that define the FZP structures to be implemented on mask. Few parameters are required: the thickness of the optical spacer, the thickness of the a:Si layer and the effective focal length of the FZP, considering light propagates in silicon oxide before reaching the silicon. Thus, we performed 3D rigorous electro-magnetic simulations[8] with FDTD-Solutions software[9] which include the model of the SPAD, based on its layout and CMOS 40nm technology description (see Fig. 3). The model is illuminated by plane waves

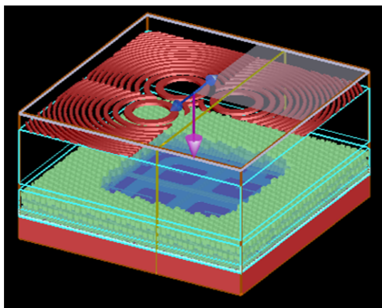


Fig. 3. 3D model of 2×2 SPAD pixel (see Fig. 1b): silicon in red at the bottom, metal lines in blue and green and FZP structures in red on the top of the model.

and the electric field inside the structure is recorded as shown in Fig. 4. Our figure of merit is the amount of light absorbed in the volume defined by the photodiode N-well. In order to limit the process trials, after a first optimization, we fixed the thickness of the silicon oxide pedestal to $10\mu m$. Then we finely optimized the two remaining parameters (a:Si layer thickness and FZP focal length). Nevertheless, as the simulation time is very long for such pixels, we strongly limited the number of simulation runs by using metamodelization framework or Surrogate Based Design Optimization (SBDO) developed at CEA-LETI[10]. With only few tens of

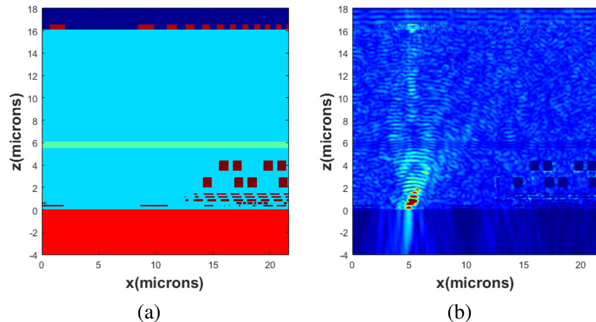


Fig. 4. Vertical cross-sections of model presented in Fig. 3: (a) refractive index of the structure and (b) simultated electrical field.

simulations, the optimum was found. For instance, for the 2×2 SPAD, results are shown in Fig. 5. In this case, optimum is reached for $f_{effective} = 15.5\mu m$ and a a:Si thickness of $465nm$, introducting a $3\lambda/2$ phase shift when light passes through the rings.

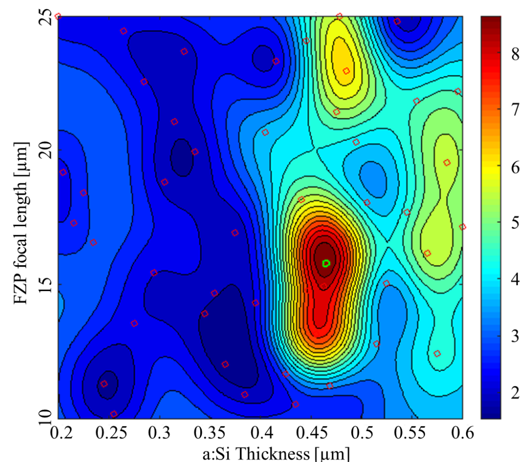


Fig. 5. Results of SBDO for 2×2 SPAD pixel as a function of a:Si thickness and FZP effective focal length. The point highlighted in green is the estimated optimum.

In addition to this simulated optimal design, we tested several FZP designs by increasing the effective focal length and using as nominal wavelength the standard laser diode emission wavelength ($850nm$, $905nm$ and $940nm$) (see tables I and II for all combinations).

IV. Process development

The two main components required for the realization of the diffractive structures are the optical spacer and the amorphous silicon structures. The first one is made by thick oxide deposition and need to fulfill several constrains: a thickness of $10\mu m$, a low refractive index (around 1.5), a low temperature deposition for back-end compatibility (below $400°C$) and low mechanical

stress to ensure a minimum bow on the wafer for the lithography done afterward (maximum allowed bow is $100\mu m$). Thus, we developed a SiO_2 PECVD deposition at $350°C$, giving a layer with a refractive index of $1.52@633nm$ and a maximum bow on $300mm$ wafer below $10\mu m$.

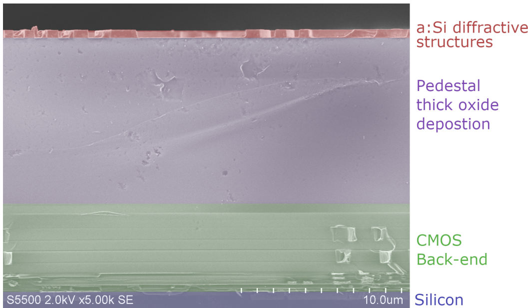
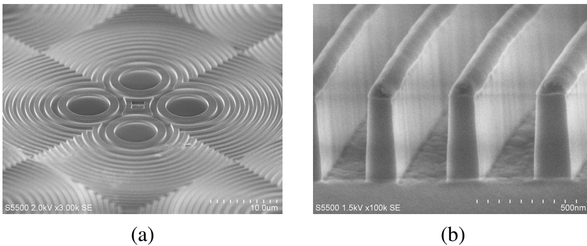


Fig. 6. Vertical cross-section of optical spacer and a:Si microlens processed on CMOS wafer

The a:Si layer shares the same constraints in terms of process compatibility: a low temperature deposition and a low mechanical stress. In addition, we were specially careful to the absorption coefficient in the spectral range of interest ($\lambda \geq 800nm$). By tuning the RF power, precursor flux and pressure of our PECVD tool, we were able to deposit a a:Si layer with a thickness of $465nm$ while keeping the bow on the wafer below $80\mu m$, compatible with the lithography scanner.

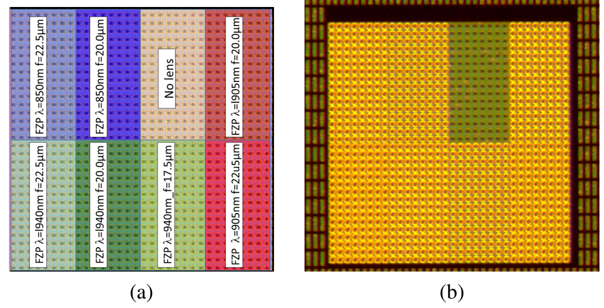


(a) (b)

Fig. 7. (a) Tilted SEM view of FZP structures implemented on 2×2 SPAD, (b) SEM view of pattern with CD $= 100nm$ after etching.

The lithography was made on a Deep-UV scanner with an Optical Proximity Correction of the mask set to ensure the critical dimensions of CD=$100nm$ and space=$100nm$ (see Fig. 7b). Etching and stripping were developed to minimize the slope of the a:Si pattern and suppress the under-etch of underlying oxide.

In order to implement few design variants of FZP on the 32×32 SPAD arrays while ensuring statistically representative sampling, we split the image into 8 areas of 8×16 SPADs. One of them was kept free from microlens and serves as reference for measurement, avoiding intra and inter wafer variations (see Fig. 8).



(a) (b)

Fig. 8. Implementation of diffractive microlenses on 32×32 circuit, (a) view of layout, (b) optical microscope.

V. Electro-optical characterization results

Devices were characterized using in-house characterization capabilities. For few dice we measured the spectral response, or photon detection efficiency, with spectrally and spacially controlled diffuse light ($\Delta\lambda = 10nm$ and $f_{\#}$=2). For each die, mean value and standard deviation over the 8×16 SPADs area are computed and one example is reported on Fig. 9.

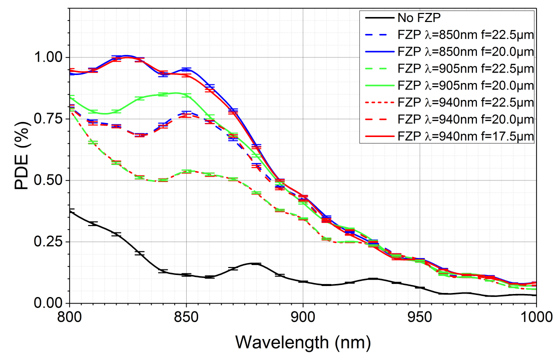


Fig. 9. Spectral photon detection efficiency for bare SPAD and for eight diffractive microlens variants, for centered SPAD design.

As the dispersion inside a die is low, and in order to measure a larger number of dice, we used a simplified procedure with only two illumination wavelengths ($850nm$ and $940nm$) corresponding to standard laser diodes. For each wavelength, we computed the optical gain provided by each diffractive microlens design. This gain is measured for several dice over the wafer. Mean value and standard deviation are reported on table I and table II. We achieved an optical gain of $\times 5.3$ at 850nm for centered SPAD design, and $\times 3.3$ at 850nm for off-centered SPAD design. This latter lower gain is mainly due to the $2.4\times$ higher optical fill factor ($ff_o = 12\%$ versus $ff_o = 5\%$) and the strong off-axis leading to more interaction between light and the metallic interconnections, thus reducing the light concentration capability of the lens.

TABLE I
OPTICAL GAIN OF DIFFRACTIVE MICROLENS ON CENTERED SPAD, MEASURED OVER 60 DICE.

FZP design		optical gain	
λ_{design}	$f_{effective}$	@$850nm$	@$940nm$
$850nm$	$20.0\mu m$	$\mathbf{5.3 \pm 0.6}$	2.4 ± 0.1
$850nm$	$22.0\mu m$	4.5 ± 0.6	2.3 ± 0.1
$905nm$	$20.0\mu m$	4.8 ± 0.5	2.3 ± 0.1
$905nm$	$22.0\mu m$	3.5 ± 0.4	2.1 ± 0.1
$940nm$	$17.5\mu m$	4.3 ± 0.6	2.4 ± 0.1
$940nm$	$20.0\mu m$	4.6 ± 0.6	$\mathbf{2.4 \pm 0.1}$
$940nm$	$22.5\mu m$	3.5 ± 0.6	2.1 ± 0.1

TABLE II
OPTICAL GAIN OF DIFFRACTIVE MICROLENS ON 2×2 SPAD, MEASURED OVER 20 DICE.

FZP design		optical gain	
λ_{design}	$f_{effective}$	@$850nm$	@$940nm$
$940nm$	$15.5\mu m$	$\mathbf{3.3 \pm 0.3}$	$\mathbf{1.7 \pm 0.1}$
$940nm$	$17.5\mu m$	3.1 ± 0.3	1.7 ± 0.1
$940nm$	$20.0\mu m$	2.8 ± 0.3	1.6 ± 0.1

VI. CONCLUSION

In this study, we have successfully demonstrated the capability to improve SPAD sensitivity using diffractive microlenses in the near infrared. Relying on Fresnel Zone Plate structures, we designed the microlenses based on optical simulations taking into consideration the SPAD layout and CMOS technology. Specific process was developed for the optical spacer, made with thick oxide deposition, and for the microlenses, made by patterning of amorphous silicon layer. These microlenses were implemented on STMicroelectronics 40nm CMOS testchips. We measured a sensitivity improvement up to a factor $\times 5.3$ at $850nm$ for SPAD having a pitch of $21.6\mu m$ and bare fill-factor of 5%. Even though this is a first implementation of FZP microlenses on SPAD, results are very encouraging and to the best of our knowledge this is the highest optical gain demonstrated with diffractive microlens on SPAD, comparable or exceeding results obtain with refractive microlens. In addition, this technology offers several advantages like planar and inorganic microlens or the capability to design off-axis microlens.

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