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A high dynamic range, 1.9 Mpixel CMOS image sensor for X-ray imaging with in-pixel charge binning and column parallel ADC

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***Abstract*—**CMOS image sensors (CIS) coupled to a scintillator or a phosphor screen are used for medical X-ray imaging. This paper presents a sensor specifically designed for the intraoral dental market. The sensor features 1.9 million pixels on a 18.5 µm pitch. The pixels are designed in a 2x2 group and each pixel has its own overflow capacitor. High dynamic range is achieved both for un-binned and 2x2 binned pixels. It has a noise of 75 e- rms and a full well of 4 million electrons, thus giving a sensor a high dynamic range in excess of 94.3 dB. The frame rate is up to 31 fps, thus allowing video recording. The sensor was manufactured in a 180 nm CIS process.

III. INTRODUCTION

DESIRED features for X-ray medical imaging are commonly:

- small pixels for good spatial resolution, typically down to about 20 µm for intraoral dental and around 50 µm for larger panels, e.g. mammography panels;
- high dynamic range HDR, with simultaneous low noise and high full well;
- pixel binning, ideally noiseless;
- a way of controlling when the X-ray beam is on in order to optimize exposure and minimize dose.

In order to simplify the ease of use of the sensor and its integration, as many functionalities as possible should be integrated in the sensor.

The sensor presented here includes all of the features above and others (Figure 1). The sensor features 1204x1612 pixels with a pitch of 18.5 µm. The floorplan of the sensor is shown in figure 1. The sensor can be operated with a global reset, while the readout is always rolling. Column-parallel ADCs are integrated in each column. The data from the ADC are passed in a parallel to shift-register which feed the data serialiser. Data are sent to LVDS outputs. There is a total of 5 LVDS I/O and the user can select to activate 1, 2 or 5 of them, for a corresponding speed of of 6.4, 10.7 and 31.4 frames per second (fps) respectively. This allows to trade-off speed with power consumption depending on the application. The sequencer which controls the functioning of the sensors is integrated on the chip so that the sensor runs only with a master clock and a reset signal. The default value of the master clock is 200 MHz. Bias currents and voltages are generated on chip by a programmable bias generator. The setting of this generator as well as of the timing and of other programmable features is controlled by a simple two-wire serial interface.

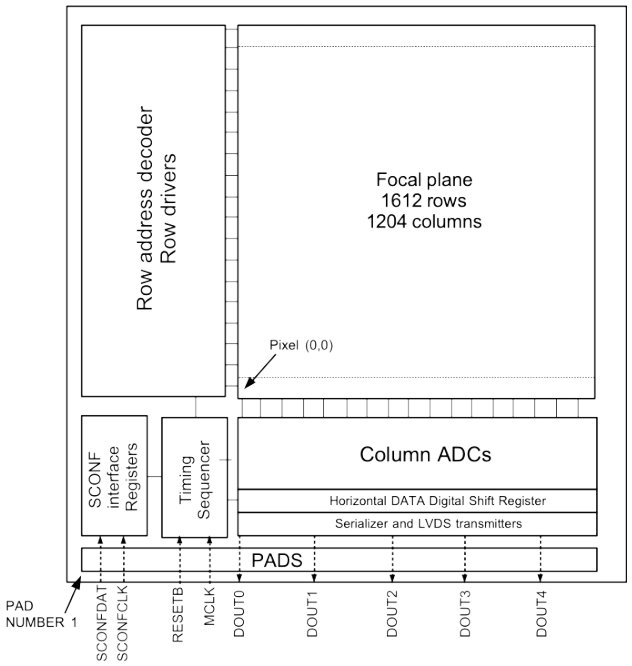

Figure 1. DENTIX architecture.

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IV. Pixel Architecture

The pixel pitch is 18.5 µm. The design goal was for the pixel to have high dynamic range and being able to perform 2x2 binning while preserving this feature. Pixels where arranged in groups of 2x2 with a shared reset transistor. The figure below shows the schematic of such a 2x2 group.

Each pixel has high dynamic range through a lateral overflow structure and binning is done in the charge domain, preserving the high dynamic range performance (Figure 2 and Figure 3). Note that the RST transistor is shared between the two pixels in the same row, effectively reducing the transistor count for increased fill factor. So, while the pixel alone would have 6 transistors, the 2x2 structure is equivalent to 6.5T instead of 7T. The BIN and RST transistors work together to perform reset and binning when required. The timing for the signal in the two different modes is shown in Figure 4 and Figure 5 Note that the BIN transistor is switched in normal mode as well as the RST transistor and the reset is performed through it and the RST transistor. In full resolution mode, when the pixel comes out of reset, BIN is OFF but RST is held at an intermediate potential so that the shared floating junction is allowed to overflow to the VRST potential, thus avoiding blooming of the pixel because of charge accumulating on this floating junction. In binning mode, RST is OFF during integration, but BIN is kept ON but not overdriven to avoid the risk of stress on the gates of these transistors during integration. The photodiode is partially pinned and has a low intrinsic capacitance. The desired noise and full well are achieved by adding extra in-pixel capacitance connected to the overflow transistor (capacitance C1 in Figure 2). (see table 1). As it is desirable to have higher sensitivity in HDR mode, a smaller capacitance C0 is tied to the PPPD. The LO signal controls the lateral overflow. In full frame mode, LOa/b signals are operated with the corresponding row, while in binned mode they are operated together.

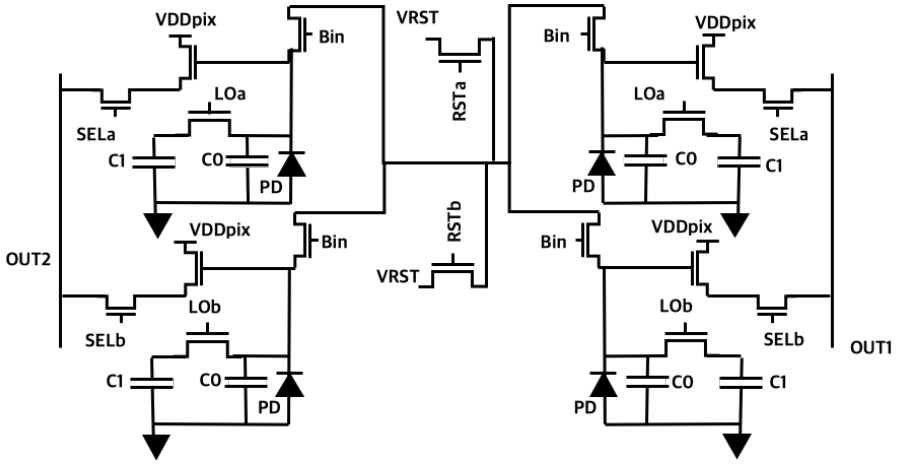

Figure 2. Schematic of a 2x2 group of pixels, showing the RST transistor, which is shared by the two pixels in the same row.

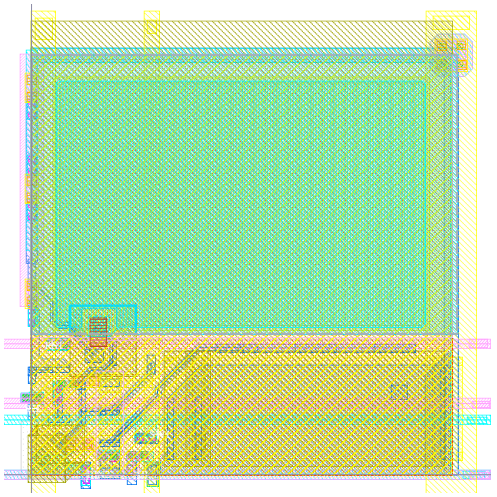

Figure 3, Pixel layout.

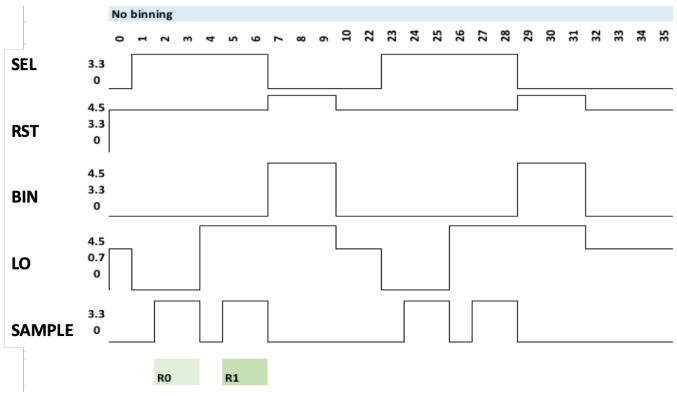

Figure 4. Timing of the pixel in normal mode, no binning. During integration, the gate of the RST transistor is biased with an intermediate voltage, to allow charge collected by the floating node between RST and BIN to discharge to VRST.

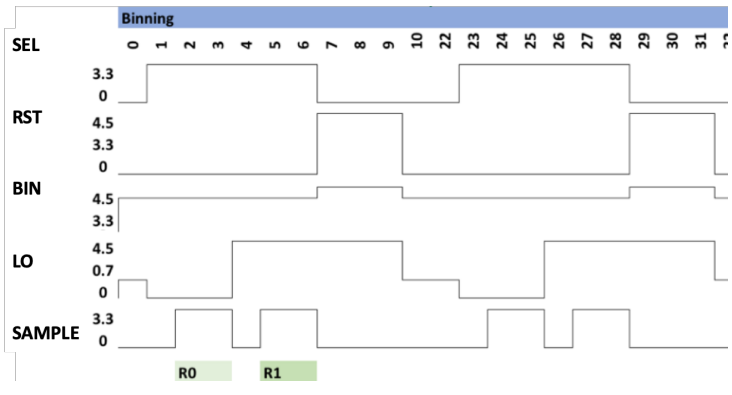

Figure 5. Timing of the pixel in binning mode. During integration, the gate of the BIN transistor is kept at an intermediate level, thus allowing the charge to be shared between nodes, without overdriving the transistor.. During readout BIN is fully ON.

III. Readout Architecture

For the readout, each pixel is read in both high gain (given by C0 when signals LOa/b are low) and low gain (given by C1 when signals Loa/b are high), and automatically the column circuitry selects one of them for optimal accuracy. The selected value is converted by column-parallel 2nd order incremental sigma-delta ADCs (Figure 6) [2] performing a 14-bit conversion in 8 µsec with an input clock of 25 MHz. The input clock is derived internally by dividing the 200 MHz master clock. The ADC data have an extra bit to avoid digital overflow of the decimator. The gain bit is stored in the ADC together with the 15-bit conversion data. The 16-bit data are stored into an internal register for readout while the ADC is reset and made ready for the next conversion.

A dedicated input allows the characterization of the ADC array in isolation from the focal plane pixels. Table 1 summarizes the measured performance of the converter.

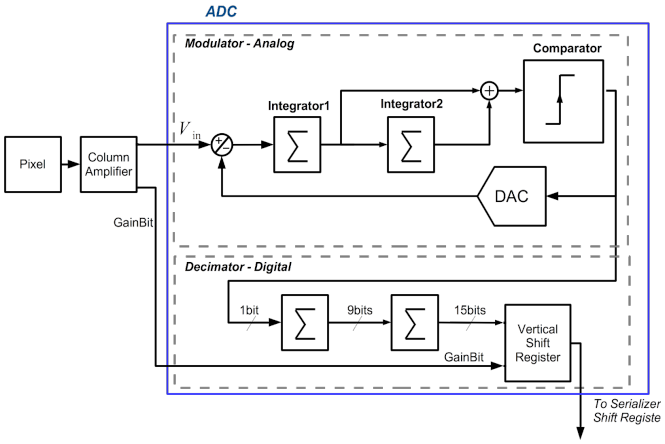

Figure 6. Schematic of the column-parallel ADC.

Table 1 ADC performance summary

Parameter	Value
Operating frequency	25 MHz
Cycles per 14-bits conversion	200
Conversion time (14 bits)	8 µsec
LSB	167.1 µV
Noise (including column amplifier)	130 µV

Each column generates a 16-bit data. These data are fed to a 16-bit serializer. The chip has 5 LVDS outputs and the user can select whether data are read through 1, or 2 or 5 of them, which correspond to frame rate of 6.4, 10.7 and 31.4 f frames per second. The LVDS outputs run at 200 MHz in single data rate. The data flow has an embedded clock synchronization pattern.

The timing is integrated on chip as well as the generation of bias. The setting of these parameters is done through a 2-pin serial-to-parallel interface with proprietary protocol. The entire chip is operated with only 7 pins, thus simplifying the interface with external electronics.

IV. Sensor characterization.

For the characterization, the photon transfer curve (PTC) method was used. In-house equipment was used to perform the measurement and integration sweeps were performed to extract the electro-optical parameters of the chip. Measured curves for the high and low gain are shown in Figures 7 and 8 respectively. In these curves, the measured points are in blue and the points used for the fit are in green with the fitted curve is shown in red. In order to select the region of the PTC where to perform the fit, the log-log plot of variance vs average was analysed and the region where the slope is equal to 0.5, signaling photon shot noise is dominating was selected. This same region was used to fit the PTC curves. In these tests, the sensor was operated with the default values, hence in high gain, the column circuitry switches to the log gain before the linear full well, i.e. the maximum of the variance in the PTC, is achieved. As the sensor features global reset, the integration time effectively varies from one line to another. Each point in the PTC curves represents the vergae values of one of these lines.

The cumulative dark current distribution measured at room temperature is shown in Figure 9. This number is low enough so that the sensor can be operated with global reset and rolling readout with no loss of performance.

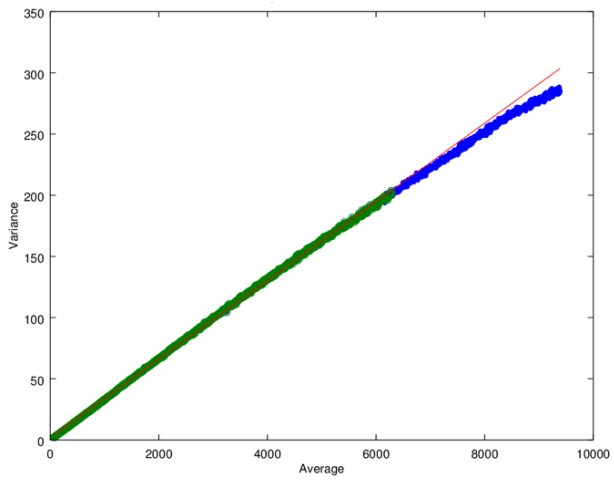

Figure 7. Photon transfer curve applied to the high gain section of the pixel. The default settings were used so that the range is limited by the HDR threshold. Blue: measured point; green: points over which a log-log ft gives a slope of 0.5; these points are used to extract the gain; red: fitted curve

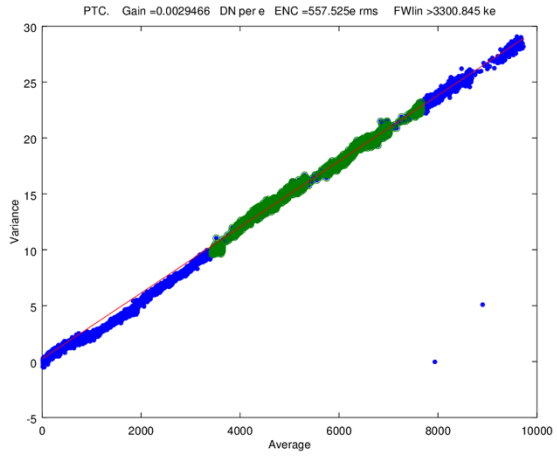

Figure 8. Photon transfer curve applied to the low gain section of the pixel. Blue: measured point; green: points over which a log-log ft gives a slope of 0.5; these points are used to extract the gain; red: fitted curve

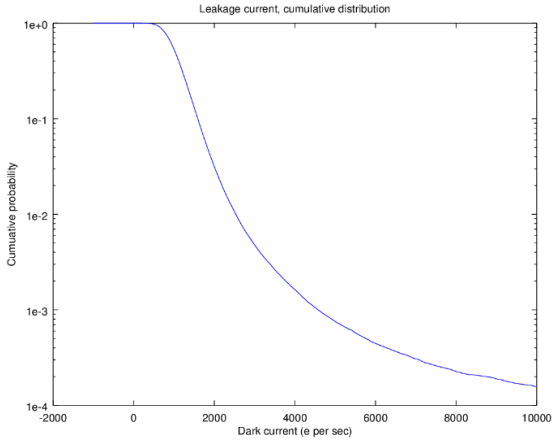

Figure 9. Cumulative dark current distribution, measured at room temperature.

V. Conclusions.

A 1.94Mpixels, high-dynamic range, CMOS image sensor for intraoral dental X-ray imaging is presented. The sensor features 18.5 µm pixels arranged in an array of 1612x1204 pixels. The pixels can be binned in a 2x2 group in the charge domain, thus achieving HDR operation in both full frame and binned mode. The dynamic range of the sensor is measured to be of 94.3 dB. The sensor was manufactured in a 180 nm CIS process. It was designed first-time right and is currently in production.

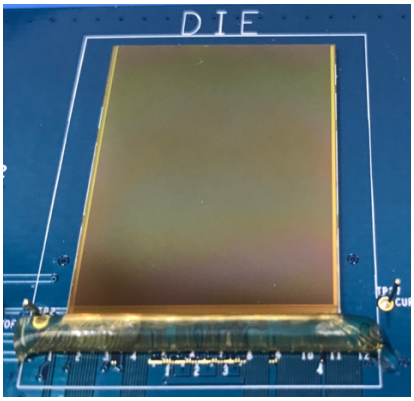

Figure 10. Microphotograph of the chip mounted on a test board.

Parameter	Value
Technology	180 nm CIS
Pixel architecture	6.5T, HDR
Pixel size	18.5µmx18.5µm
Format	1612 x 1204
Megapixels	1.94
Pixel binning	2x2, charge domain
Reset	Global and rolling
ADC	Column-parallel Incremental ΣΔ
Accuracy	14 bits
Conversion time	8 µsec
Data I/O	Up to 5 LVDS pairs at 200 MHz
Frame rate	6.4 fps with 1 LVDS output
	31 fps with 5 LVDS outputs
ENC(HG) [e- rms]	75
ENC(LG) [e- rms]	340
FW(HG) [ke-] sat	355
FW(LG) [ke-] sat	4,000
DR in HDR	51,800
	94.3 dB
	15.7 bits
Leakage current (e-/sec @RT)	1,100

Table 2. Summary of sensor features

References

[1] Bohndiek, S. E., Blue, A. , Clark, A. T., Prydderch, M. L., Turchetta, R., Royle, G. J. and Speller, R. D. (2008) Comparison of methods for estimating the conversion gain of CMOS active pixel sensors. IEEE Sensors Journal, 8(10), pp. 1734-1744.

[2] J. Márkus, J. Silva and G. C. Temes, "Theory and Applications of Incremental Delta Sigma Converters," IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, vol. 51, no. 4, pp. 678-690, 2004.