Pixel with nested photo diodes and 120 dB single exposure dynamic range

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This paper present a 3.0 µm pixel with two nested photo diodes. The pixel has a dual gain readout with overflow on the small diode, so that it has three response slopes. The single exposure (flicker free) dynamic range is 120 dB and the SNR stays above 25 dB at each of the two transition points. The nested photo diodes improve the color accuracy for the small photo diode compared to a traditional staggered dual photo diode approach.

Motivation

The most common technique for extending the dynamic range of an image sensor is the multiple exposure technique [1,2,3] where images with different integration times are combined to generate one HDR image. This method generates artefacts in case of motion in the scene or in case of pulsed light sources. The case with pulsed light sources is of particular interest for automotive applications since traffic signs and tail lights of cars often use pulsed LEDs.

More preferred approaches for increasing the dynamic range capture all data during a single integration time. The dynamic range can then be increased by reducing the read noise like [4], by increasing the maximum signal by in-pixel multiple gain [5,6] or overflowing to a low gain capacitor like [7,8,9]. Another technique to generate two signals with different response slopes is the dual photo-diode technique [10,11]. The photo diode region in the pixel is divided in a large and a small section where the large section collects most of the photo generated electrons. The response ratio of the two photo diodes is called the optical ratio.

Pixel concept

The presented pixel combines a dual photo diode approach with overflowing to a low gain capacitor. This gives the pixel three gains. The highest gain is the large photo diode read in high conversion gain. The middle gain is the small photo diode read in high conversion gain and the lowest gain is the overflow signal from the small photo diode read in low conversion gain. Figure 1 shows the schematic of the pixel. The large photo diode (PD1) has an anti-bloom (AB) gate that allows excess charge to flow towards the supply instead of overflowing over the transfer gate towards the low gain capacitor. Only overflow charge from the small diode (PD2) is collected on the low gain capacitor.

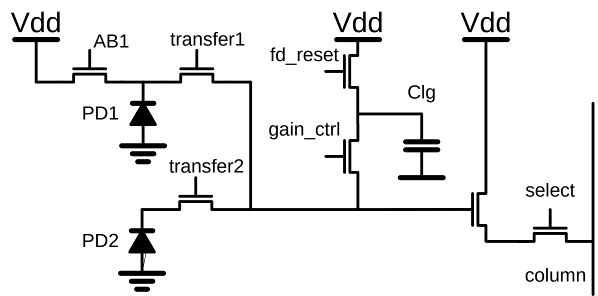

Figure 1: The pixel is a two way shared pixel with a dual gain readout. Only the large photo diode (PD1) has an AB gate since the small photo diode (PD2) will overflow to Clg.

Typically the large and small photodiode are adjacent to each other. e.g. by placing the small diodes on the corners of the large diodes [11]. The presented pixel improves on this by placing the small photo diode in the center of the large photo diode. Figure 2 shows a concept drawing of the deep photo diode layers. These layers define the optical performance of this BSI pixel. The photo diodes are smaller on the shallow photo diode layers at the front surface the sensor. The in-pixel circuits and the low gain capacitor are placed over a part of the deep diode.

The two main advantages of a common center for the diodes are improved color reproduction for the small diode and absence of a sub-pixel shift between the two images. The latter is mainly important for machine vision algorithms that detect the exact location of features in the image.

Figure 2: Concept drawing of the layout of the photo diode layers. The small photo diode is in the center of the large photo diode.

Trade-offs

Figure 3 shows a simulated SNR curve with the three dynamic range (DR) sections (referred to as E1, E2 and E3). The figure is annotated with the key parameters that define the shape of the SNR curve. There is a trade-off between overall dynamic range and minimum SNR at the transitions between the sections. The two key parameters are the optical ratio between the photo diode responses and the conversion gain ratio between the high and low conversion gain also referred to as the capacitance ratio.

The SNR1 point on the E1 read sets the start of the DR. The equivalent PD1 charge of the of the saturation point of the low gain PD2 overflow read sets the end of the DR. Increasing the optical ratio implies that less photo generated charge is collected on the small PD2. This shifts the E2 and E3 curves to the right, to higher equivalent PD1 charge. While this increases the overall dynamic range it also reduces the minimum SNR on the E1/E2 transition. The E1/E2 transition point is set by the full well charge (FWC) of the E1 read. A higher optical ratio implies that at the fixed E1 FWC the E2 signal is smaller and hence the SNR will be worse. Practically, with the available FWC the optical ratio should be 16 to keep the SNR above 25 dB at the E1/E2 transition.

Increasing the capacitance of the low gain capacitor extends the DR at the high side since it increases the FWC of the overflow signal of the small PD2 (E3 signal). As long as the E3 SNR is shot noise limited at the E2/E3 transition, there is little penalty to increasing the low gain capacitance. Practically, the low gain capacitance is maximized within the available space. The capacitor is a poly on diffusion capacitor (NMOS capacitor) that competes for area with the shallow photo diodes and the in pixel transistors. With the available capacitor, the capacitance ratio is about 16.

The PD2 full well charge sets the E2/E3 switch point and the exact location has limited impact on the temporal SNR when the E3 SNR is shot noise limited at the transition. However, at high temperature the spatial SNR and hence to total SNR will be limited by the E3 dark signals non-uniformity (DSNU). The DSNU is caused by (floating) diffusion leakage current. The impact of the leakage current can be minimized by shifting the switch point to a higher signal and hence the PD2 full well charge should be maximized. This is a weak point of this architecture since the FWC of the small PD2 will always be limited and the impact of the DSNU will be higher than for a single photo diode overflow pixel [9].

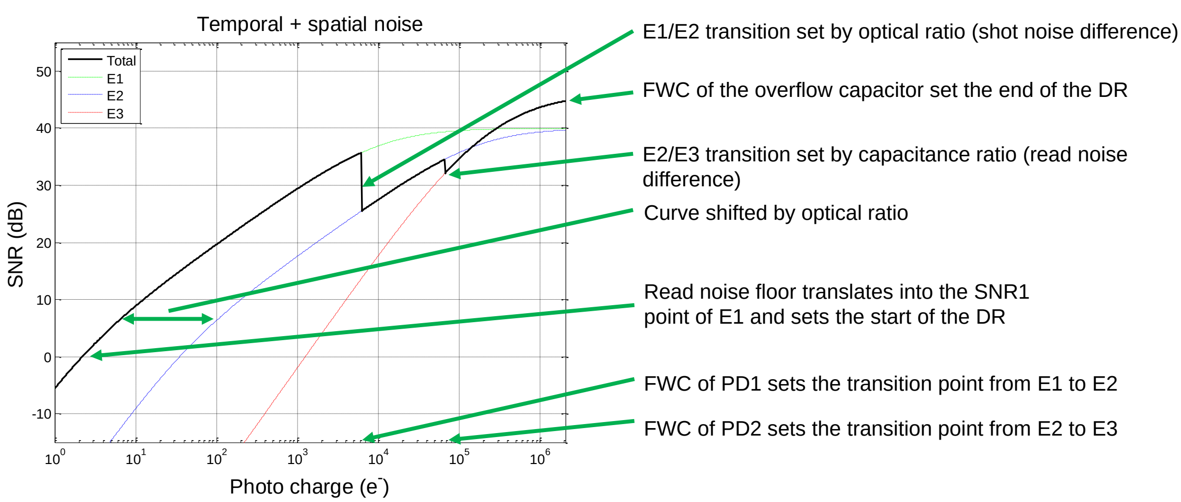

Figure 3: Simulated SNR as a function of PD1 equivalent photo charge. E1 (green), E2 (blue) and E3 (red) refer to the three sections of the dynamic range. E1 is the highest gain, E3 the lowest.

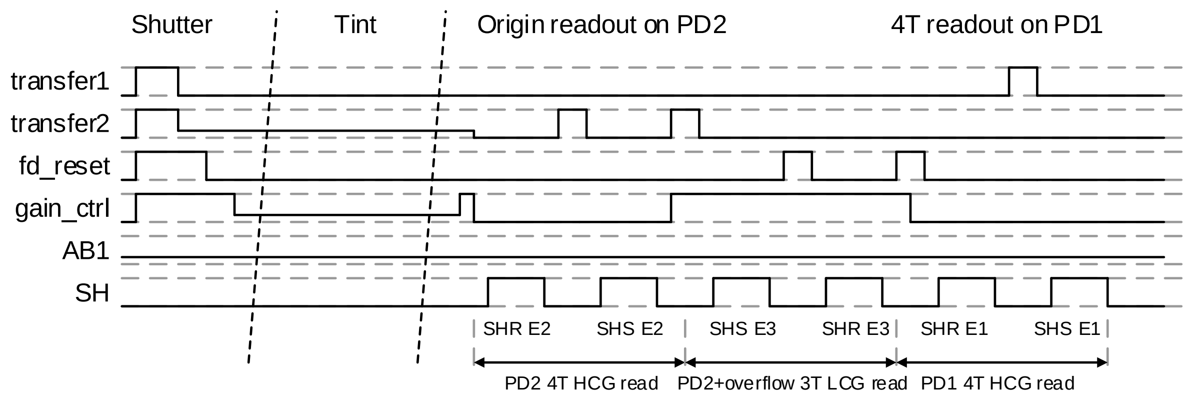

Figure 4: Timing diagram. The pixel timing consists of an origin mode readout of the PD2 and PD2 overflow signals and a 4T readout of the PD1 signal.

Operation

Figure 4 shows the timing diagram for the baseline operating mode. Since the PD2 overflows to the low gain capacitor, the readout sequence has to start with the reads related to PD2. In this timing the PD2 photo diode charge is read first in a 4T CDS read followed by charge summed PD2 photo diode and overflow signal in a low gain 3T DS read. In the last phase PD1 is read in a regular 4T CDS read.

During the integration time, the overflow barriers on AB1, transfer2 and gain_ctrl need to be tuned such that PD1 overflows to the supply and PD2 overflows to the low gain capacitor. Blooming from one photo diode to the other also has to be avoided. All of this can be done either by voltage or by process tuning.

Characterization

The main challenge in the design of a multiple photo diode pixel is the optical performance. For any multiple gain high dynamic range scenario it is critical that the ratio between the gain channels is constant to avoid non-linearity's and color shifts at the switch points. In case of a dual photo diode pixel this implies that the QE of the large and small photo diode have to track exactly over wavelength within each color channel.

Figure 5 shows the (absolute) QE of the large photo diode plotted together with the scaled up QE of the small photo diode. The plot shows for each color channels the data of the micro lens design that results in the closest to target and flattest optical ratio. The used scaling factors are also optimized for each of the color channels individually. This is acceptable since in the product each color channel can have a dedicated micro lens design since the minor variation is in the lens design have very little impact on the neighboring pixel.

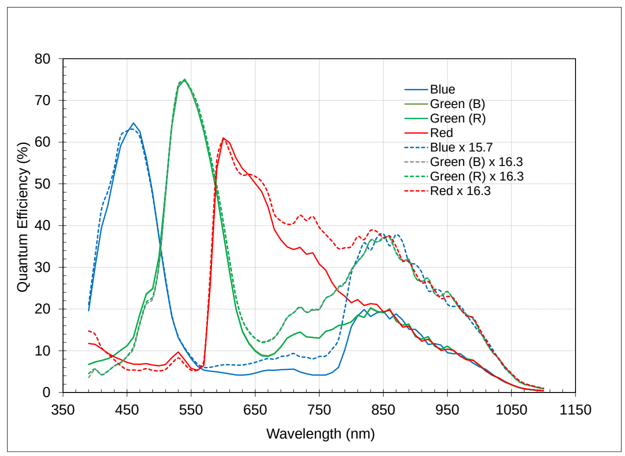

Figure 5: Quantum efficiency (QE) as a function of wavelength for PD1 (solid) and PD2 scaled up by the respective optical ratio for each color channel (dashed).

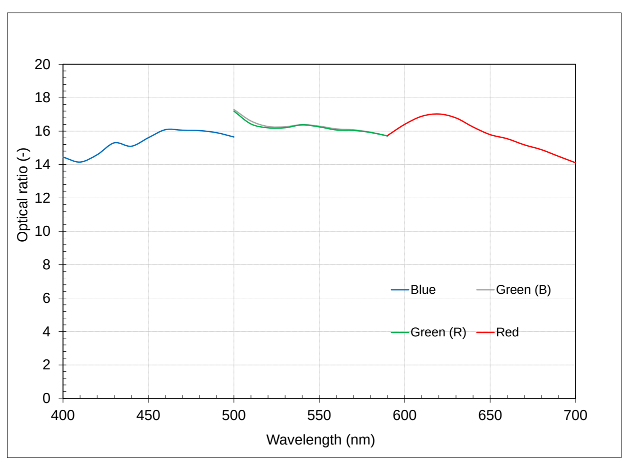

Figure 6: Optical ratio as a function of wavelength plotted only for the visible range and for the passbands of each of the color filters. In the passbands the optical ratio is quite flat and close to the target of 16.

Figure 6 shows the optical ratio plotted only for the passbands of the respective color filters. These are the most relevant regions since a variation in the optical ratio of the stopband will have little impact on the overall signal of the channel, except for narrowband light where it will still have only a minor impact on the perceived color. The optical ratio in the passbands is quite flat and close to the target of 16.

Figure 7 shows the SNR as a function of signal for the three pixel reads. This plot combines data from several measurements since it was not possible to cover the entire dynamic range in one measurement due to limitation of the test chip and the light source. The data from high and low analog gain measurements is merged. On a product with a low unity gain read noise floor this will not be required. The graph shows an SNR1 on the E1 read of about $2e^-$ in high analog gain and a saturation full well charge on E3 of about 170 ke^-. The SNR drop on the E2 (blue) to E3 (red) transition near the full well of the E2 (blue) curve is very limited and the SNR stays above 30 dB. The SNR drop on the E1 (green) to E2 (blue) transition is not visible on this graph since it doesn't show information on the optical ratio. The E2 and E3 curves need to be shifted by 16x to the right to put the x-axis in equivalent PD1 signal. With an optical ratio of 16, the SNR will be 25 dB at the E1/E2 transition at room temperature. The total dynamic range is:
~20*log10(16*170000/2) = ~122 dB.

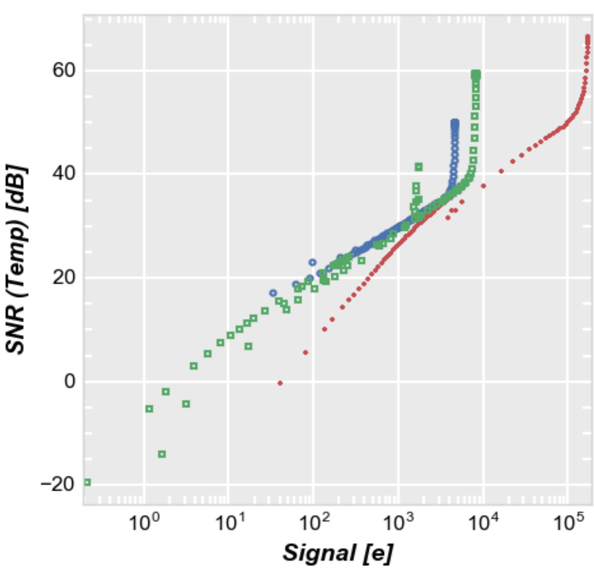

Figure 7: Temporal SNR as a function of signal. For the PD1 high conversion E1 read (green, high and low analog gain), PD2 high conversion gain E2 read (blue) and PD2 low conversion gain origin E3 read (red). The signal axis represents the actual charge and hence the optical ratio and overall dynamic range is not visible in this plot.

Conclusion

This paper presents a work in progress. The measurements are done on a far from perfect test chip that doesn't allow to measure a 120 dB DR in one sweep. Additionally we don't have measurements from a single piece of silicon that combines the best electrical properties with the optimized micro lens layout for each of the color channels. However, with a bit of cherry picking the data, this paper does show a path to a single exposure 120 dB DR pixel. Thanks to the nested layout, the small diode doesn't suffer from crosstalk from other colors and the optical ratio is flat across wavelength. This will allow good linearity and color consistency across the transition from the large to the small diode.

Table 1: key specifications

Parameter	**Specification**
Pixel Size	3.0 µm x 3.0µm
Pixel Type	2 way shared 4T with dual gain
Shutter Type	Rolling Shutter
Temporal Noise	$2e^-$ (in test chip @ 8x gain)
FWC E1	6.3ke^- (lin) 8.3ke^- (sat)
FWC E2	3.7ke^- (lin) 4.6ke^- (sat)
FWC E3	112ke^- (lin) 172ke^- (sat)
Peak QE	80% at 540 nm (PD1+PD2)
Optical ratio	~16
Capacitance ratio	~16
Dynamic Range	~120 dB
SNR@transitions	> 25 dB

References

[1] O. Yadid-Pecht and E. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling", IISW 1997

[2] J. Solhusvik et al., "A 1280x960 3.75um pixel CMOS imager with Triple Exposure HDR", IISW 2009

[3] S. Velichko et al., "140dB Dynamic Range Sub-electron Noise Floor Image Sensor," IISW 2017

[4] B. Fowler et al., "Wide Dynamic Range Low Light Level CMOS Image Sensor," IISW 2009

[5] I. Takayanagi et al., "An 87dB Single Exposure Dynamic Range CMOS Image Sensor with a 3.0µm Triple Conversion Gain Pixel,"IISW 2017

[6] F. Lalanne et al., "A native HDR 115dB 3.2µm BSI pixel using electron and hole collection," IISW 2017

[7] N. Akahane, et.al. "A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor," in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 851-858, April 2006.

[8] T. Geurts et al., "A 98dB Linear Dynamic Range, High Speed CMOS Image Sensor," IISW 2017

[9] M. Oh et al., "3.0um Backside illuminated, lateral overflow, high dynamic range, LED flicker mitigation image sensor," IISW 2019

[10] T. Willassen et al., "A 1280×1080 4.2µm Split-diode Pixel HDR Sensor in 110nm BSI CMOS Process," IISW 2015

[11] S. Iida et al., "A 0.68e-rms Random-Noise 121dB Dynamic-Range Sub-pixel architecture CMOS Image Sensor with LED Flicker Mitigation," IEDM 2018