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Dark Current Limiting Mechanisms in CMOS Image Sensors

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Introduction to Dark Current

Definition:

Dark current is the signal from a typical pixel that is not due to photons

- Dark current is physical charge
- Dark current in current technology is not understood
- Understanding is needed to drive improvement

Corollary:

Photo-carrier collection tends toward equilibrium

Dark current caused by thermal processes does the same

Dark current is a charge-domain offset in dark frames & in image frames

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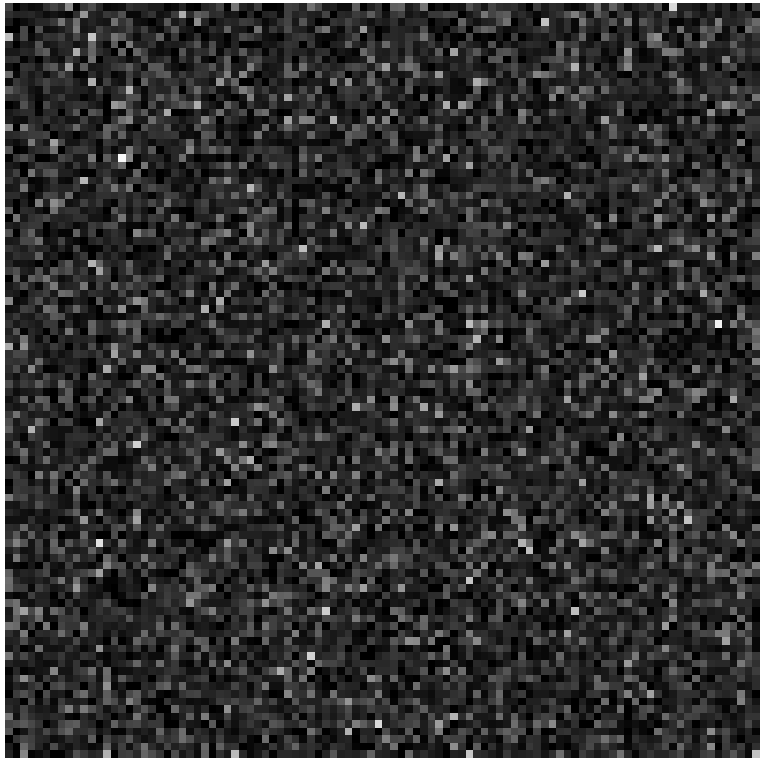
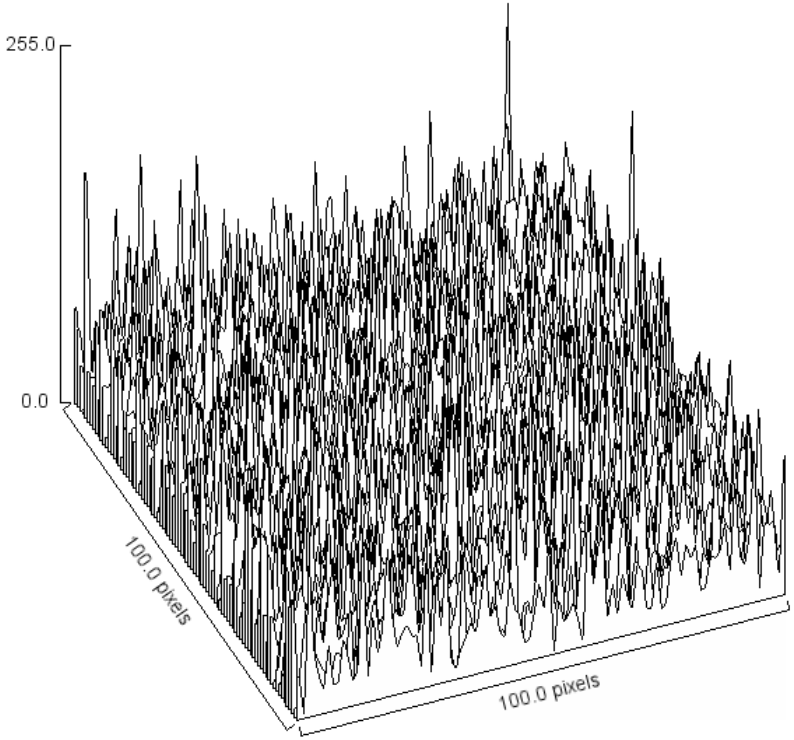
The present state & mystery [1]



Synthetic dark image appears grainy



Surface plot shows combination of "grainy" gray & of "snow" spikes

- Dark current is what happens in every pixel
- Defects happen only in some pixels – not the subject of this talk

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The present state & mystery [2]

R.H. Dyck, M.D. Jack, Low Light Level Performance of a Charge-Coupled Area Imaging Device, 1974 CCD Workshop, Edinburgh, UK

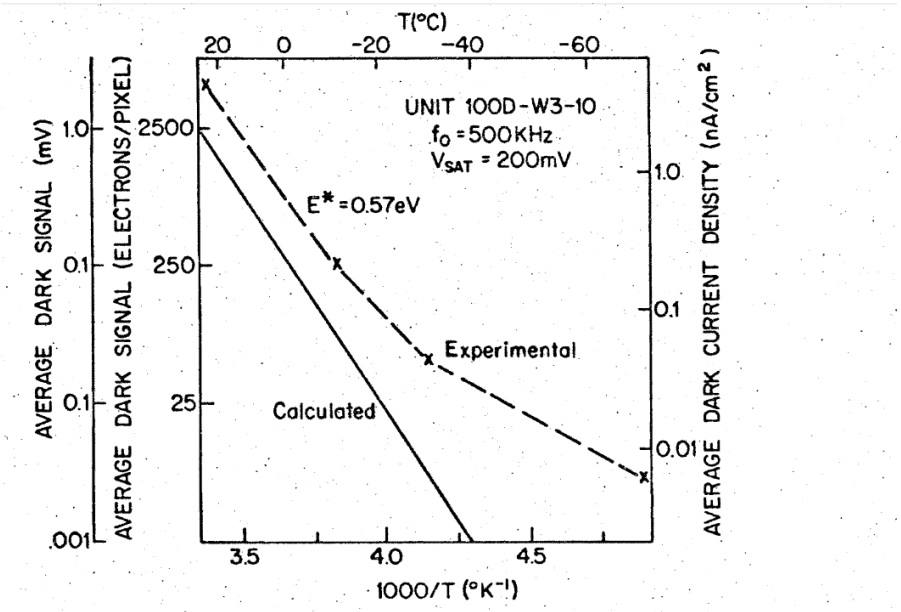
1974:

- Room temperature dark current of 2 nA/cm2
- temperature dependence is SRH ($E_g/2$)

2015:

- Room temperature dark current of 0.4 pA/cm2 ⇒ 5000x improvement
- temperature dependence is bandgap (E_g)

M.Kobayashi, et al, A Low Noise and High Sensitivity Image Sensor with Imaging and Phase-Difference Detection AF in All Pixels, 2015 IISW, Vaal, Netherlands
Canon Inc. ⇒ 20 pA/cm2 60C



EXPERIMENTAL AND CALCULATED CURVES OF DARK CURRENT VS. TEMPERATURE. THE EXPERIMENTAL DATA WAS TAKEN WITH A UNIT EXHIBITING AN AVERAGE DARK CURRENT OF 2 nA/cm^2 AT ROOM TEMPERATURE. THE TWO ORDINATES ON THE LEFT GIVE THE DARK OUTPUT AND THE CORRESPONDING DARK CHARGE PER PIXEL. THE ORDINATE ON THE RIGHT GIVES THE CALCULATED DARK CURRENT DENSITY.

- 5000x improvement in Dark Current;
- Shift in temperature dependence indicates shift in mechanism

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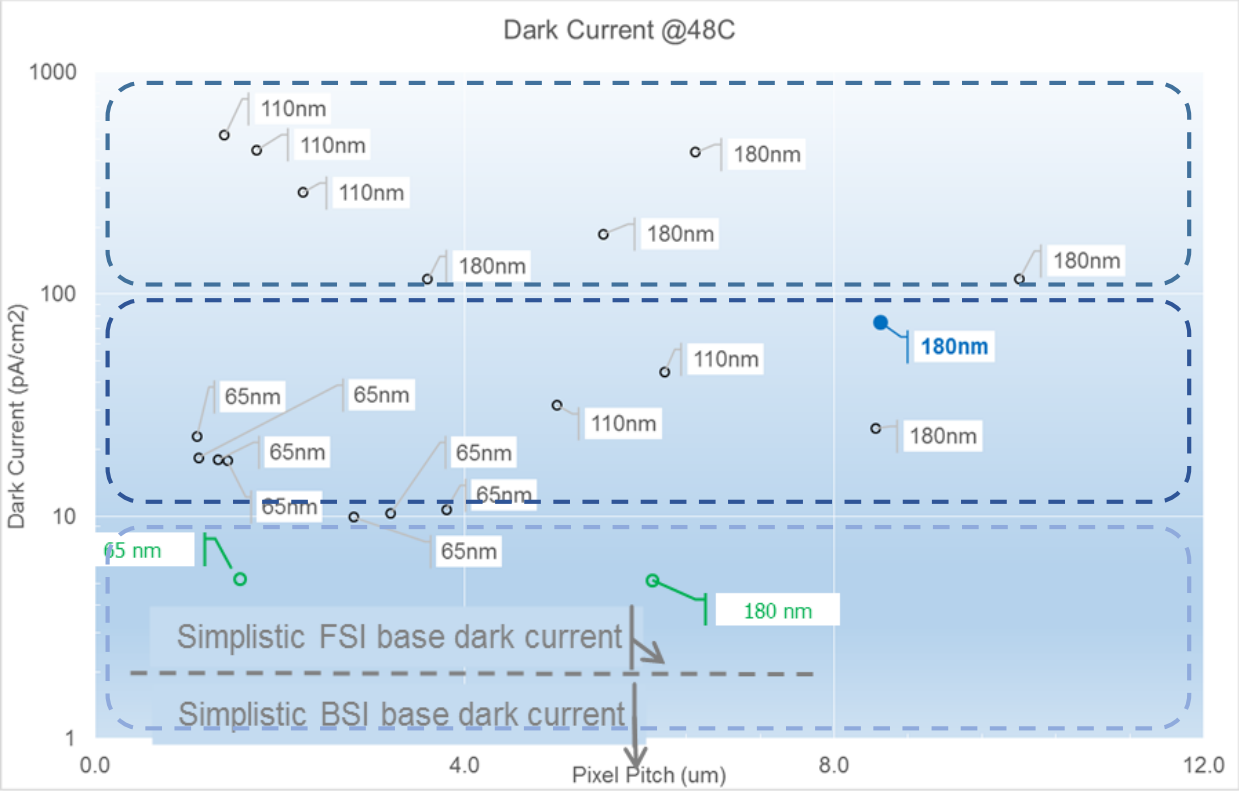
The present state & mystery [3]



- Dark current data for a selection of world-class CIS foundries:
- Dark current has progressed with nominal 10x scaling per technology node
- Dark current in a technology seems best characterized "per pixel area"

- Commercial applications have & are pushing development as constant improvement
- At some point there is a limit: defect-free silicon limited or device-limited
- Neither is understood

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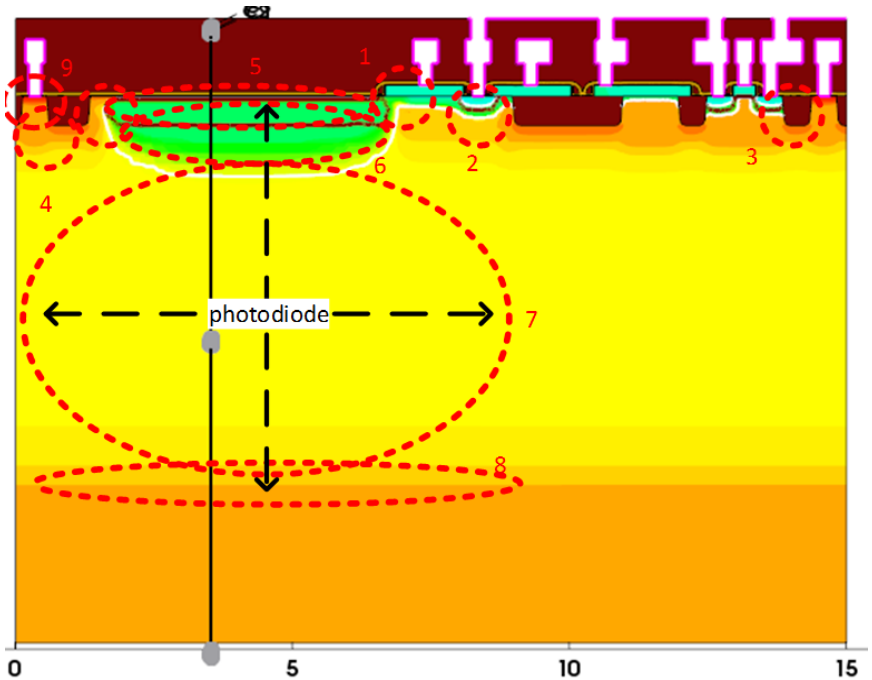
Pixel



I want to acknowledge Nobu Terenishi's talks also exploring root cause of "diffusion" dark current

Dark current sites within pixel:

1. **TX edge: diffusion from interface (E_g); lucky drift from interface ($E_g/2$); interface stress (E_g);**
2. FD injection: blooming forward bias;
3. Other junction: forward bias or carrier injection;
4. STI interface: diffusion from interface (E_g); interface stress (E_g);
5. Pinning layer: diffusion from interface (E_g); interface stress (E_g); doping-based SRH (E_g);
6. **Deep depletion: SRH from contamination ($E_g/2$);**
7. Lightly doped region: diffusion from weak SRH ($E_g/2$ or E_g);
8. **Back interface: diffusion from weak interface SRH (E_g);**
9. Contact substrate current (Eg)

- Many possibilities exist for dark current in the pixel

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Pixel: Dark current sources

Source	Location	Dependence	Comments
Metallics	Photodiode depletion region	• "$E_g/2$" temperature dependence (~10C doubling); • Photodiode depletion area & volume	• Reduced by bulk gettering, use of screen oxides, cleaning & implant contamination control
Interface states	TX-gate-edge depletion region	• "$E_g/2$" temperature dependence (~10C doubling); • TX gate width dependence	• Should be isolated from photodiode by bulk barrier
Substrate diffusion current	Bulk silicon (depleted & un-depleted)	• "E_g" temperature dependence (~6C doubling); • Pixel area dependence • Presence of un-depleted substrate	• Minority carrier diffusion • *Should be reduced by BSI thinning*
Pinning layer diffusion current	Photodiode pinning layer	• "E_g" temperature dependence (~6C doubling); • Pixel area dependence	• Sensitive to dielectric-induced stress
STI diffusion current	STI edge	• "E_g" temperature dependence (~6C doubling); • STI length • STI depth	• Sensitive to STI corner stress • Impact of STI engineering & depth has reduced
Back surface diffusion current	Back interface for thinned device	• "E_g" or "$E_g/2$" temperature dependence • Pixel area dependence	• Mitigated by accumulation in present BSI
Contact diffusion current	Contact	• "E_g" temperature dependence (~6C doubling)	• Diffusion through substrate from contact
Gate injection	TX edge	• Weak temperature dependence • Gate voltage dependence	• Should be isolated from photodiode by bulk barrier
Gate-induced diode leakage	TX edge	• Weak temperature dependence • Non-linear TX gate voltage dependence	• Due to high fields • Isolated from photodiode by bulk barrier
Spill back dark current	TX edge	• "E_g" or "$E_g/2$" temperature dependence • TX gate width dependence	• Should be isolated from photodiode by bulk barrier
Dopants	Bulk silicon	• "E_g" temperature dependence	• SRH with shallow traps
Auger / Impact ionization	Bulk silicon	• "E_g" temperature dependence	• Requires valence band momentum transfer

- More possibilities other than contamination & interface states exist for dark current

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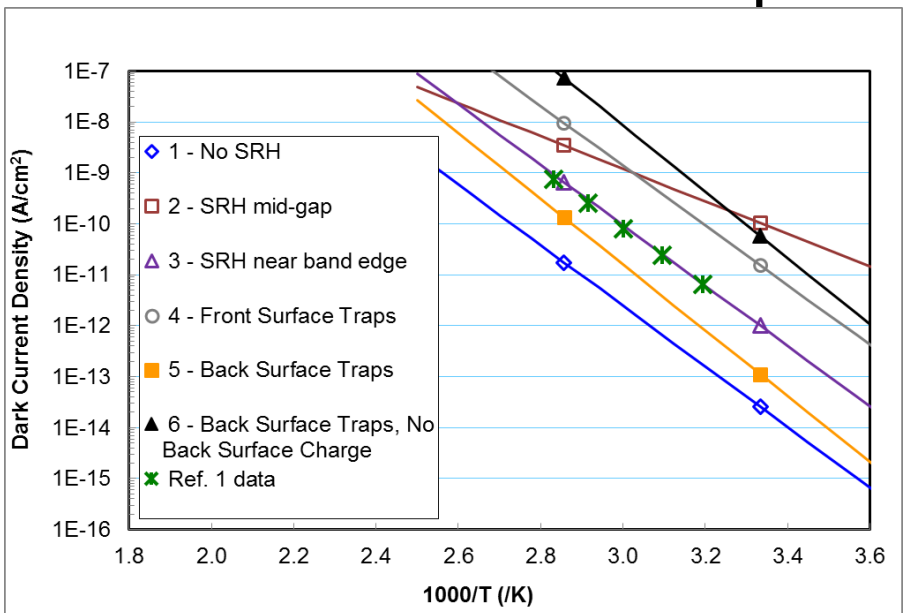
Dark Current Temperature Dependence



Curve #	1	2	3	4	5	6	Parameters
Ea (eV)	1.18	0.64	1.18	1.16	1.28	1.29	
Bulk SRH, mid-gap		X					Et=0, tau=1e-3 s
Bulk SRH, near band edge			X				Et=0.5, tau=4.6e-8 s
Front surface SRH, mid-gap				X			Et=0, Nit=1e11 cm-2
Back surface SRH, mid-gap					X	X	Et=0, Nit=1e11 cm-2
Back surface fixed charge	X	X	X	X	X		Qf=-1e12 cm-2

3-d simulation of pixel dark current mechanisms. E_t is the SRH trap energy relative to mid-gap. E_a is the activation energy from the slope of the curve.

Ref. 1) H. Rhodes et al, "The Mass Production of Second Generation 65 nm BSI CMOS Image Sensors", 2011 IISW, Hokkaido, Japan

- TCAD can generate a prediction for defect-free silicon with ~E_g temperature dependence
- E_g temperature dependence can result from various mechanisms
  - Front or back surface generation & diffusion
  - SRH for traps near the band edge
  - SRH for dopants

- TCAD has hooks to simulate dark current due to process & design
- TCAD has limit because it does not consider that carriers are quantized

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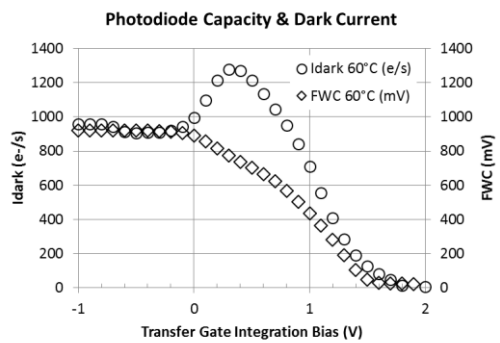
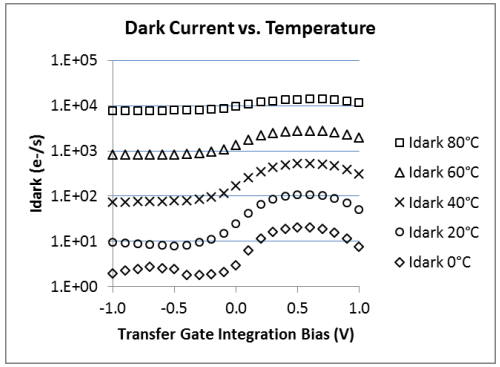
Characterization: probing the pixel

- Temperature dependence
  - Dramatic due to exponential dependence of Boltzmann equation
  - Leads to use of 'doubling temperature' as metric:
    - Eg/2 ~ 11 C/doubling
    - Eg ~ 6 C/doubling
- Voltage dependence
  - Biasing shapes the depletion region
    - Changes the volume
    - Creates inversion layers
    - Changes the dopants
    - Moves barriers





- Device operation is a window into pixel dynamics

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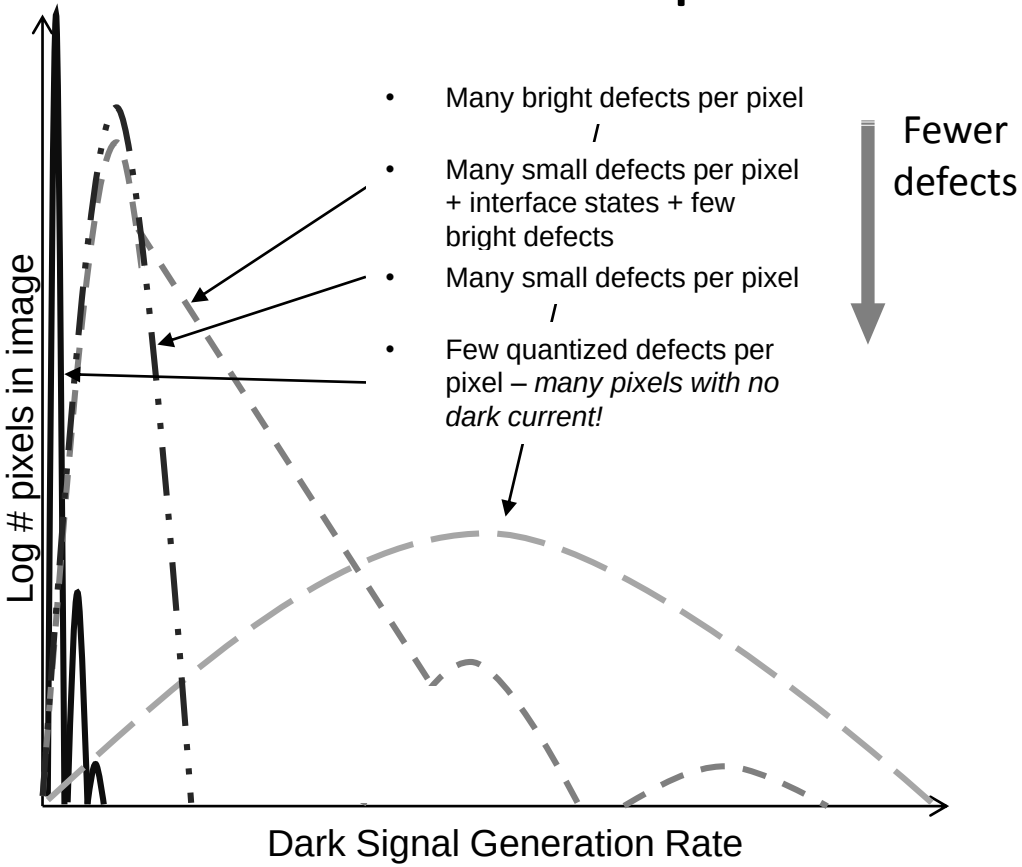
Dark Current Spectroscopy (DCS)



Impact in the Photon Counting World:

- Reduced dark current is critical for photon counting imagery
- The *dark current changes from looking like background noise to looking like "false positive" signal*
- Dark current will be a random phenomenon *quantized in space & time*

- Progression of dark current in the pixel
- Dark current quantization means that in the extreme-low dark current required for photon counting most pixels most the time will have no dark current

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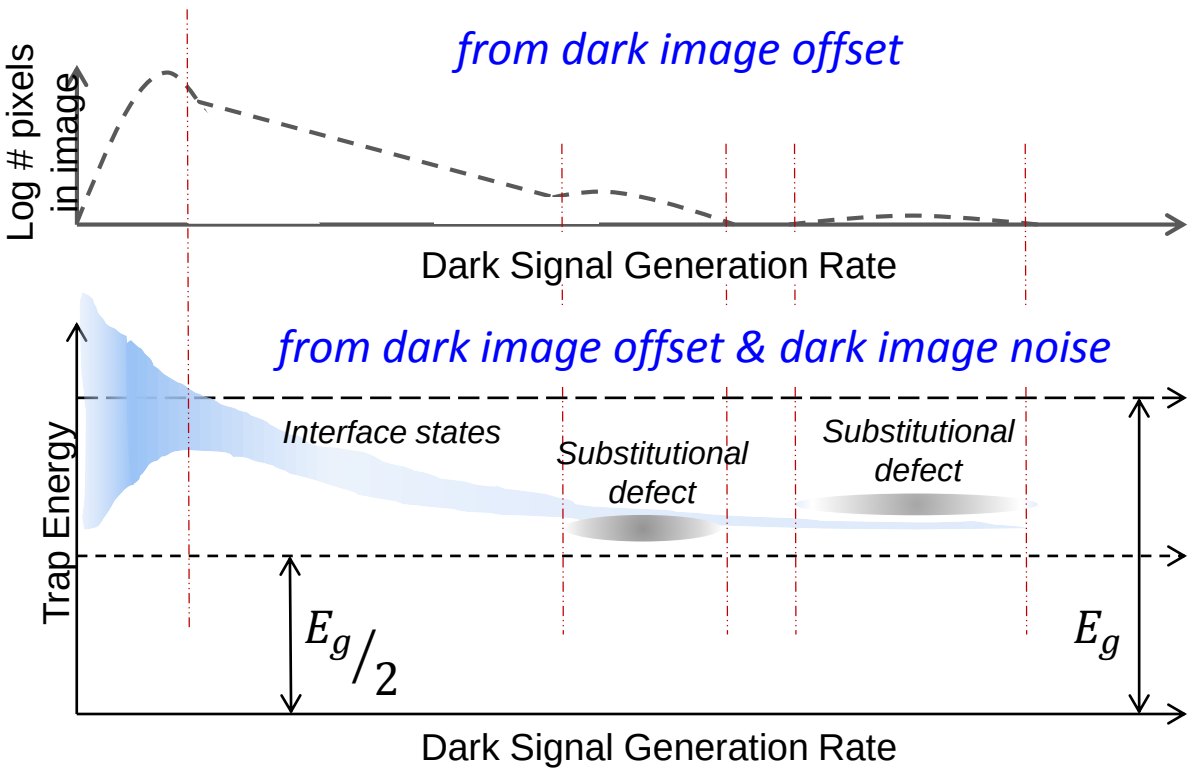
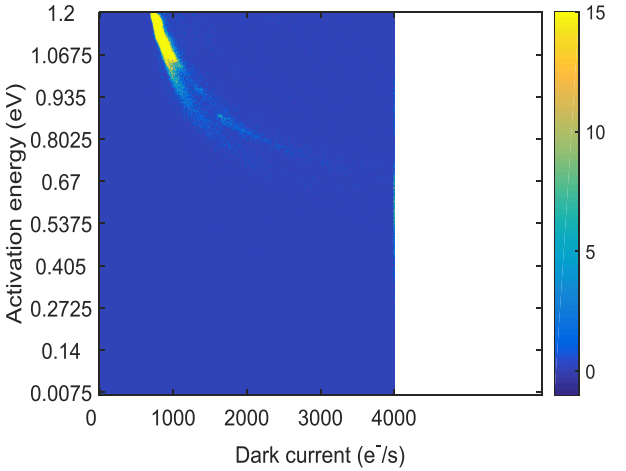
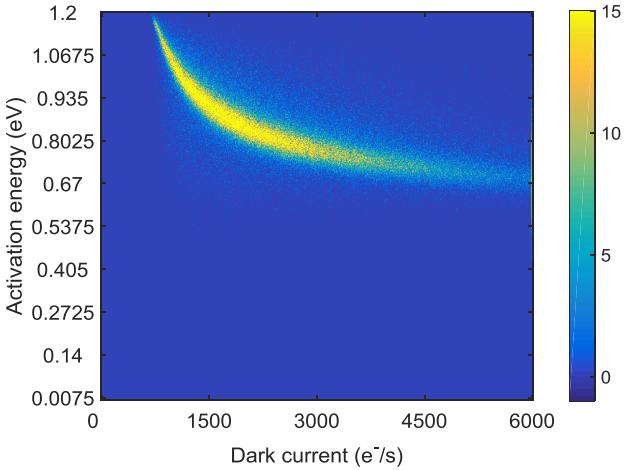
2-d DCS







- Many more possibilities exist for dark current

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Past progress & present mystery

Past progress:

- Initially uniform dark current was dominated by interface states; these were eliminated by use of inversion & pinning layers: CCD & CIS pinned photodiodes
- Snow-like dark current addressed by using DCS as a tool to relegate metallics to be only "bright pixels" through contamination control & gettering
- Dark current temperature dependence shifted from ~11 C/doubling to ~6 C/doubling

Present conundrum:

- Manufacturing improvements aimed at contamination does not address ~6 C/doubling
- Categorizing ~6 C/doubling as "diffusion current" does not provide an "actionable" root cause
  - *Dark current diffusion is backwards from p-n junction diffusion (e- flow is from p-to-n instead of n-to-p)*
  - *Question of whether "diffusion" in image sensor without recombination*
- No root cause connecting dark current & process

- Root cause is needed to have actionable improvement

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Limits of dark current in silicon [1]

Simplistic model for deep-depleted photodiode

a. Model is for deep-depletion photodiode, undepleted pinning layer & undepleted substrate
b. E_g = 1.12eV
c. Lifetime is limited by Auger process:
    a. electron promoted into conduction band
    b. hole created in valence band
    c. electron or hole that conserves momentum
d. Generation lifetime equals equilibrium recombination lifetime: $\tau_{1/2} = 2.5 \cdot 10^{-3}\ s$
e. No recombination occurs because electrons generated are swept away due to electric fields
f. Charge generation depends on Δn, the concentration difference from equilibrium

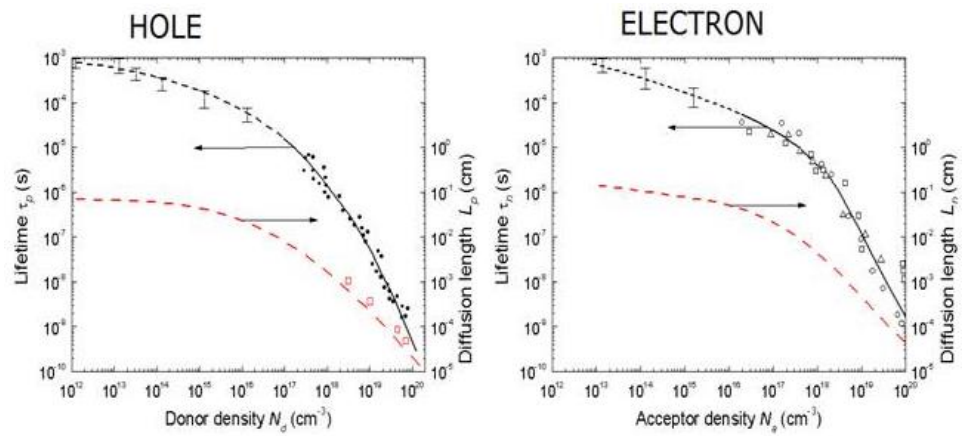

Figure 1. Hole and Electron Bulk Lifetime for different Silicon Doping [3-4]

M. S. Tyagi and R. Van Overstraeten, Minority carrier recombination in heavily-doped silicon, Solid-State Electron.,vol. 26, pp. 577 1983.

Calculations carried out for nominal T = 27C

- Simple model based on Auger process looks at "pinning layer + depleted PD + undepleted"

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Limits of dark current in silicon [2]

Simplistic model for depleted volumes in photodiode

1. Available electrons are the valence band density of states: $N_V = 3.1 \cdot 10^{19}\ cm^{-3}$
2. Conduction band electron concentration given by Boltzmann equation: $n = N_V exp\{-E_g/kT\}$ where $kT = 0.025\ eV$
3. In equilibrium the recombination has exponential decay: $\tau_{1/2} = 2.5 \cdot 10^{-3}\ s$
4. Generation process in all cases equals recombination in equilibrium characterized by the lifetime due to very small acceptor density: $G = -R = n/\tau_{1/2}$

$$G = {}^{N_V exp\{-E_g/kT\}}/_{\tau_{1/2}} = 450\ {}^{e^-}/_{cm^3 \cdot s} = 7 \cdot 10^{-5}\ {}^{pA}/_{cm^3}$$

$$G^{dd}_{FSI\ (\mathbf{1.5\ \mu m})} = 9 \cdot 10^{-9}\ {}^{pA}/_{cm^2}$$

$$G^{dd}_{BSI\ (\mathbf{2.5\ \mu m})} = 1.5 \cdot 10^{-8}\ {}^{pA}/_{cm^2}$$

Calculations carried out for nominal T = 27C

- Conclusion: Negligible dark current from depleted volumes

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Limits of dark current in silicon [3]

Simplistic model for undepleted substrate

1. Equilibrium concentration $n = {n_i}^2/N_A$ where $n_i = 1.0 \cdot 10^{10}\ cm^{-3}$
2. Removing equilibrium constraint leads to exponential-decay recombination which is doping dependent: $\tau_{1/2}$ from Figure 1
3. Generation process equals recombination in equilibrium characterized by the lifetime as acceptor density becoming very small: $G = -R = n/\tau_{1/2} = {n_i}^2/(N_A \cdot \tau_{1/2})$
4. Pinning layer is doped 3x10^{18} cm^{-3} with 0.1 µm depth: $\tau_{1/2}$=10^{-6} s
5. Collection volume for FSI is doped 1x10^{15} cm^{-3} with 6.5 µm depth: $\tau_{1/2}$=2x10^{-4} s
6. Collection volume for BSI is effectively zero

$$G^{pin} = (1.0 \cdot 10^{10}\ cm^{-3})^2/(\mathbf{2 \cdot 10^{18}\ cm^{-3}} \cdot 10^{-6} s) = 3.5 \cdot 10^7 cm^{-3} \cdot s^{-1} = 6\ {}^{pA}/_{cm^3}$$

$$G^{pin}_{(\mathbf{0.1\ \mu m})} = 6 \cdot 10^{-5}\ {}^{pA}/_{cm^2}$$

Calculations carried out for nominal T = 27C

$$G^{collect} = (1.0 \cdot 10^{10}\ cm^{-3})^2/(\mathbf{1 \cdot 10^{15}\ cm^{-3}} \cdot 10^{-4} s) = 1.4 \cdot 10^9 cm^{-3} \cdot s^{-1} = 2 \cdot 10^2\ {}^{pA}/_{cm^3}$$

$$G^{collect}_{FSI(\mathbf{6.5\ \mu m})} = 1.4 \cdot 10^{-1}\ {}^{pA}/_{cm^2}$$

$$G^{collect}_{BSI(\mathbf{0\ \mu m})} = 0\ {}^{pA}/_{cm^2}$$

- Conclusion: FSI undepleted substrate is dominant dark current

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Limits of dark current in silicon [4]

Dark current generation rate (27C)

$$G^{FSI} = G^{dd}_{FSI\,(1.5\,\mu m)} + G^{pin}_{(0.1\,\mu m)} + G^{collect}_{FSI(6.5\,\mu m)}$$
$$= 9 \cdot 10^{-9}\, {}^{pA}/_{cm^2} + 6 \cdot 10^{-5}\, {}^{pA}/_{cm^2} + 1.4 \cdot 10^{-1}\, {}^{pA}/_{cm^2}$$
$$= \mathbf{1.4 \cdot 10^{-1}\, {}^{pA}/_{cm^2}}$$

$$G^{BSI} = G^{dd}_{BSI\,(2.5\,\mu m)} + G^{pin}_{(0.1\,\mu m)} + G^{collect}_{BSI(0\,\mu m)}$$
$$= 1.5 \cdot 10^{-8}\, {}^{pA}/_{cm^2} + 6 \cdot 10^{-5}\, {}^{pA}/_{cm^2} + 0\, {}^{pA}/_{cm^2}$$
$$= \mathbf{6 \cdot 10^{-5}\, {}^{pA}/_{cm^2}}$$

Calculations carried out for nominal T = 27C

Discussion

- Image sensors have not reached the limits of dark current possible in "perfect" silicon, so process improvements are still important to reach the fundamental limit
- FSI is approaching these limits due to the generation in the undepleted collection volume
- BSI could also approach this limit if it introduces thicker silicon enabled by better pixel-to-pixel isolation
- Process improvements that increase the depletion volume should lower the fundamental limits without trading off spectral response

- Dark current limit for simple model

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Looking into a crystal ball darkly

- Conjectures:
  - Commercial pressures will continue to push to reduce dark current
  - General view that improvement is natural fallout from advancing technology nodes
  - Improvement would be helped by identifying root cause of the dominant defect(s)
  - Understanding the root cause provides opportunity for design-driven improvement
  - Data is needed for *actionable* understanding
  - There will be a point where silicon *rather than defects* becomes the limitation ⇒ *only design-driven improvements will be possible*

- Dark current reduction is actionable

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Illumination

- SRH theory has provided a means to understand & eliminate a predominant source of dark current
- Dark current has gone from "gray" background to quantized snow and back to "gray" background. It is about to again be quantized, *this time in space & in time*
- There is no root cause to understand the present dark current
- There is a need for data & analysis
- It is unclear when dark current will hit the limit of pure silicon where process improvements will no longer help.
- When there is an identified root cause then there is the possibility for improvement through design

- Understanding of dark current root cause and limits is needed

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