A 47 MPixel 36.4 x 27.6 mm^2 30 fps Global Shutter Image Sensor

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Introduction

Earlier we reported frontside and backside illuminated image sensors with pipelined 8-transistor CDS voltage domain global shutter pixels with a pixel pitch of 5.5 µm, and resolutions up to 12 MPixel, developed in 0.18 µm CMOS [1,2,3]. We also reported a scaled pixel at 3.5 µm pitch with shared readout, shifted exposure periods between odd and even columns, and using a 110/90 nm process [4]. In this article, we present a 47 MPixel global shutter image sensor with 4.6 µm pixel pitch developed for machine vision applications. Scaling to 4.6 µm pitch was achieved by use of a 90/65 nm CMOS process, without transistor sharing in the pixel, and dynamic range was increased by larger sample capacitors and increased voltage swing. The pixel also uses deep trench isolation for low cross-talk and a low 2 metal Cu stack with 1.5 µm distance between Si and CFA for good angular response.

Fig. 1 shows the architecture of the chip. The device is 1D stitched. One vertical stitch line is centered in the effective pixel area. Additional stitch lines are located in the left and right pixel buffer zones between the active pixels and optical black reference pixels. The sensor supports on-chip binning for monochrome and color as shown in fig. 2 by summation and averaging circuitry in the analog front-end of the column amplifier. The rest of this article discusses specific concerns caused by the large area and high pixel count of the device and concludes with the achieved performance.

Concerns related to the large area pixel array

Fig. 3 shows the 8T pixel schematic and fig. 4 shows the pixel timing in this device. In-pixel sample capacitors are 19 fF and realized through NMOS gates and some parasitic metal capacitance. Conversion gain at the floating diffusion is 81 µV/e- and 1.2V swing is used at the FD. The large resolution and large chip size require specific measures for the design and timing of this pixel. At the end of the exposure, the 8T pixel capacitors must be discharged and the bias current of the 1st source follower must be enabled. This parallel operation in all pixels can cause a large peak current on the pixel array power supply. Timing and bias is adapted to minimize its impact. At the end of the exposure, first the internal nodes in the pixel are cleared through a pulse pattern as indicated in fig. 4. A large bias current (10 nA) is employed to discharge the capacitors. To prevent the large current peak to hit the pixel current supply, the supply line is pulled down when this large bias current flows. Later, during sampling of the FD reset and signal levels, a smaller bias current is employed. This also increases the max. signal amplitude. But the variability of this current through mismatch and process corner variations is considerable since the transistor operates in deep subthreshold. The bias setting is optimized to ensure that enough current flows through each bias transistor to settle the signal levels. To find the optimal bias setting, first the minimum precharge current needed to correctly discharge the capacitors in the allocated time (4 µs) is determined, and then the bias level is selected to ensure that this is reached for >99.9% of the pixels under worst case conditions taking the statistical transistor mismatch data into account. Due to variations in resistance of the ground net, bias currents will be lower in the center of the pixel array. Pixel linearity is verified in simulations with this effect taken into account.

Also the interconnect control lines have significant capacitances and resistances. For example, the total worst-case capacitance and resistance of the TX line are 57 pF and 83 kΩ, respectively. The minimum exposure time is 320 µs in standard operation, limited by the time required for the pulses shown in fig 4. For shorter exposures, a non-pipelined exposure timing mode can be programmed where the min exposure is 125 µs.

Concerns in the design of the column readout circuits

During readout, besides SEL, only S2 is pulsed in the pixel, during 400 ns. In total, 5 µs are available to read the reset and signal levels stored in C2 and C1 respectively into the column amplifiers. The column bus sampling timing and bias scheme of the column load is optimized to increase the signal swing as much as possible and lower the noise.

8160 column amplifiers and column ADCs operate together in a pipelined manner to read out, amplify, sample, AD convert and multiplex the data from one row of pixels in 5.5 µs. Careful distribution of clocks, power and reference signals over the column structures is required. A specific strategy has been followed to eliminate electrical cross-talk effects, which may otherwise shift black levels on a row depending on the amount of saturated or gray pixels on that row, causing 'banding' effects in the image.

1. Counting ramp column AD converters with 2 counters per column are used to achieve the required frame rate and a 12 bit conversion time per row of 5.5 µs. As discussed in [5], this topology ensures a constant power dissipation, independent of the input signal levels. Signal dependent supply variations, which could be a source of row banding effects, are avoided.
2. 2x 98 optical black pixel columns at the left and right sides of the pixel array are used to clamp the black reference level to a fixed register-programmed value. This also brings the temporal row noise at 1/14th of the pixel temporal noise.
3. For the ramp ADC design, a comparator circuit is used that ensures a constant input capacitance, independent of the output state. This circuit also avoids kick-back to the input node at the moment that the comparator toggles.

Fig. 5 shows the comparator design. The ramp signal of the column ramp ADC is generated by a constant current source that integrates its current over a large distributed capacitance, and is connected to one of the inputs of the ADC comparator in each column. A stable reference VB is generated, for example as shown by a current source and transistor M5. The feedback loop will set the current I2 such that VA is always equal to VB. This also ensures that the current I2.1 is constant, independent of the state of the comparator output and equal to I3 if M5 and M1 have the same dimensions. This keeps the input capacitance of M3 constant independent of the Vramp level. Current I2.2 drops once the Vramp level is higher than the ADC_IN level. Fig. 7 shows the timing of the comparator and the current flowing in the different branches.

In the absence of the feedback circuit, it has been found that when the ramp signal Vramp is close to the ADC_IN level, the voltage on circuit node VA will drop because the current I2.1 through transistor M3 would be increasing. The current I2.2 would decrease accordingly such that the sum of both currents I2.1 and I2.2 is always equal to current I2, which is constant without the proposed feedback scheme. Due to the presence of a parasitic capacitor, C2, the voltage drop on VA distorts the Vramp signal as shown in fig. 6 and the slope of the ramp signal Vramp will be lowered because of the change of the input capacitance of M3. The proposed comparator avoids these signal-dependent impacts on the Vramp node.

Concerns on the output interface.

The sampling in the camera of the LVDS output data from a set of source-clock synchronized data channels is typically more sensitive to variations on large area sensors. By implementing a packet based readout mode, including a CRC checksum and information on the position of the data within the image, the data reception is made more robust and flexible. Also 8b10b clock encoding in the serial data stream can be enabled to eliminate clock skew and jitter issues.

Measured results and conclusions

The chip runs at 30 fps at full resolution with 12 bit AD resolution and 2.9W power consumption. Dynamic range is 64.5 dB in full resolution mode and 68.5 dB in 2x2 binned mode. More measured specifications are summarized in table 1. Fig. 8 shows QE for monochrome and color devices. Fig. 9 shows the angular response for vertical and horizontal rotations for red, green and blue wavelengths, measured on a monochrome device. Fig. 10 shows the chip packaged in a 141 pins PGA. All measured parameters were according to the expected values during the design phase, thanks to some of the large area design considerations discussed in this article.

References

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[2] G. Meynants, "Global Shutter Pixels with Correlated Double Sampling for CMOS image sensors", Journal of Adv. Opt. Techn. 2013; 2(2), p. 177-187
[3] J. Bogaerts, et al, "High Speed 36 Gbps 12 Mpixel global pipelined shutter CMOS image sensor with CDS", proc. IISW 2011, pp. 335
[4] B. Wolfs, et al, "3.5 µm global shutter pixel with transistor sharing and correlated double sampling", proc. IISW 2013, pp. 397
[5] G. Meynants, et al, "24 MPixel 36 x 24 mm2 14 bit image sensor in 110/90 nm CMOS technology", proc. IISW 2013, pp. 333

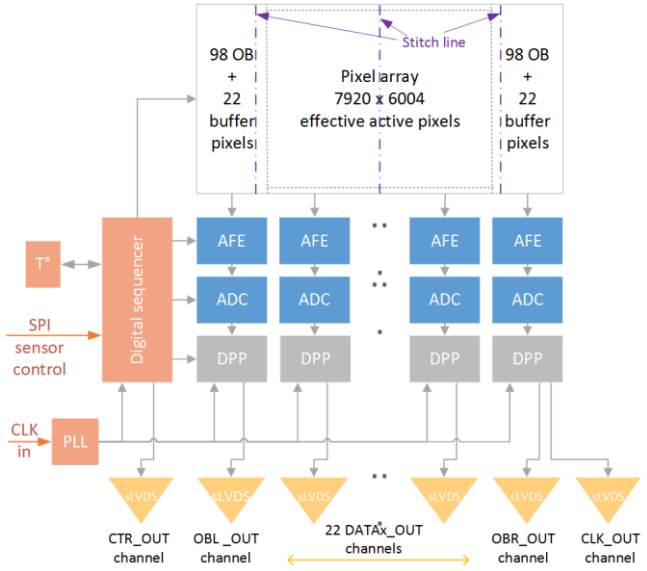

Figure 1 – block diagram

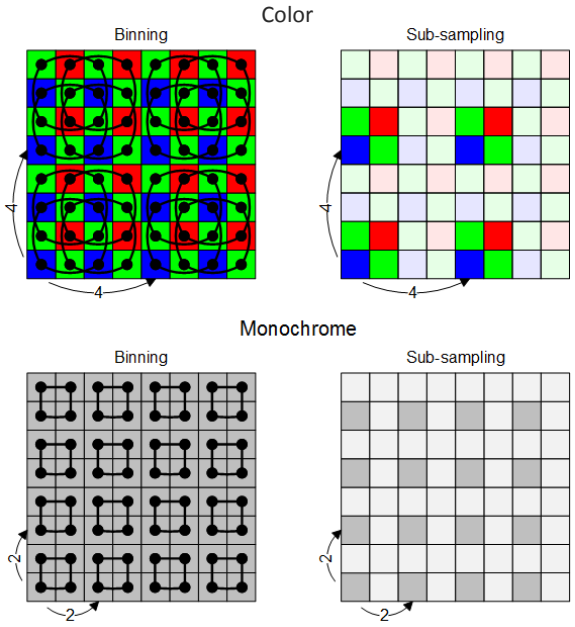

Figure 2 –binning & subsampling modes

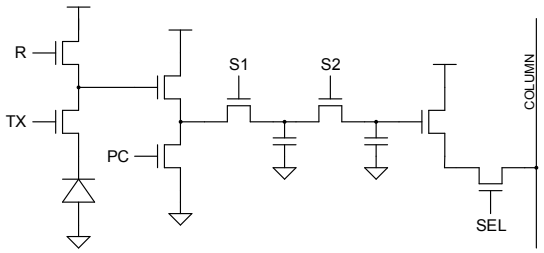

Figure 3 – pixel schematic

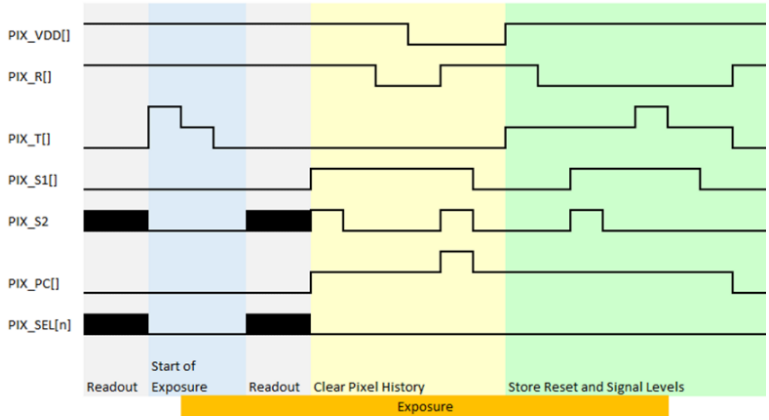

Figure 4 – pixel timing

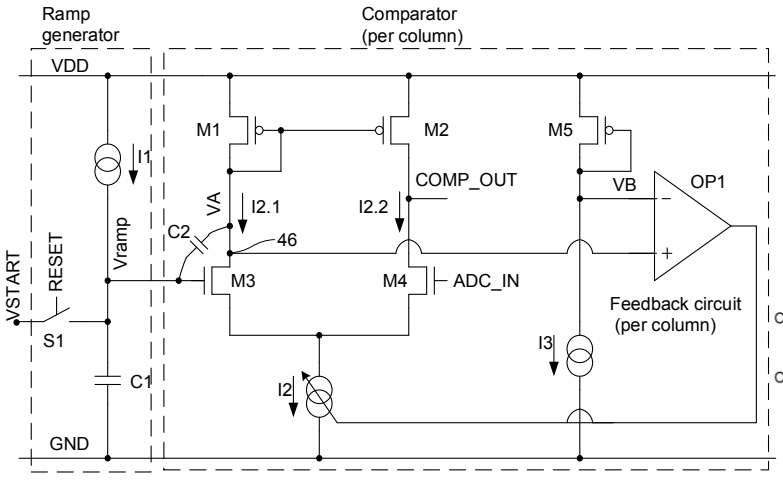

Figure 5 – Comparator design

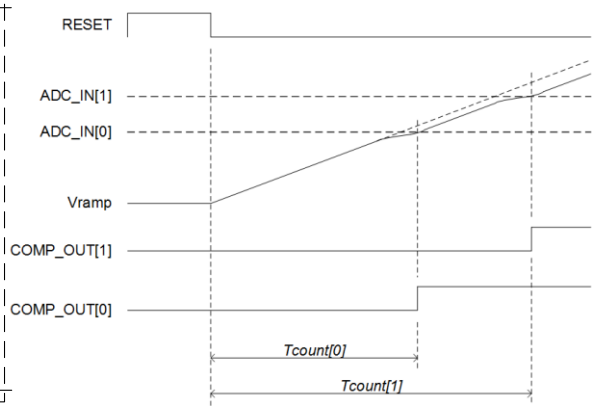

Figure 6 - effect of parasitic C2 capacitance on ramp signal in ramp ADC

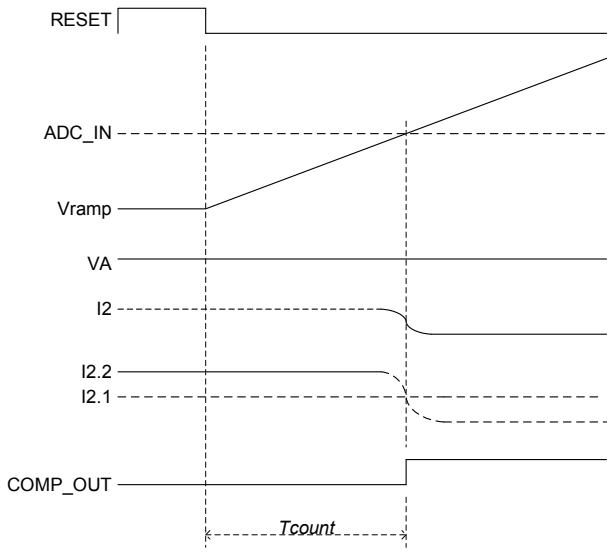

Figure 7 – timing of the comparator and currents in its branches

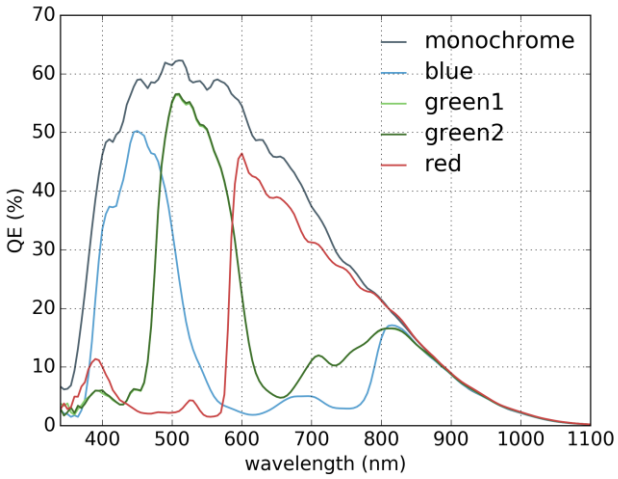

Figure 8 – QE (monochrome and color devices)

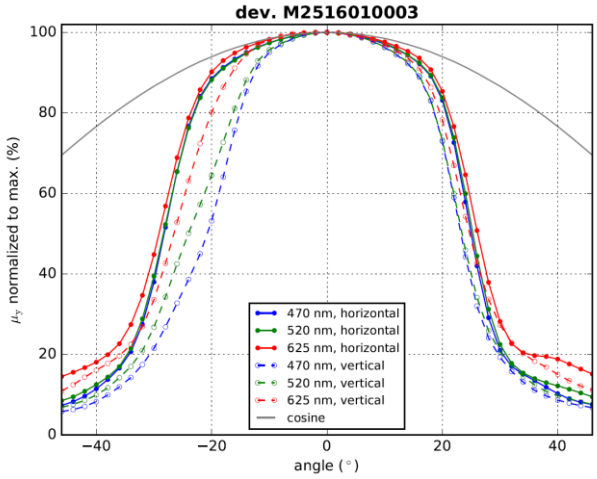

Figure 9 – angular response (monochrome, 3 wavelengths, horizontal & vertical)

Table 1: Overview of key specifications

Parameter	Value
Pixel pitch	4.6 µm
Pixel resolution (effective)	7920 x 6004
Frame rate	30 fps (full resolution) 30 fps (2x2 binned) 60 fps (2:1 subsampled)
A/D Converter	12-bit
Black reference	Optical black columns at left/right side of array. On-chip optical black clamping circuit
Full Well Charge Qsat (150% sat.)	14579e- (full resolution or 2:1 subs.) 57764e- (2x2 binned mode)
Full well charge (Max variance point)	14094 e-(full resolution or 2:1 subs.) 55939 e- (2x2 binned mode)
Temporal Noise | (at gain 1x)	8.8 e- (full resolution or 2:1 subs.) 22.0 e- (2x2 binned)
Dynamic Range (QSat, at gain 1x)	64.5dB (full resolution or 2:1 subs.) 68.5dB (2x2 binned)
Dynamic range (EMVA 1288)	63.8 dB (full resolution or 2:1 subs) 68.1 db (2x2 binned)
Parasitic light sensitivity of storage node (mono device)	470nm: 1 / 19187 520nm: 1 / 17958 625nm: 1 / 8448
MTF @ nyquist (X/Y) mono device	0.66 / 0. 63 @ 554 nm
Dark current signal (typical)	0.21 e-/s @ 20C 63.7 e-/s @ 60C
Fixed Pattern Noise	19.0e- RMS
Lag	0.6 e-
Power Consumption	2.9W
Package	141 PGA
Temperature range	-30…+70 °C
Output	22 data, 1 control & 2 optical black data channels @ 830 Mbps Source synchronous with DDR clock or 8b10 embedded clock Packet-based readout option for more robust data reception

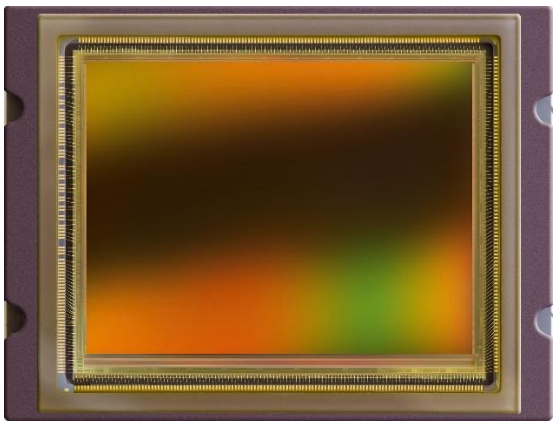

Figure 10 – picture of the chip