Low Dark Current and Low Noise 0.9 μm Pixel in a 45 nm Stacked CMOS Image Sensor Process Technology

Seiji Takahashi, Yi-Min Huang, Jhy-Jyi Sze, Tung-Ting Wu, Fu-Sheng Guo, Wei-Cheng Hsu, Tung-Hsiung Tseng, Chia-Ching Liao, Chin-Chia Kuo, Tzu-Hsiang Chen, Wei-Chieh Chiang, Chun-Hao Chuang, Keng-Yu Chou, Chi-Hsien Chung, Kuo-Yu Chou, Chien-Hsien Tseng, Chuan-Joung Wang and Dun-Nien Yaung

Taiwan Semiconductor Manufacturing Company
No. 8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsinchu, Taiwan, ROC
Tel: +886-3-5636688 ext. 723-5765, e-mail: seijit@tsmc.com

***Abstract*—A 0.9 μm pixel with well-balanced light and dark performance by making full use of a highly manufacturable 45 nm advanced technology incorporated with stacked CMOS image sensor (CIS) is presented. The 45 nm advanced technology is desirable for submicron pixel generation because of tighter design rule and higher controllability for process variation. In addition, the flexibility of stacked CIS process improves pixel performance. In this work, we demonstrated low dark current of 3.2 e/s at 60 °C, ultra-low read noise of 0.90 e rms, a high full well capacity (FWC) of 4,100 e, and blooming free in a 0.9 μm pixel with pixel supply voltage of 2.8 V.**

I. Introduction

Scaling down is an absolutely necessary for demands for high resolution imaging as well as quanta image sensor [1]. Backside illumination technology had been developed and has enabled drastic S/N improvement [2,3]. Stacked CMOS image sensor chips enable more flexible manufacturing process dedicated to image sensor [4]. Furthermore, a 45 nm advanced technology incorporated [5] with stacked CIS is quite promising to boost up light signal, lessen noise, and control process variation caused by critical dimension fluctuation and mask overlay error, which are more serious for submicron pixel generation.

II. A 45 nm Stacked CMOS Image Sensor

The test chip architecture is a 8-mega-pixel (3296(H)x2512(V)) raw data output CIS test vehicle. The block diagram of the vehicle is illustrated in Fig.1. The pixel architecture adopted 2x2 shared 4T without row-select and pixel unit cell size is 0.90 μm. Taking into account overall pixel performance, all pixel devices were placed in CIS wafer, as shown in Fig. 2. The processed CIS wafer was bonded with a logic wafer, followed by backside illumination process including thin down, anti-reflection coating, color filter and microlens array process [6].

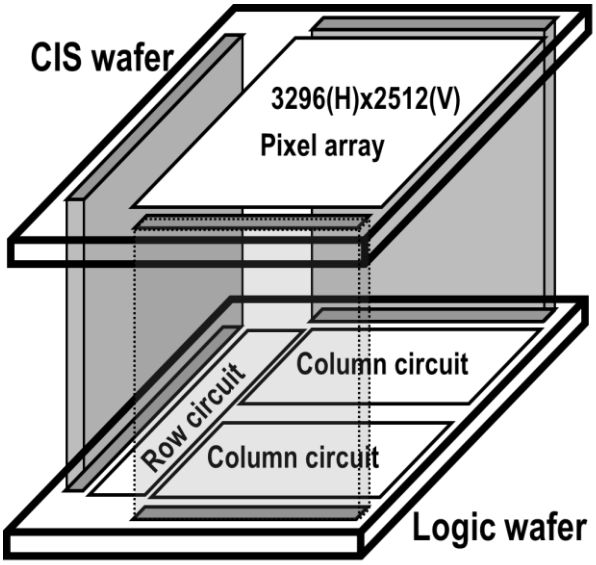

Fig. 1 Block diagram of 45 nm stacked CIS test vehicle.

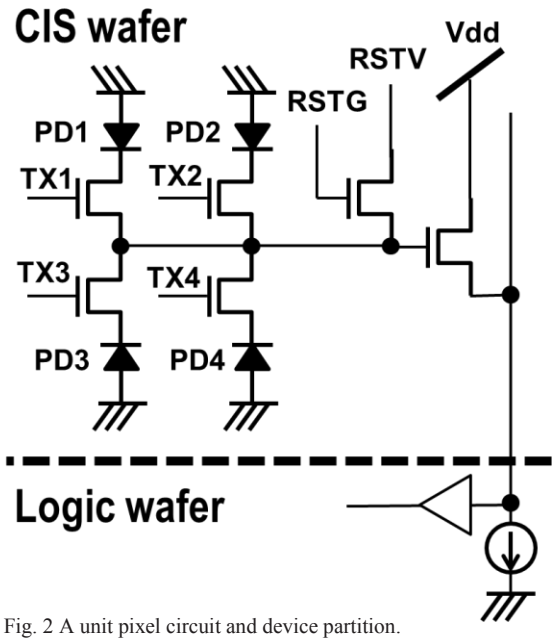

Fig. 2 A unit pixel circuit and device partition.

Lithography capability is a key process element in this submicron pixel development. A 193 nm ArF immersion lithography is used for critical layers so that fill factor of 0.90 μm pixel increased by 20% with respect to 65 nm technology. With the tighten design rule, source follower device gate area can be maximized in a given small area in order to decrease random noise and random telegraph signal [7]. The scaling of gate oxide thickness is also effective for random noise reduction [8]. In addition to these, related processes were fully optimized, for instance, minimizing etching damage, eliminating dangling bonds, and device channel engineering [9]. As a result, one of key performance index, read noise was reduced to 0.90 e rms at analog gain of 18 dB, as shown in Fig. 3.

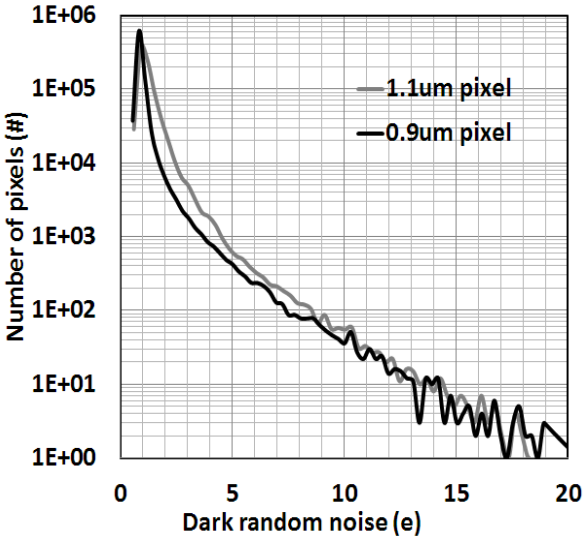

Fig. 3 Statistical read noise distributions of 0.9 μm pixel and 1.1 μm pixel at analog gain of 18 dB.

III. Pixel Design

Another process integration challenge in the submicron pixel is dark current reduction. Unlike logic transistors, image sensor basically follows constant voltage scaling law [10], as pixel size shrinks, thus necessary doping concentration is increasing as shown in Fig. 4. It is well known that transfer gate edge is a main source of dark current and white pixels [11]. Reducing floating diffusion node bias is effective to reduce dark current because of electric field relaxation. However, this degrades anti-blooming due to lower overflow potential [12,13]. Therefore, a new pixel structure was developed.

An additional N- type layer was interposed between a shallow photodiode (PD) and a deep photodiode, which also extends to floating diffusion region (Fig. 5). It is evident from 3D TCAD device simulation results that anti-blooming path was clearly made. Besides, this layer is adequate to improve image lag, as shown in Fig. 6. Thanks to the larger image lag margin, a pinning voltage (Vpin) can be decreased while keeping the same full well capacity. Lower Vpin is also helpful to reduce dark current.

Furthermore, key process conditions such as ion implantation and annealing steps were carefully optimized to minimize every kind of defects and recover damages.

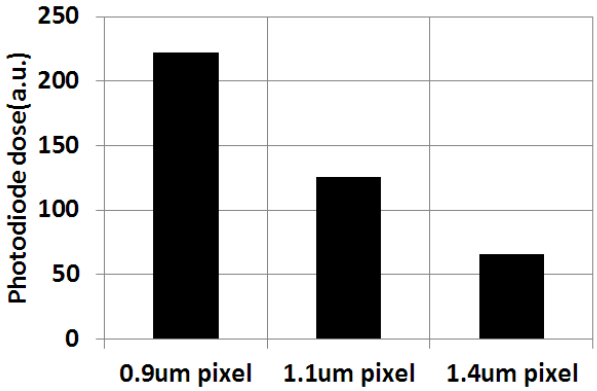

Fig. 4 Pixel generation vs. photodiode implant dose.

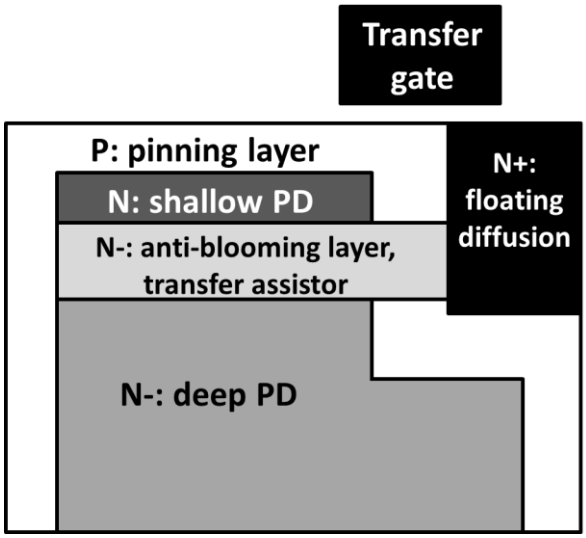

Fig. 5 Schematic drawing of pixel design concept.

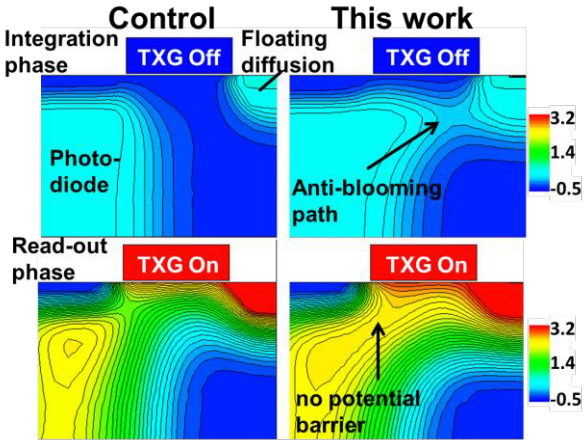

Fig. 6 3D TCAD simulations of the transfer device structure showing electrostatic potential contours.

IV. Experimental Result

A histogram of the individual pixel dark current at 60 ℃ is shown in Fig. 7. The dark current peak at 60 ℃ corresponds to 3.2 e/s for 0.9 μm pixel, and the dark current distribution of 0.9 μm pixel is close to that of 1.1 μm pixel in spite of higher photodiode dose.

Fig. 8 shows light response curve of 0.9 μm pixel. Even after green channel signal saturates, adjacent channel, red and blue signal, don't distort. From this fact we can conclude blooming is 0% [14].

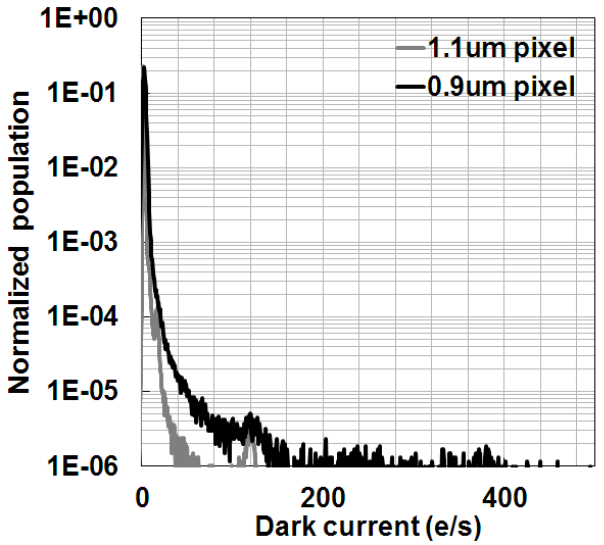

Fig. 7 Dark current histograms at 60 °C of 0.9 μm pixel and 1.1 μm pixel.

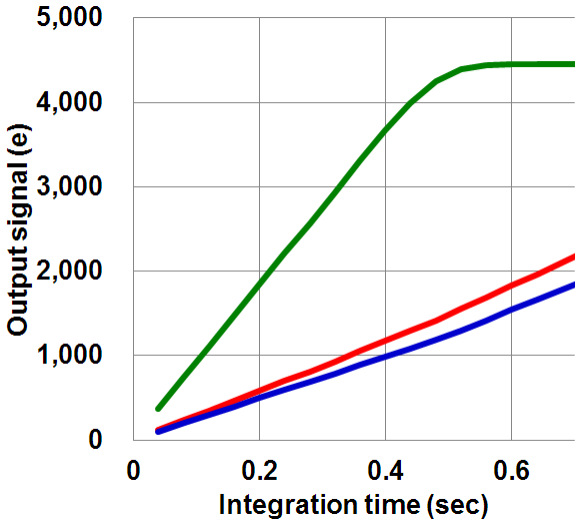

Fig. 8 Light response curve of 0.9 μm pixel.

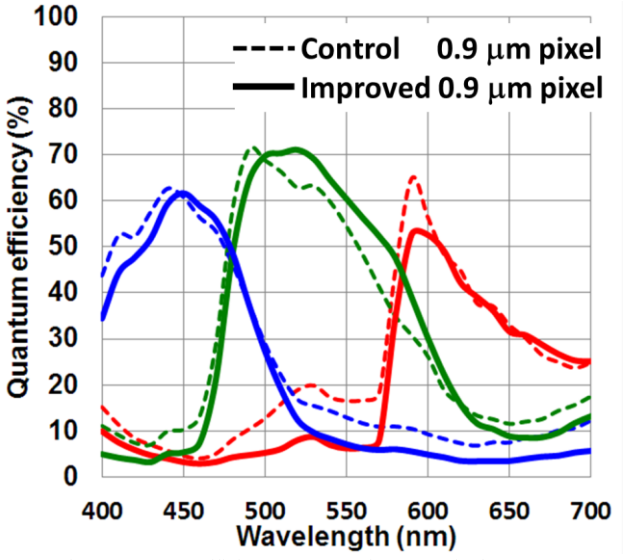

Fig. 9 Quantum efficiency spectra of 0.9 μm pixel.

Optical crosstalk improvement is mandatory in submicron small pixel [15]. We then developed optical stack thinning and cross talk suppression techniques. Optical stack height defined by the distance between backside silicon surface and top of micro lens was decreased by 10%. A deep trench isolation technology was developed to suppress optical crosstalk without scarifying dark performance in parallel. Besides, new color filter material was used to improve SNR10 index. Obtained quantum efficiency spectra of 0.9 μm pixel is shown in Fig. 9, in which crosstalk was greatly suppressed. A sample color image taken with 0.9 μm pixel in the 45 nm stacked CIS process technology is shown in Fig. 10.

Fig. 10 A sample color image taken with 0.9 μm pixel manufactured in the 45 nm stacked CIS.

V. Conclusion

A novel 0.9 μm pixel with well-balanced light and dark performance by making full use of a highly manufacturable 45 nm advanced technology incorporated with stacked CIS is presented. Table 1 gives a summary of the pixel performance. Low dark current of 3.2 e/s at 60 °C, ultra-low read noise of 0.90 e rms, high FWC of 4,100 e, and blooming free are demonstrated in a 0.9 μm pixel with pixel supply voltage of 2.8 V. This technology offers high resolution, superior low light imaging, and small chip size features in image sensors.

TABLE I
Sensor Characteristics

Process technology	45 nm 1P4M stacked CIS
Pixel size	0.90 μm
Pixel supply voltage	2.8 V
Conversion gain	120 μV/e
Dark current at 60 °C	3.2 e/s
White pixel counts with dark current of >200 e/s at 60 °C	679 ppm
Read noise at 18 dB	0.90 e rms
Full well capacity	4,100 e
Blooming	0%
Image lag	<1 e
Photo response non-uniformity	0.9%
Quantum efficiency at green peak	71%

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