ON Semiconductor®

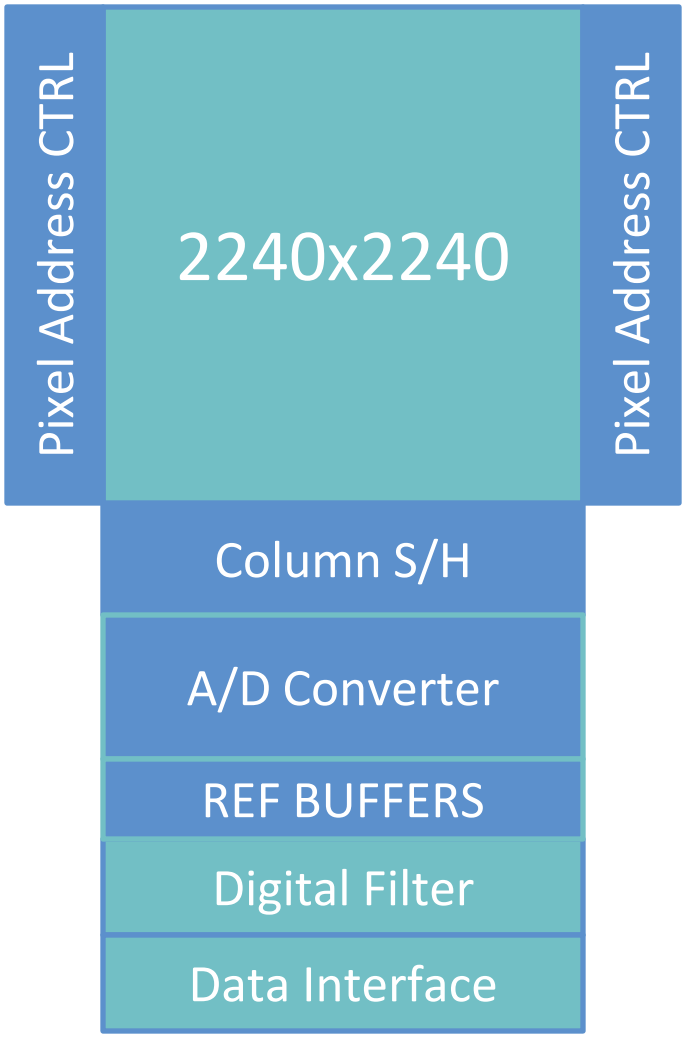
A 5 Megapixel, 1000 fps CMOS Image Sensor with High Dynamic Range and 14 bit A/D Converters

Bart Cremers

IISW 2013

Overview of Sensor Specifications

- 5 Megapixel Image Sensor
  - 1000fps @ full resolution
  - 2000fps HDTV format
  - Rolling & Global Shutter
  - 14-bit A/D converters
  - 5e- noise, 20ke- FWC
  - Patterns <1/3rd of noise floor
  - Clean RAW image
- 70 LVDS channels @ 1Gbps
- >2.5Million ASIC gates

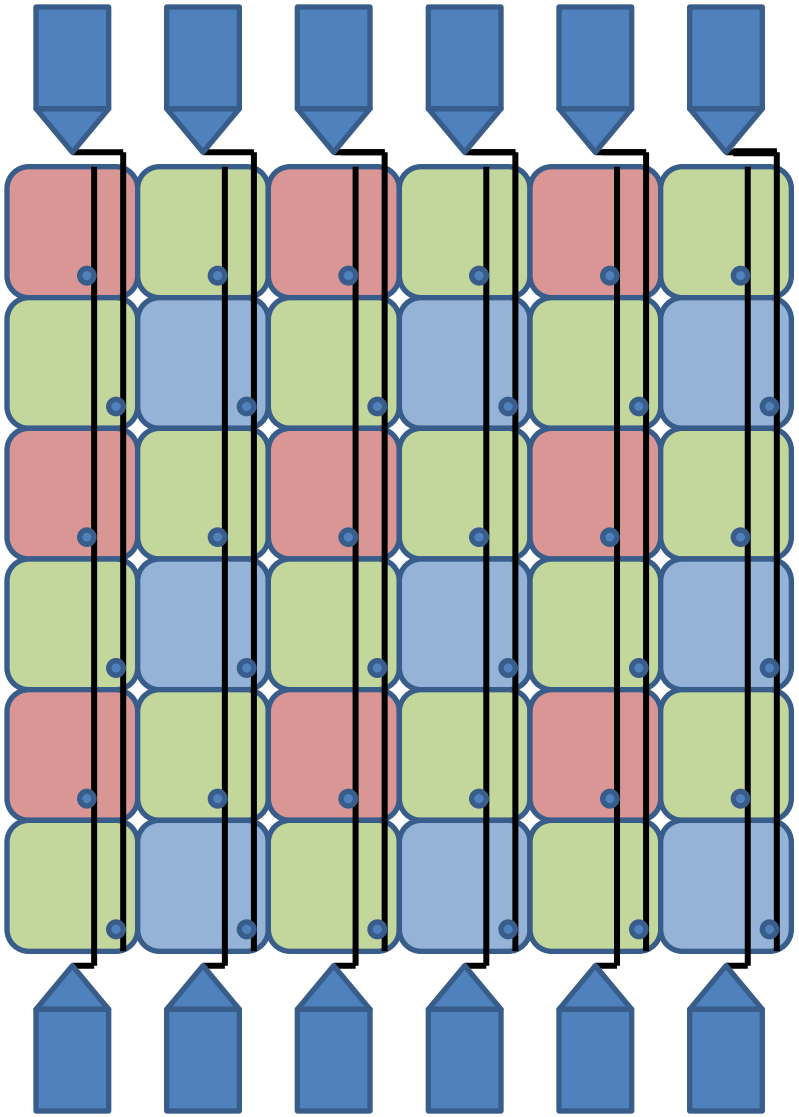


Challenges in this Work

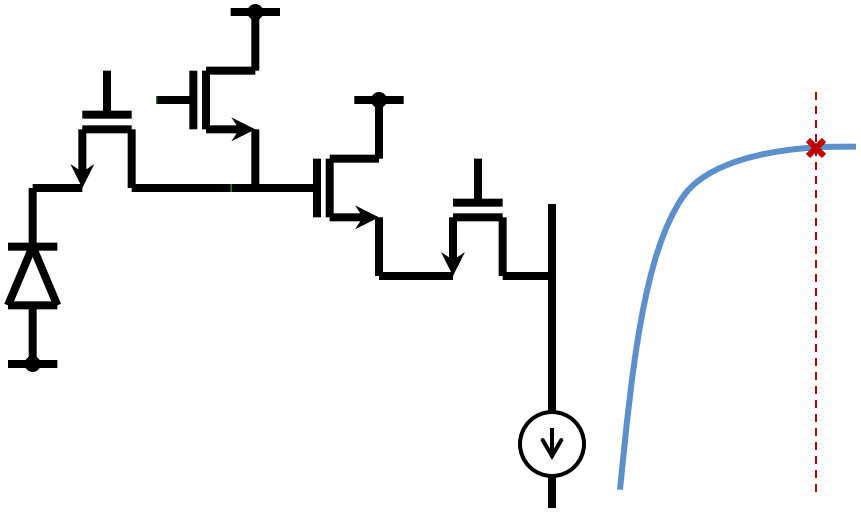
- High Speed Pixel Readout
- High Speed 14-bit A/D Conversion
- Drift Free raw image, no calibration, no scene dependent artifacts
- *High speed Interface and Packaging*

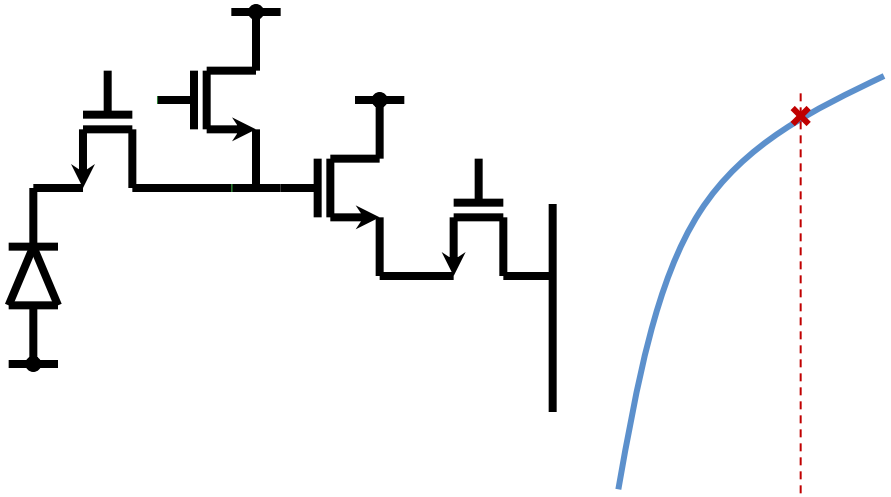
Pixel Readout Scheme

- 2 lines read in parallel
- Electrical crosstalk == color crosstalk !
- Column will not settle to 14-bit accuracy
- Successful column memory removal is critical



Column Settling





Source Follower loaded by current source.

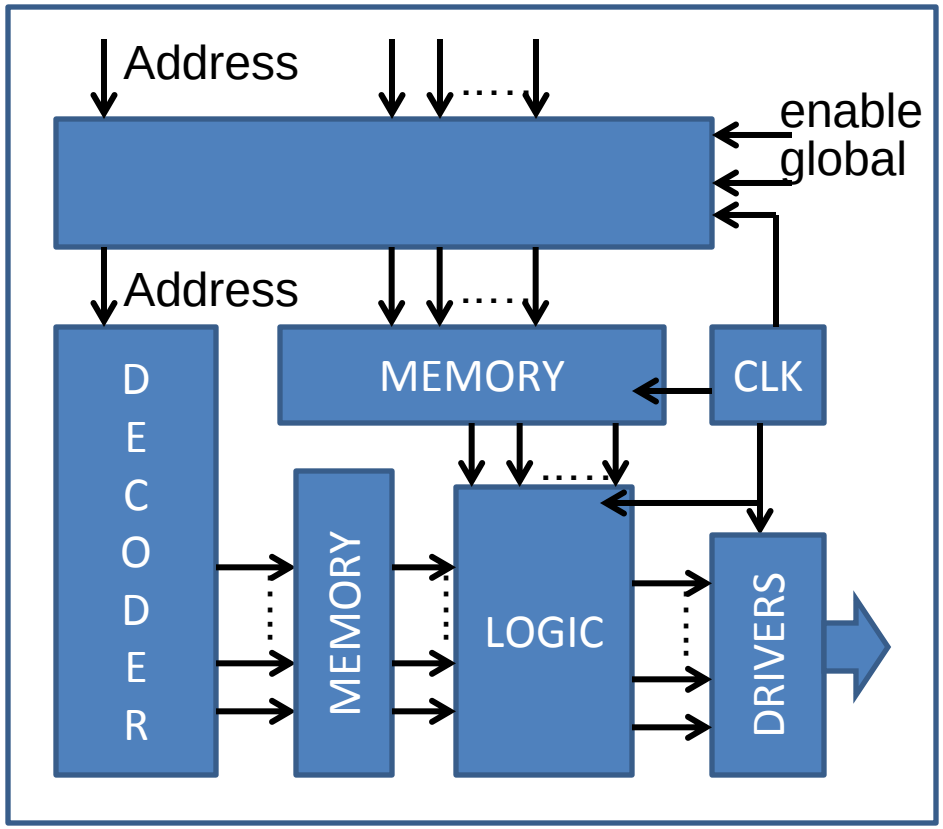
Settles to desired accuracy.

No current load. Sample SF output during settling.

- More SF gain ➔ Lower Noise
- Lower intrinsic SF noise
- More swing
- One less source of FPN/PRNU

Flexible Addressing

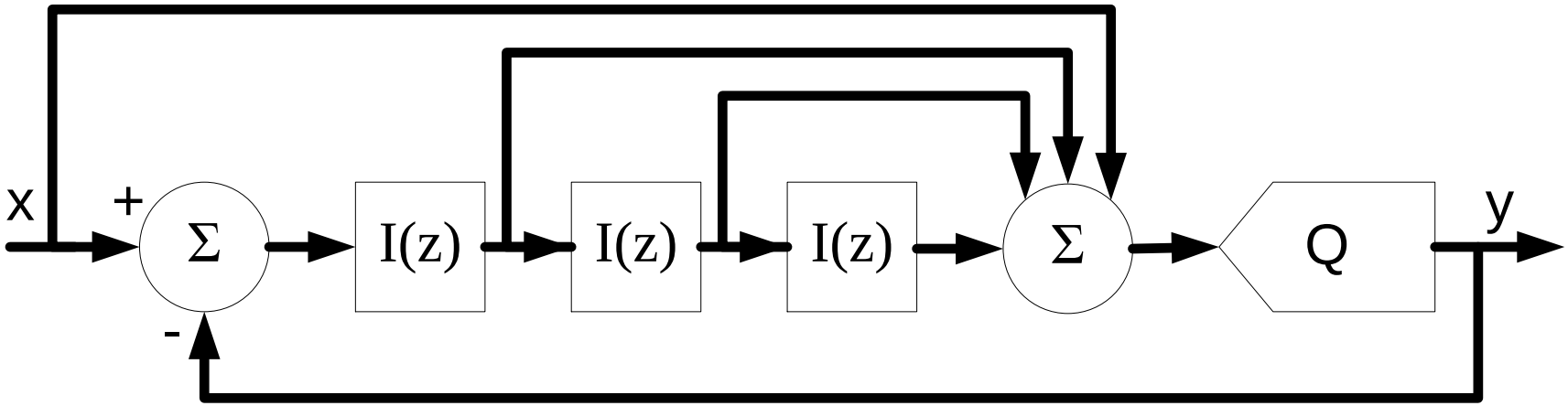
- Directly addressable pixel array
- Line-based memory
- Allows random scheduling of row based operations
- Supports both pointer-based as well as global operations



ADC architecture

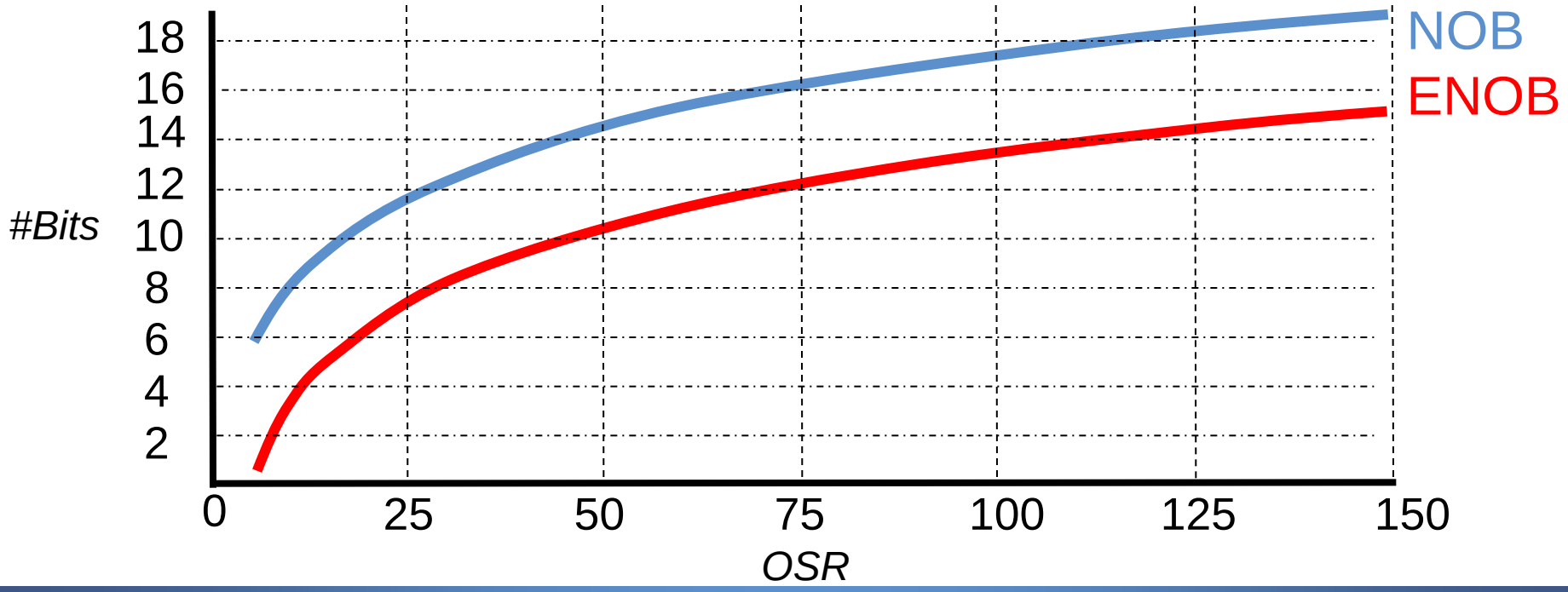
- 3rd Order CIFF Delta Sigma Modulator
  - Single bit quantizer
  - Excellent loop stability
  - Shared reference voltage for all modulators
  - Uniform power consumption over the entire line time for any signal value

Intrinsically gain matched
Calibration-free



ADC architecture

- Scales very well for high speed – high resolution combinations
- Changing OSR allows trade-off @ run-time :
  - noise & resolution vs frame rate
  - noise & resolution vs power



ADC architecture

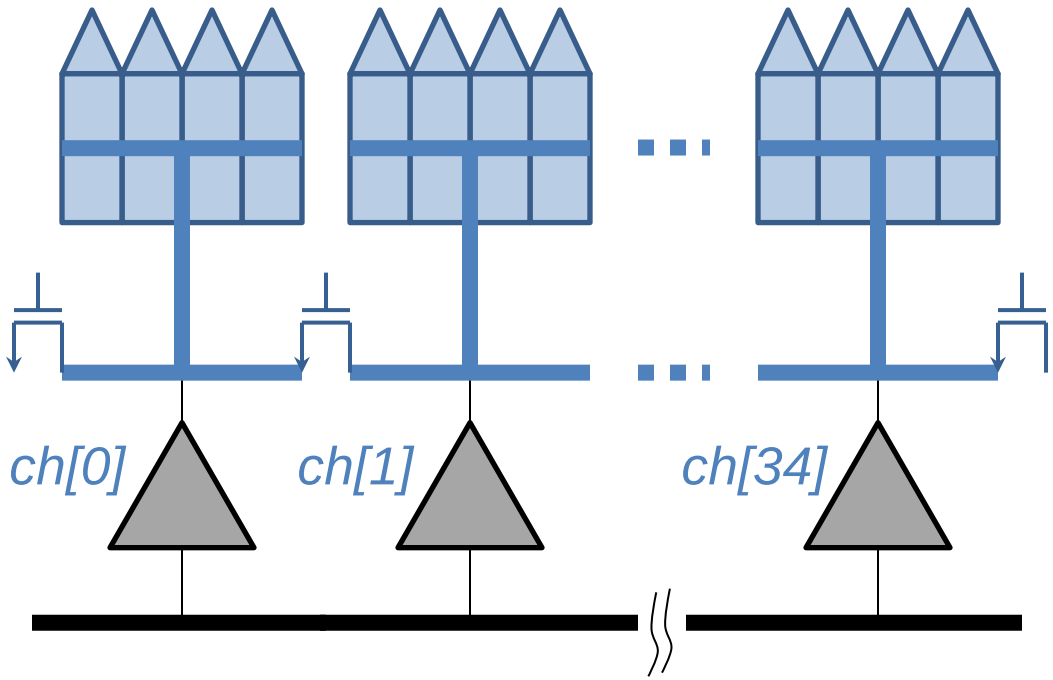
- Trade-off : artifact-free operation vs power & noise

	Digital CDS	Analog CDS
Temporal Noise	<5e-	<4e-
Column-wise offset & gain differences	< 0.3x noise floor	10x noise floor
Power	8 W	4 W
	DSM – 30% References – 40% Filter – 20%, Clock – 10%	

- Focus for future work
  - Reduce power consumption in Filter and References
  - Reduce artifacts in analog CDS mode

Reference Voltage Uniformity

- Differences lead to Column FPN and PRNU
- Large distance (>1cm) requires distributed buffering
- Outputs of buffers are shorted
- Add switches for windowed read-out and low-power modes



Key Specifications

Parameter	Value	Comment
Technology	0.18um CIS	
Resolution	2240 x 2240	
Frame Rate	1000 fps	Rolling Shutter
Temporal Noise	5 e-	
FWC	20 ke-	
DR	72 dB	Intra-Scene
Peak QE	> 50 %	@ 633 nm
MTF	63 %	@ 633 nm, @ nyquist freq.
Power consumption	10 W	Main supply voltage 1.8 / 3.3 V
ADC resolution	14 bit	#4480 ADCs in column parallel architecture
Total Data Rate	70 Gbps	70 LVDS channels @ 1Gbps

Thank You