

## Early Research Progress on Quanta Image Sensors

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### End to End System Simulation

#### Input Image 256x256 8b



#### → 4096x4096 1b x 16 fields = 268 Mb



# $H = \frac{S_H h_o}{255}$

#### Output Image 1024x1024 8b



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in this example 1 pixel =  $\Sigma$  4x4x16 jots  $SNR \le \sqrt{256}$ 





### Convolution



20

10

0 0

#### 2D Examples:

Binary valued filter

Binaryweighted filter

-3-

10

40



Down

sample





### Digital Film Sensor Algorithm





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### Readout Signal Chain Strawman Design

#### General requirements:

- Need to scan 0.1-10 Gjots at 100-1000 fields per sec
- 8k 80k jots per column  $\rightarrow 0.8 80M$  jots/sec

#### Assumptions:

- 0.1 Gjot at 100 fps  $\rightarrow$  1Mjot/sec
- 1 mV/e- conversion gain
- 150 uV rms noise on column bus (0.15 e- rms)
- 0.18 um process
- Vdd = 1.8V



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### **Readout Signal Chain**



column bus



Process	V <sub>DD</sub>	Jot array	Column Speed	Column power	Comp power	Total	Array Power
CURRENT DESIGN							
0.18um	1.8V	0.001 Gjots (1k X 1k)	1MJ/s (1000fps)	0.71uW	1.28uW	1.99uW	1.99mW
0.18um	1.8V	0.1 Gjots (10k X 10k)	1MJ/s (100fps)	6.44uW	1.28uW	7.72uW	77.2mW
SCALED DESIGN							
0.18um	1.8V	0.1 Gjots (10k X 10k)	10MJ/s (1000fps)	64.4uW	12.8uW	77.2uW	772mW
45nm	1.1V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	57uW	2.9uW	59.9uW	2.5W
22nm	0.8V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	20uW	0.74uW	20.74uW	0.87W
45nm	1.1V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	553uW	9uW	562uW	75W
22nm	0.8V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	197uW	2.3uW	199.3uW	26.5W

Adapted from Kotani et al. 1998

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Process

0.18um

VDD

1.8V

Jot array

0.001 Gjots

### **Readout Signal Chain**

Column

power

0.71uW

CURRENT DESIGN

Comp

power

1.28uW

Total

1.99uW

7.72uW

77.2uW

59.9uW

20.74uW

562uW

199.3uW

Column

Speed

1MJ/s



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Array

Power

1.99mW

77.2mW

772mW

2.5W

0.87W

75W

26.5W





### **Jot Device Considerations**

#### General requirements:

- 200 nm device in 22 nm process node ("10L")
- High conversion gain > 1 mV/e- (per photoelectron)
- Small storage well capacity ~1-100 e-
- Complete reset for low noise
- Low active pixel transistor noise <150 uV rms
- Low dark current ~ 1 e-/s
- Not too difficult to fabricate in CIS line

#### For early investigation

- Cobbled together an imaginary 85 nm process
- Students learning to use TCAD tools etc.
- Anticipate that device principles can be migrated to real process





### **Bipolar Jot Concept**



- CMOS APS but use pinning layer as emitter, storage well as base
- Complete reset of base using "TG"
- Emitter follower to reduce base-emitter cap





### BSI CMOS APS Jot with Storage under Transfer Gate



- Low capacity storage gate makes barrier easier to overcome with low TG voltage
- Minimum FD size to increase conversion gain

Storage under transfer gate first proposed in Back Illuminated Vertically Pinned Photodiode with in Depth

-10- Charge Storage, by J. Michelot, et al., 2011 IISW

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### Summary

- Early progress made on realizing Quanta Image Sensor
- >1 year support of Rambus (thanks Rambus!)
- Students up to speed and making headway
- Challenges don't look as challenging
- Lots of work to do!