A Fully Depleted Backside Illuminated CMOS Imager with VGA Resolution and 15 Micron Pixel Pitch

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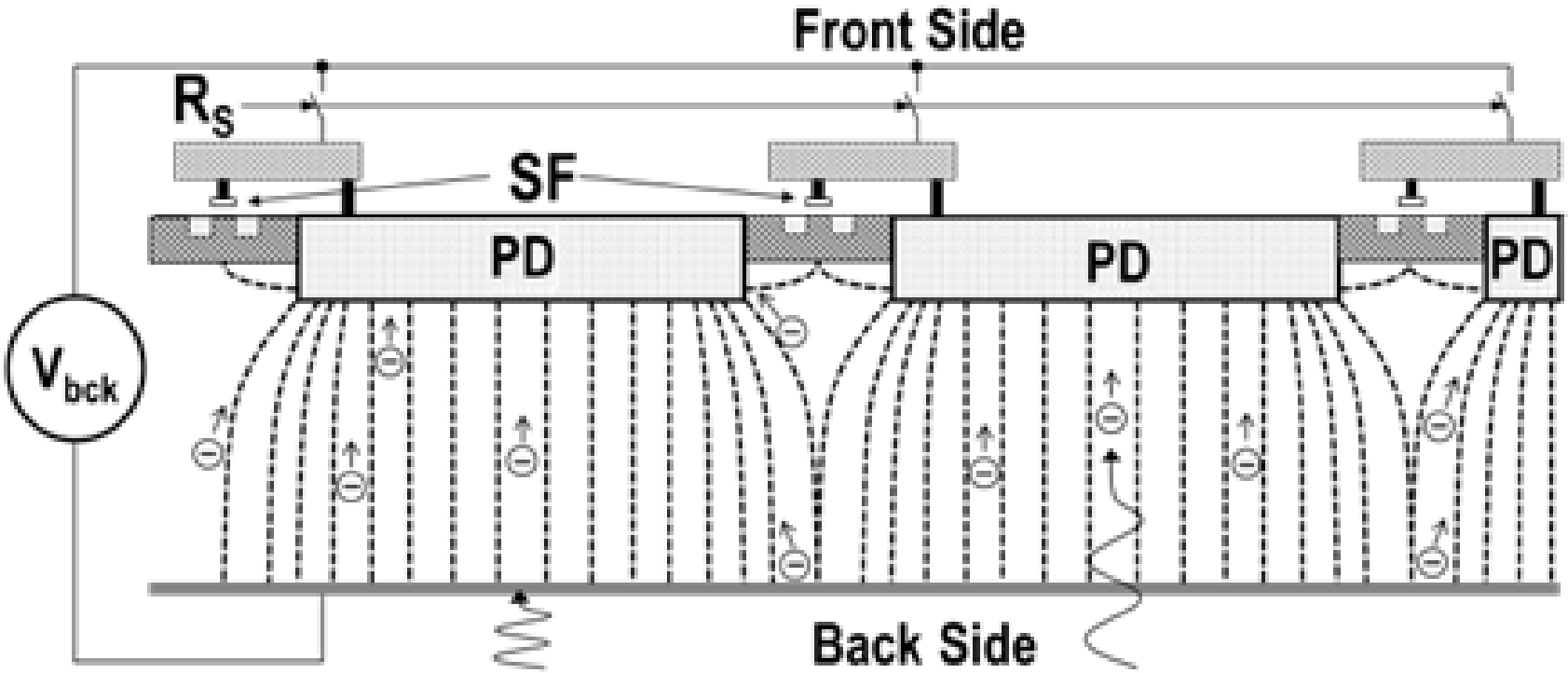
2013 International Image Sensor Workshop (IISW)
June 12 – 16, 2013

Highlights of Fully Depleted (FD) BSI Imager

- **High Sensitivity with 100% fill factor**
  - Peak QE: > 90%
  - QE at 300nm: > 30%
  - QE at 1050nm: > 25% (200micron thick silicon)
- **PIN photodiode**
  - High Speed (3dB bandwidth > 1GHz)
  - Low Noise (<10e^-)
- **2x2 Charge Domain Binning**
  - Frame rate and SNR increase by factor 4
- **Frame rate: 30Hz, 60Hz, 240Hz, 1000Hz**
- **Row programmable full well capacity: 500ke^-, 60ke^-, 10ke^-**
- **Snapshot shutter: ITR, IWR, HDR, NDR**
- **Programmable number of output ports: 1, 2, 4, 8**

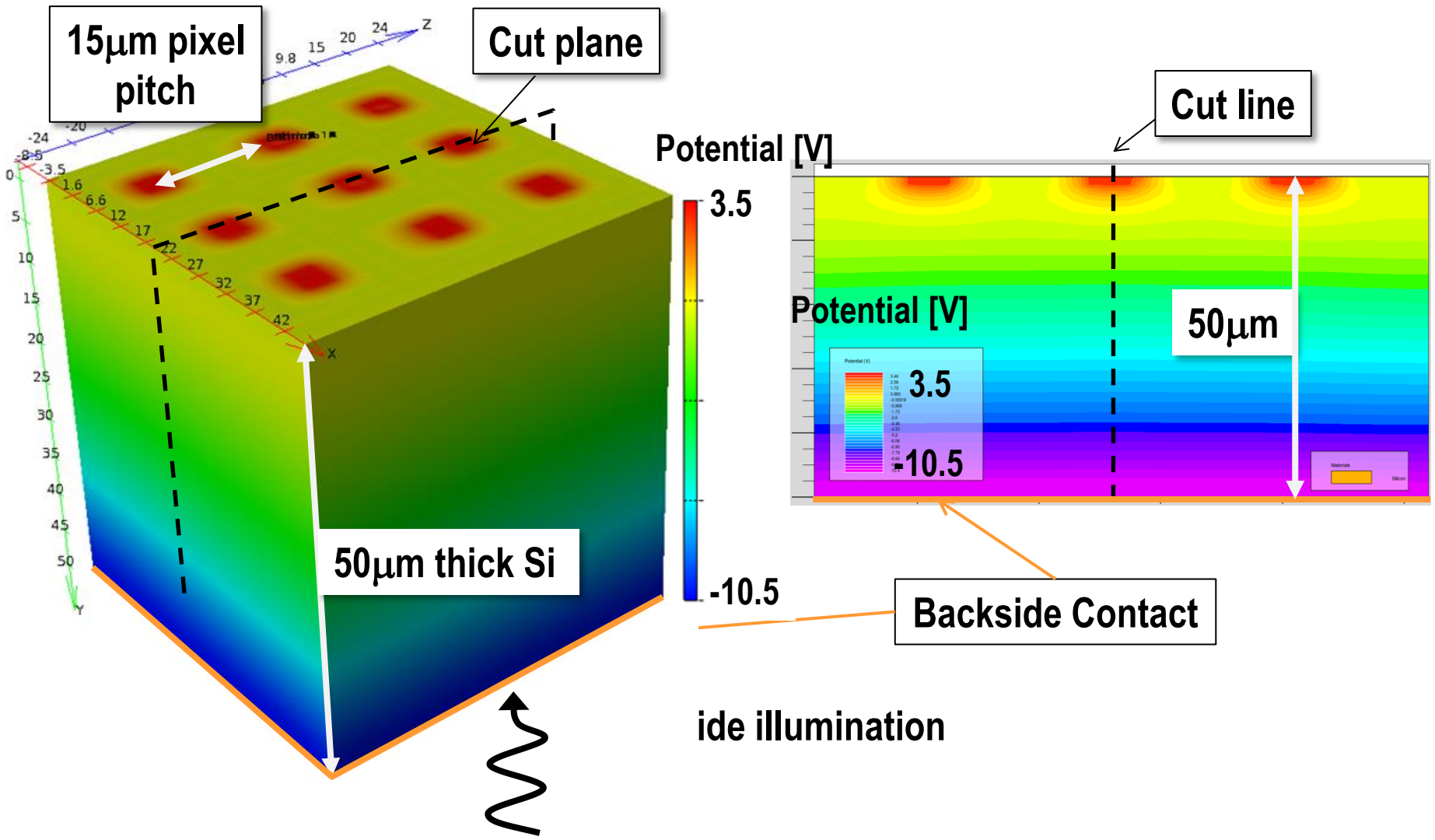
Performance Spectrum Unachieved by any other Monolithic Imager Technology

Cross Section of Fully Depleted CMOS Technology



Charge Collection Region Defined by Lateral and Vertical Depletion

3D Simulation of FD CMOS Pixel on 6.5 kΩ x cm Si



3D Device Simulations were Used to Optimize Pixel Structure

Potential Distribution Throughout Detector

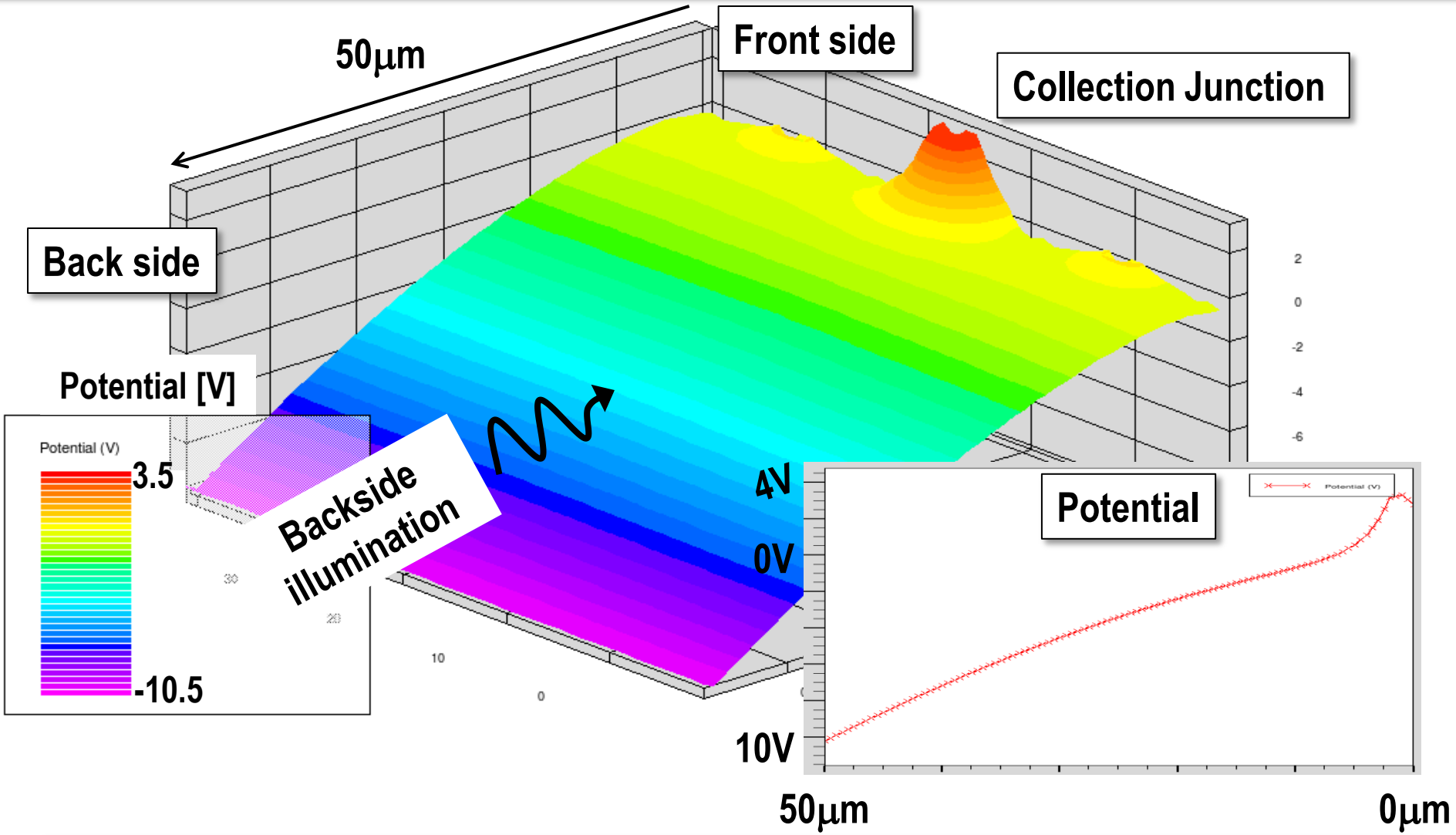
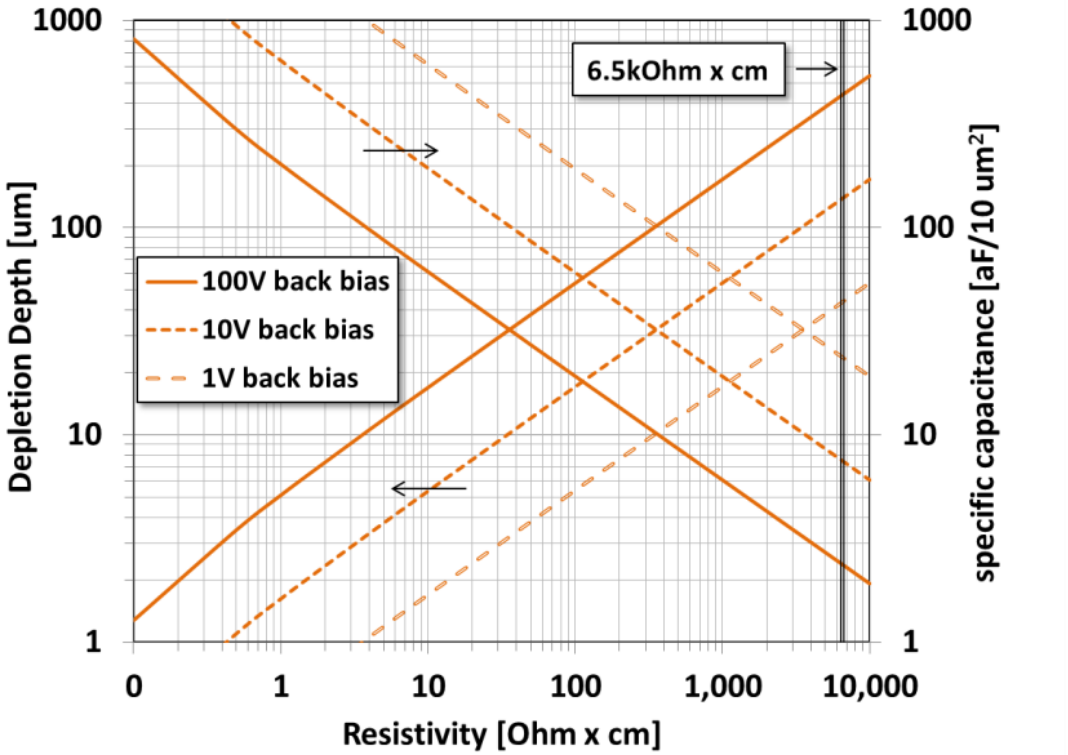


Photo Generated Charge Carriers are Gathered by Fast Drift Process (instead of slow diffusion) in Front Side Collection Junction

Estimate of Depletion Layer Versus Si Resistivity

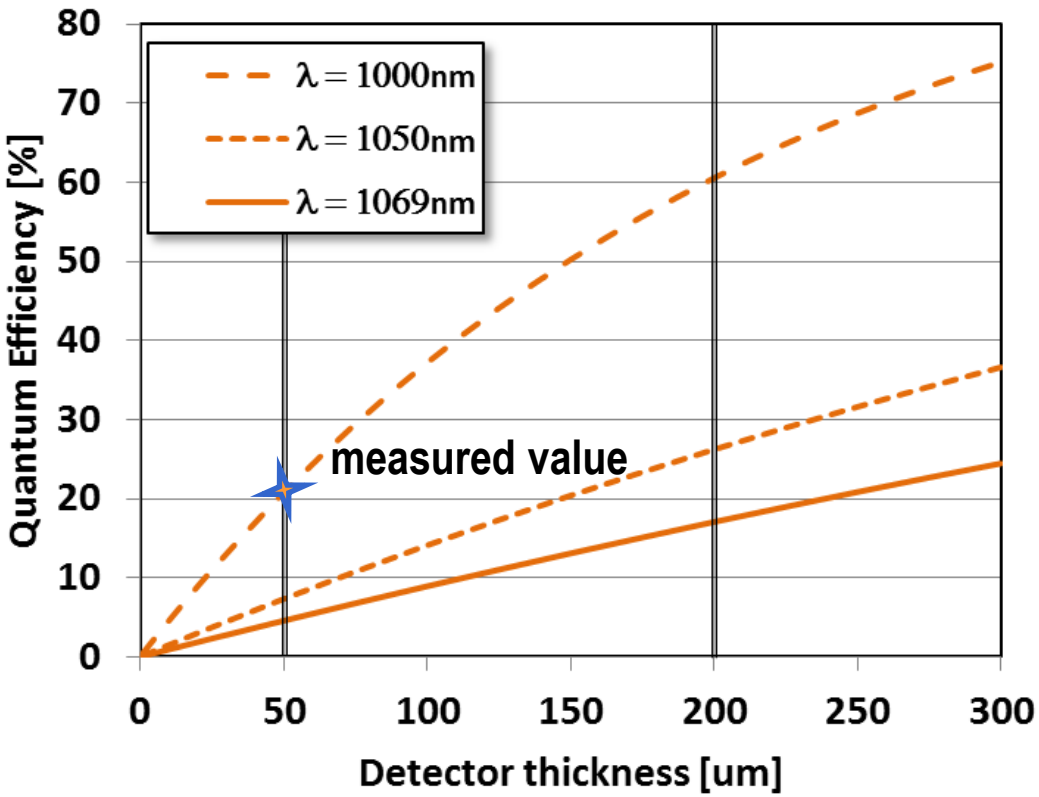


For best performance a backside bias must be applied

Our 6.5 kOhm x cm material can be depleted to a thickness > 400um when applying a backside bias of 100V

High Resistivity Silicon Must be Used to Achieve Deep Depletion

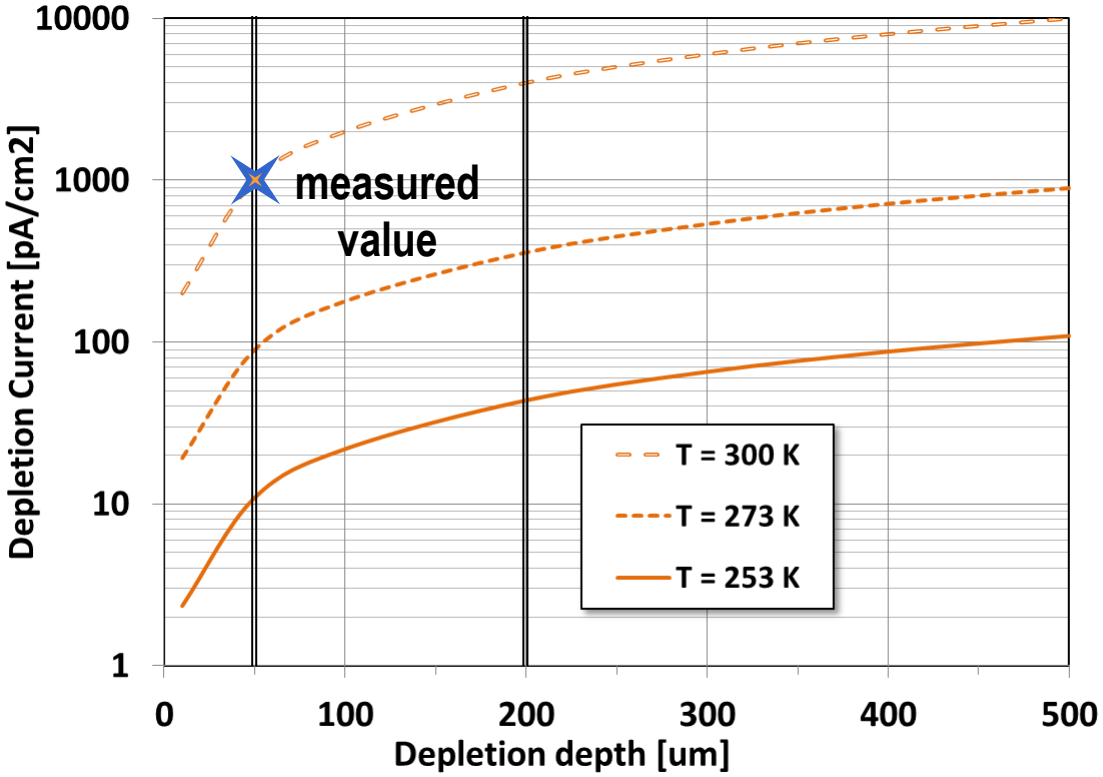
Estimated NIR QE Versus Detector Thickness



➡ At 200um detector thickness the achievable quantum efficiency for λ=1050nm is >25%

Monolithic CMOS Sensor with NIR QE Comparable to Scientific CCDs

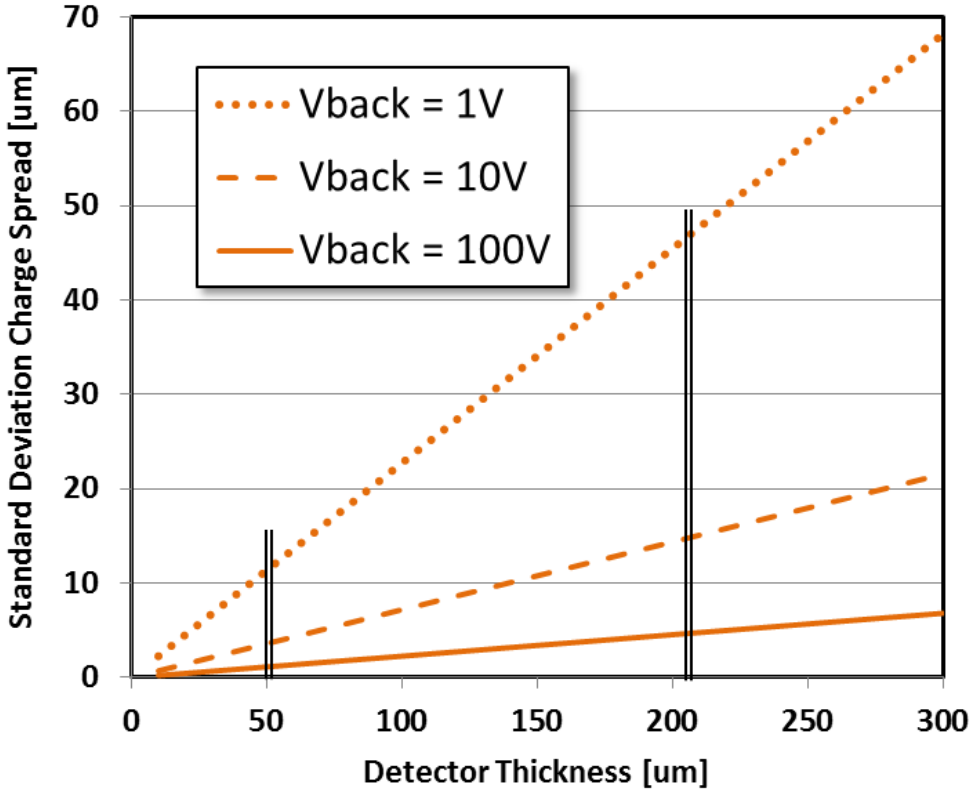
Predicted Depletion Current of thick FD PIN Diode



At T= 300K and a depletion depth of 200um (corresponding to a backside bias of 20V for 6.5kOhm x cm Si), the dark current limit is 4nA/cm^2

Dark Current is Dominated by Depletion – Not Diffusion – Current

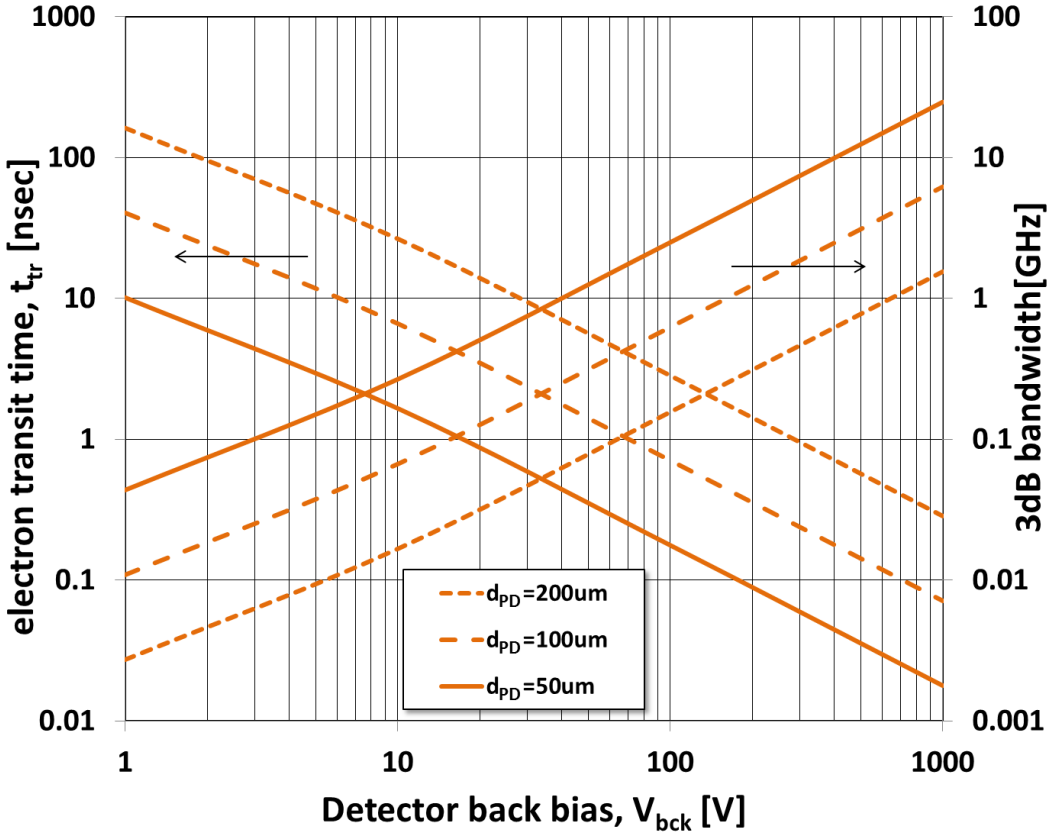
Predicted Charge Spread Versus Detector Thickness



For a 200um thick FD CMOS imager with 100V backside bias, photo generated charge carriers can spread up to 4.5 um before reaching the front side collection junction

MTF Performance Limited Pixel Pitch of FD imager: < 4.5um

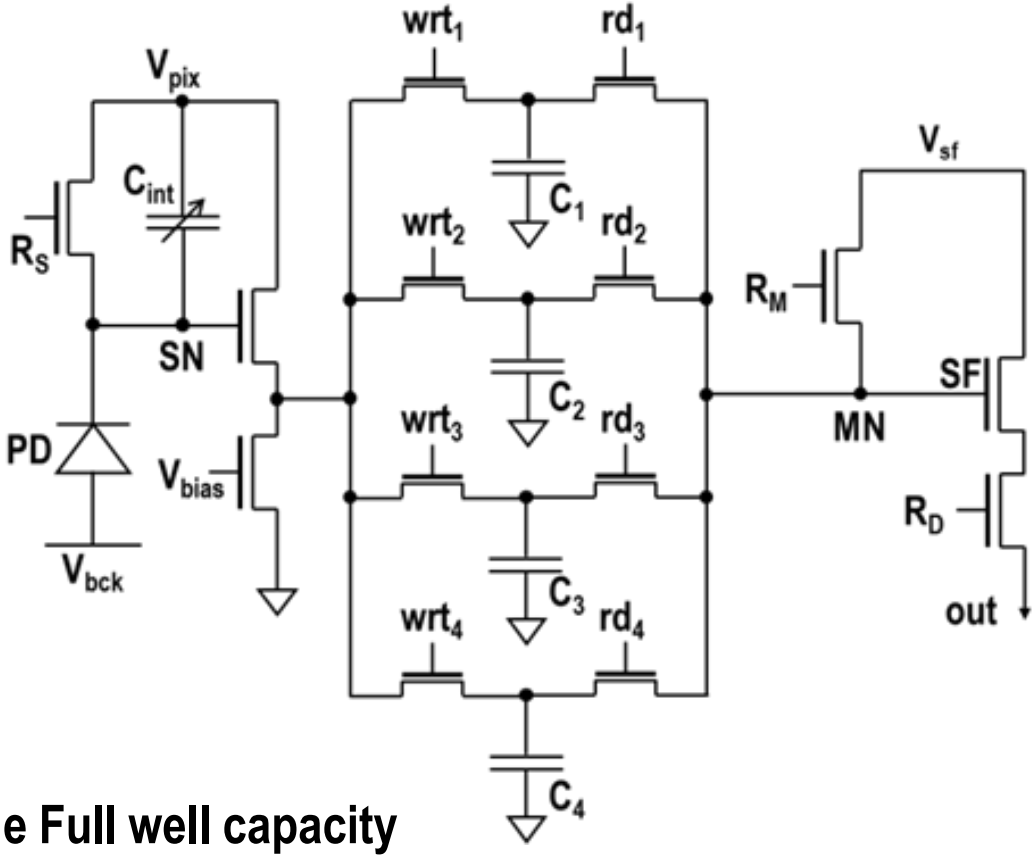
Predicted FD PIN Diode Response Time



Transit time of photo generated charge carriers in 100um FD CMOS imager with 100V backside bias < 1nsec, corresponding to a 3dB bandwidth > 1GHz

Fully Depleted Imager is Suited to Support Nanosecond Integration Time Windows

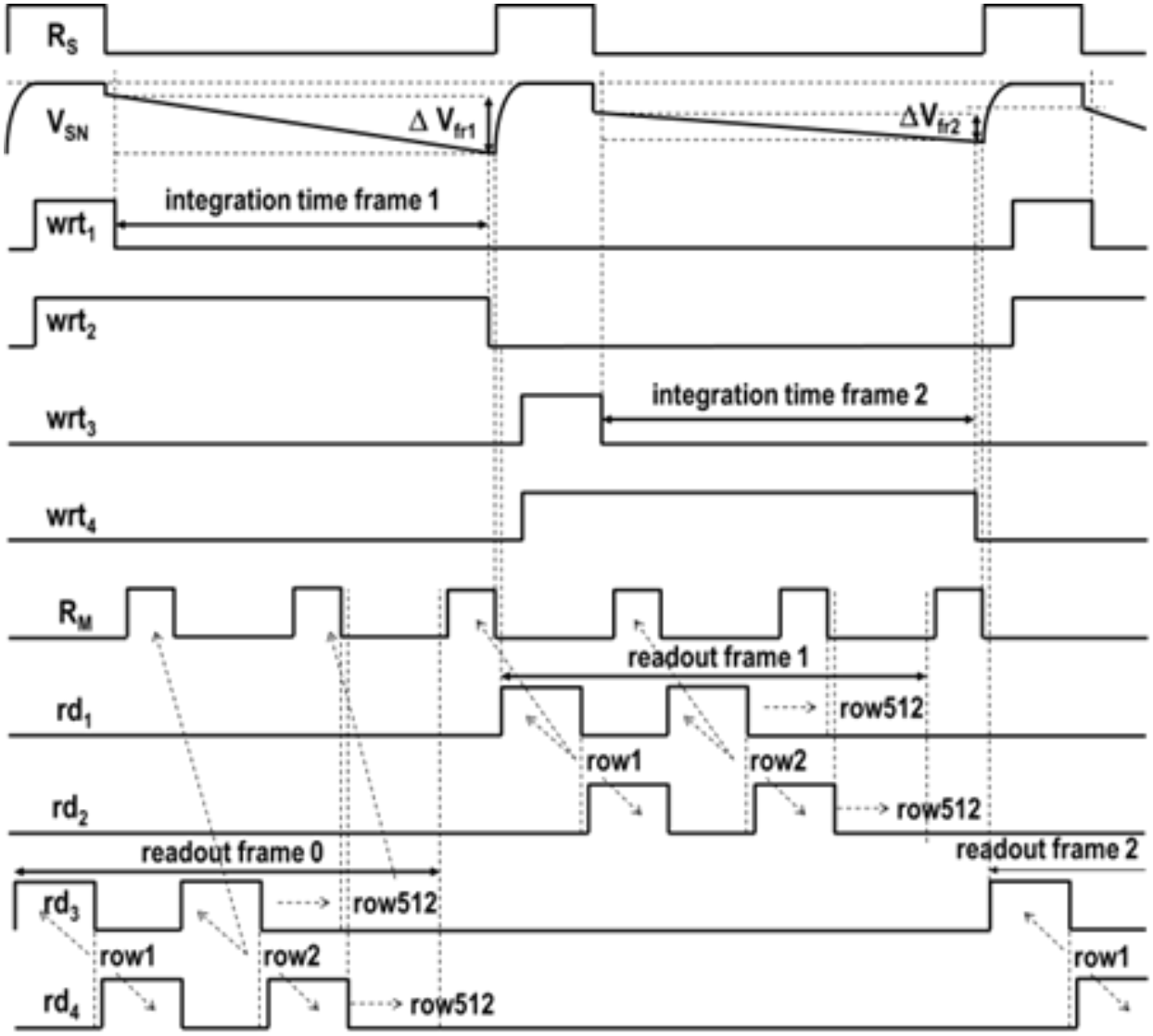
Pixel Schematic



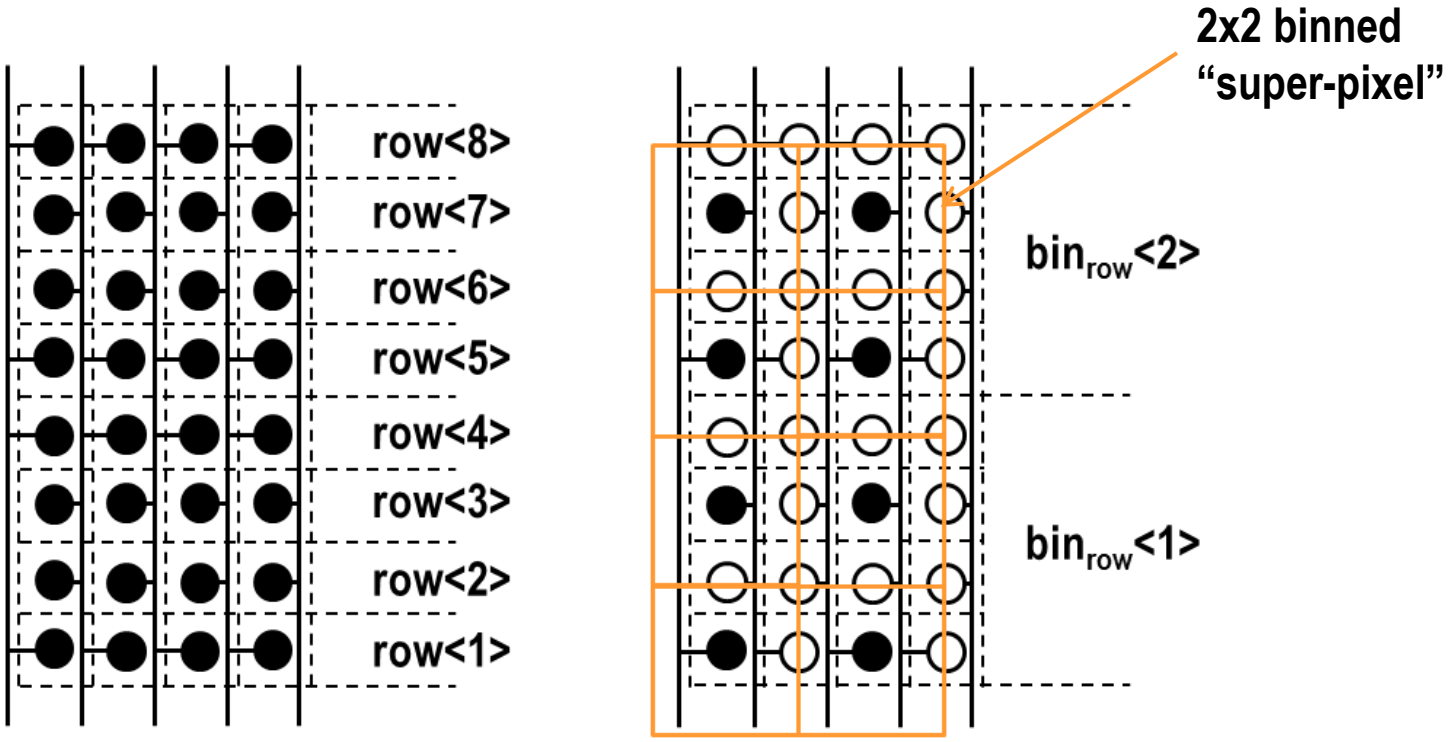
- Programmable Full well capacity
- Integrate while Read (IWR) snapshot shutter
- Correlated Double Sampling readout with IWR snapshot shutter functionality

Pixel Schematic Supports Low Noise Readout for < 100 nsec Integration Time Windows

Pixel Timing



2x2 Charge Domain Binning

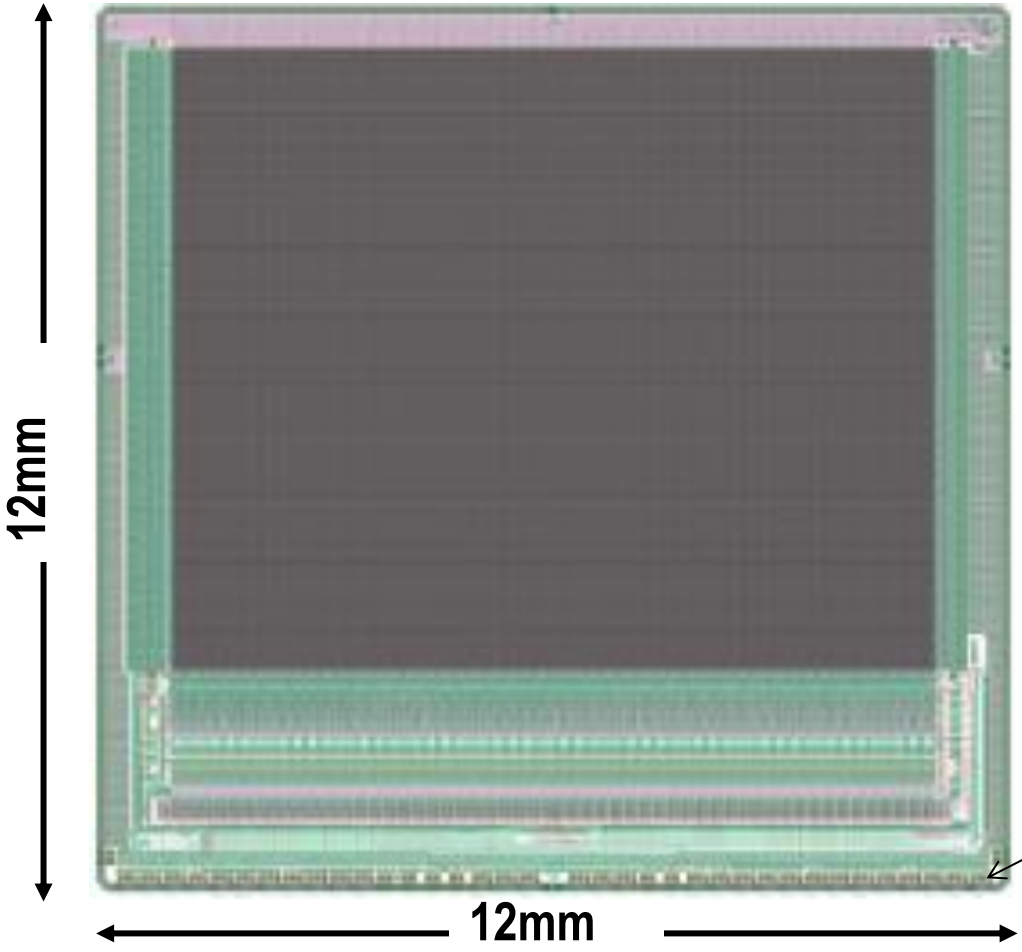


- Potential well of charge collecting junction is turned off in skipped pixels (white circles)

SNR Increase in Readout Noise Limited Domain: 4x → Same as CCDs

Frame Rate Increase: 4x → 2x Faster than CCDs

Predicted Sensor Performance of FD-CMOS Sensor



Size and Layout of Fully Depleted VGA Sensor Comparable to Standard CMOS Imagers

Summary of Specifications

Parameter	Value
Array Format	640x512
Pixel Size	15um
Die Size	12 x 12 mm^2
Frame rate	30Hz, 60Hz, 240Hz, 1000Hz
Pixel Rate	5 MHz, 5MHz, 20MHz, 41 MHz
Number outputs	1,2,4,8
Shutter type	global shutter
Integration modes	ITR, IWR, HDR, NDR
Exposure time	100nsec to 30 msec
Charge capacity	500ke, 60ke, 10ke
Minimum Noise	< $10e^-$
QE at 1050nm	> 25% for 200nm thick Si
Binning	2x2, 1x2, 2x1
Output type	analog
Power	60 mW @ 60Hz frame rate
Supply Voltages	1.8V/3.3V
Serial interface	3 wire

FD CMOS Provides Unique Performance Matrix in a Monolithic Imaging Device


Sensor Creations