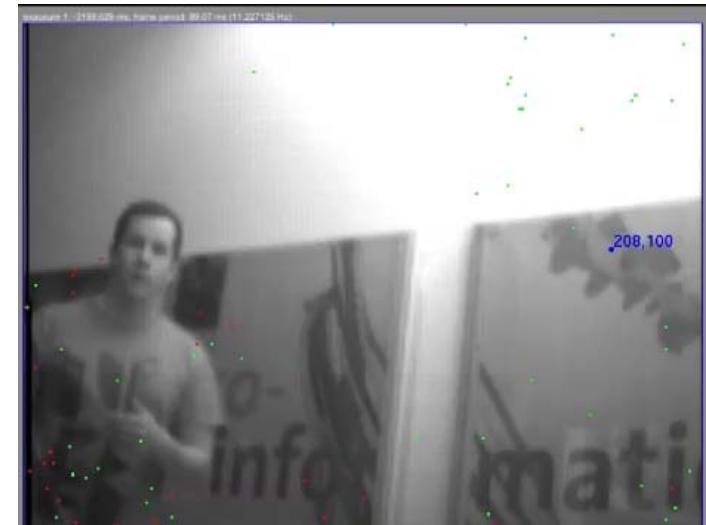
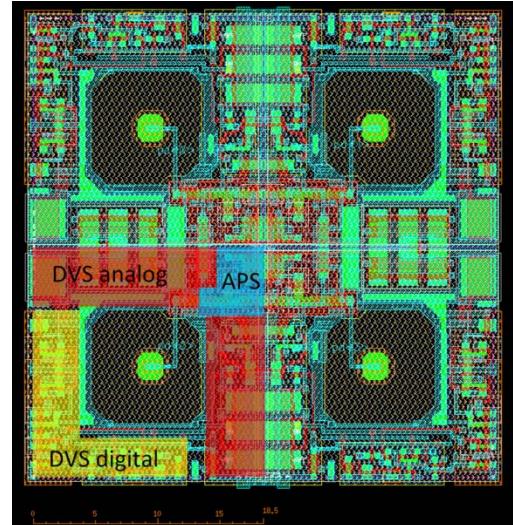
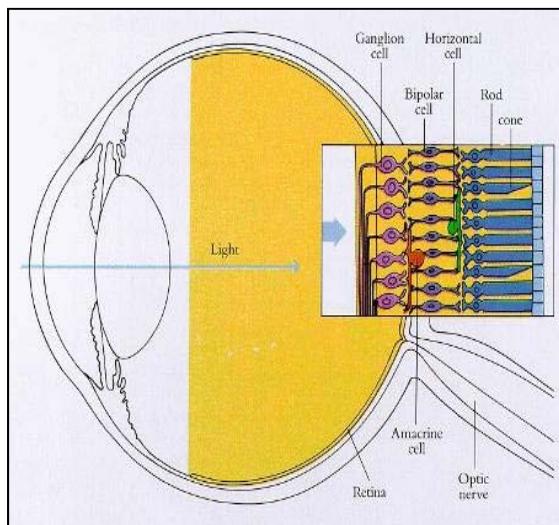


A 240x180 120dB 10mW 12us-latency sparse output vision sensor for mobile applications

Raphael Berner, Christian Brandli, Minhao Yang, Shih-Chii Liu
and Tobi Delbrück

*Inst. of Neuroinformatics,
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Machine Vision for Mobile Applications

- ENERGY matters because it is limited
- LATENCY is crucial for real time interaction

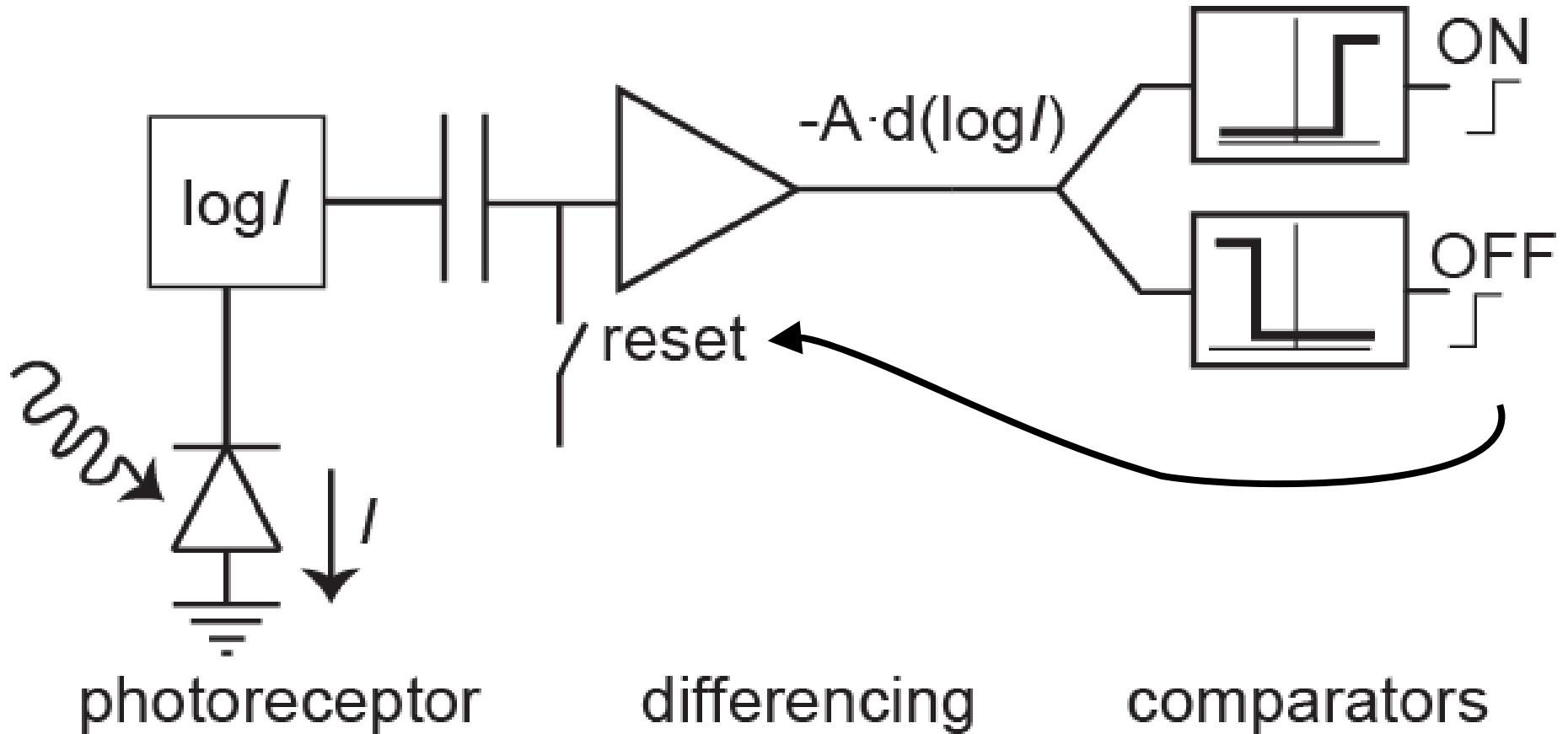
With conventional imager

- Low frame rate: low energy / high latency
- High frame rate: low latency / high energy

Most of the time and energy spent on redundant information in and between frames

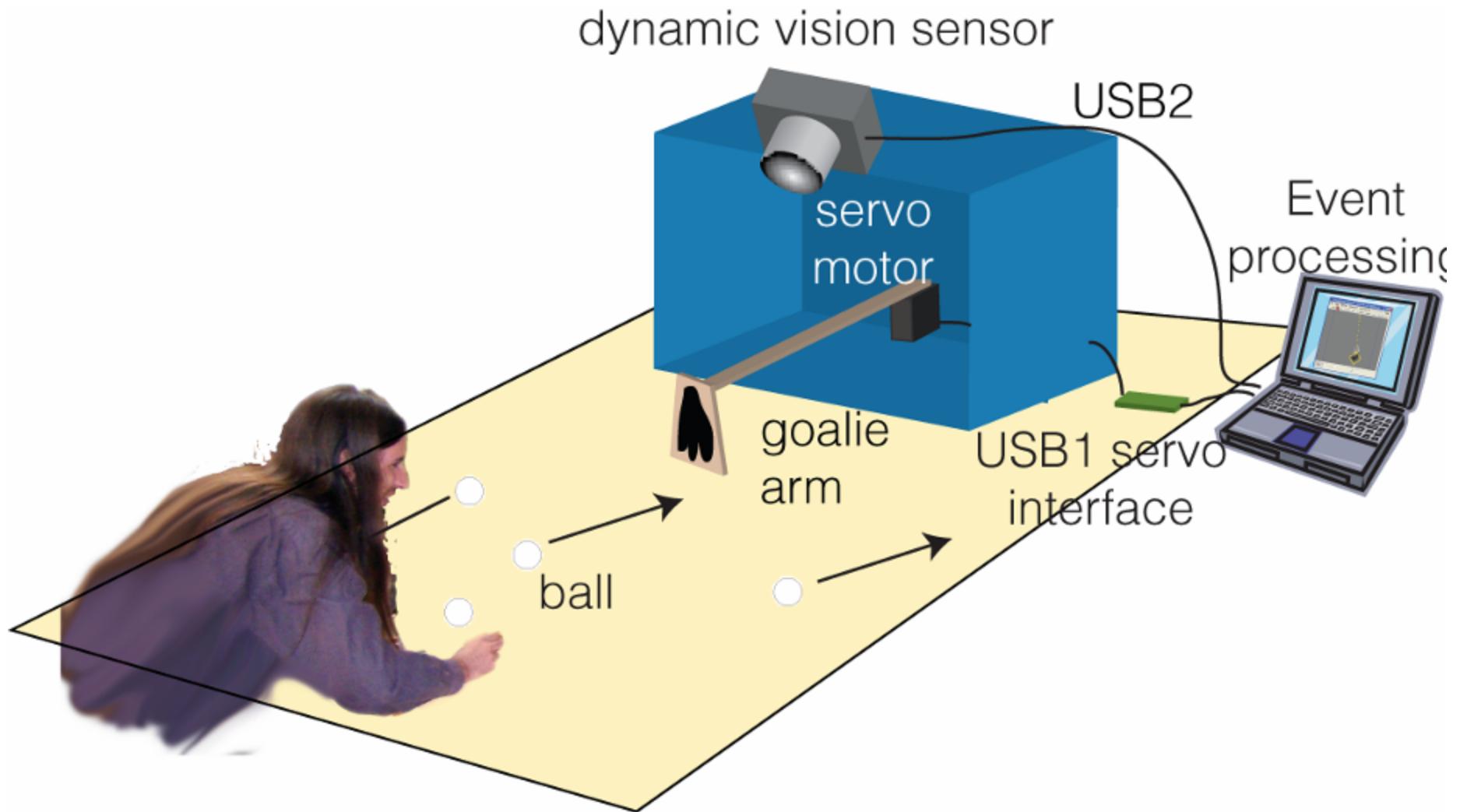
WE NEED SMARTER WAYS OF SENSING & PROCESSING

Simplified Dynamic Vision Sensor (DVS) pixel architecture



Lichtsteiner et al. JSSC 2009

Example DVS application - RoboGoalie



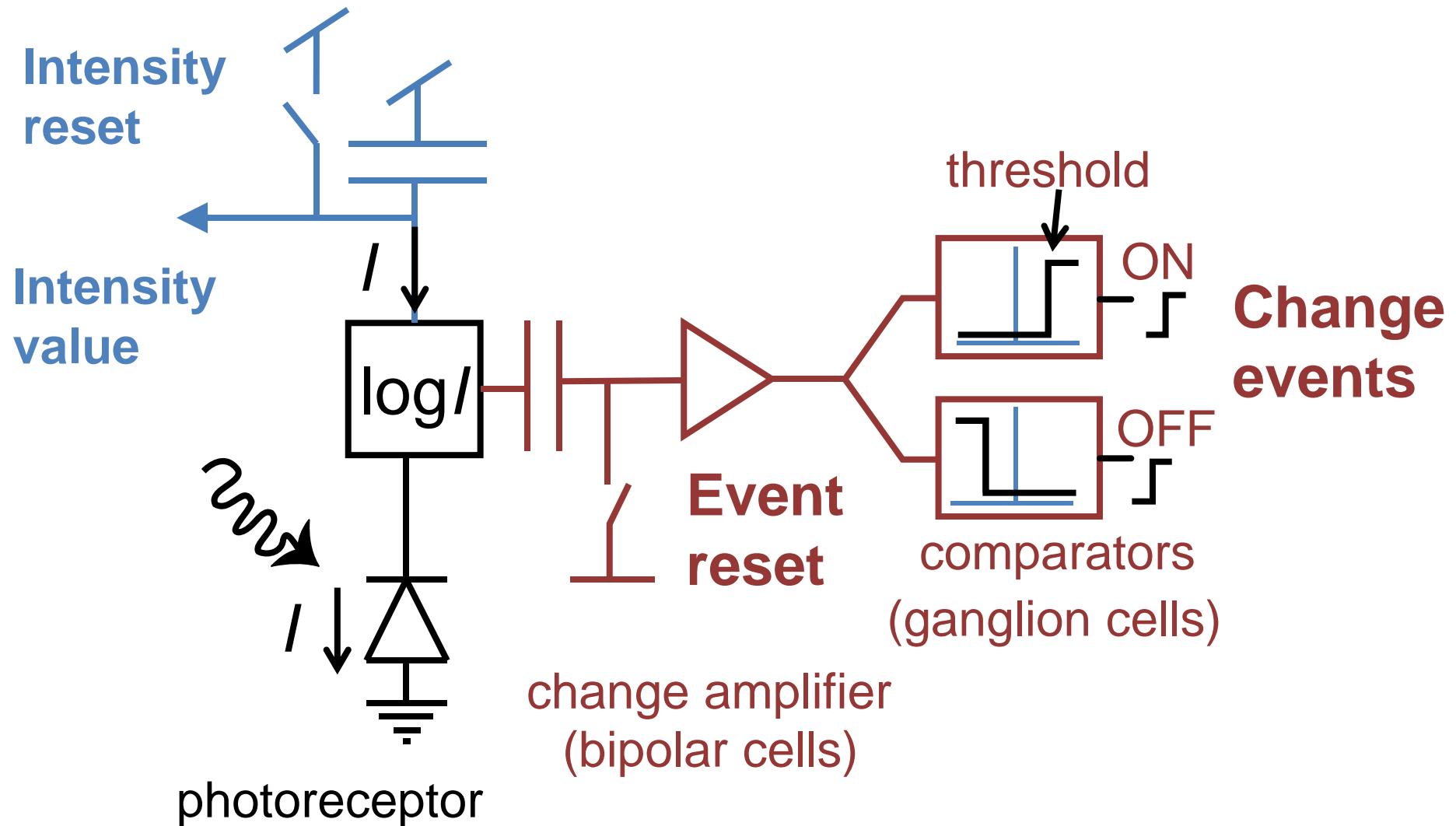
Example DVS application – RoboGoalie

Achieves 550Hz update rate at 4% laptop CPU load



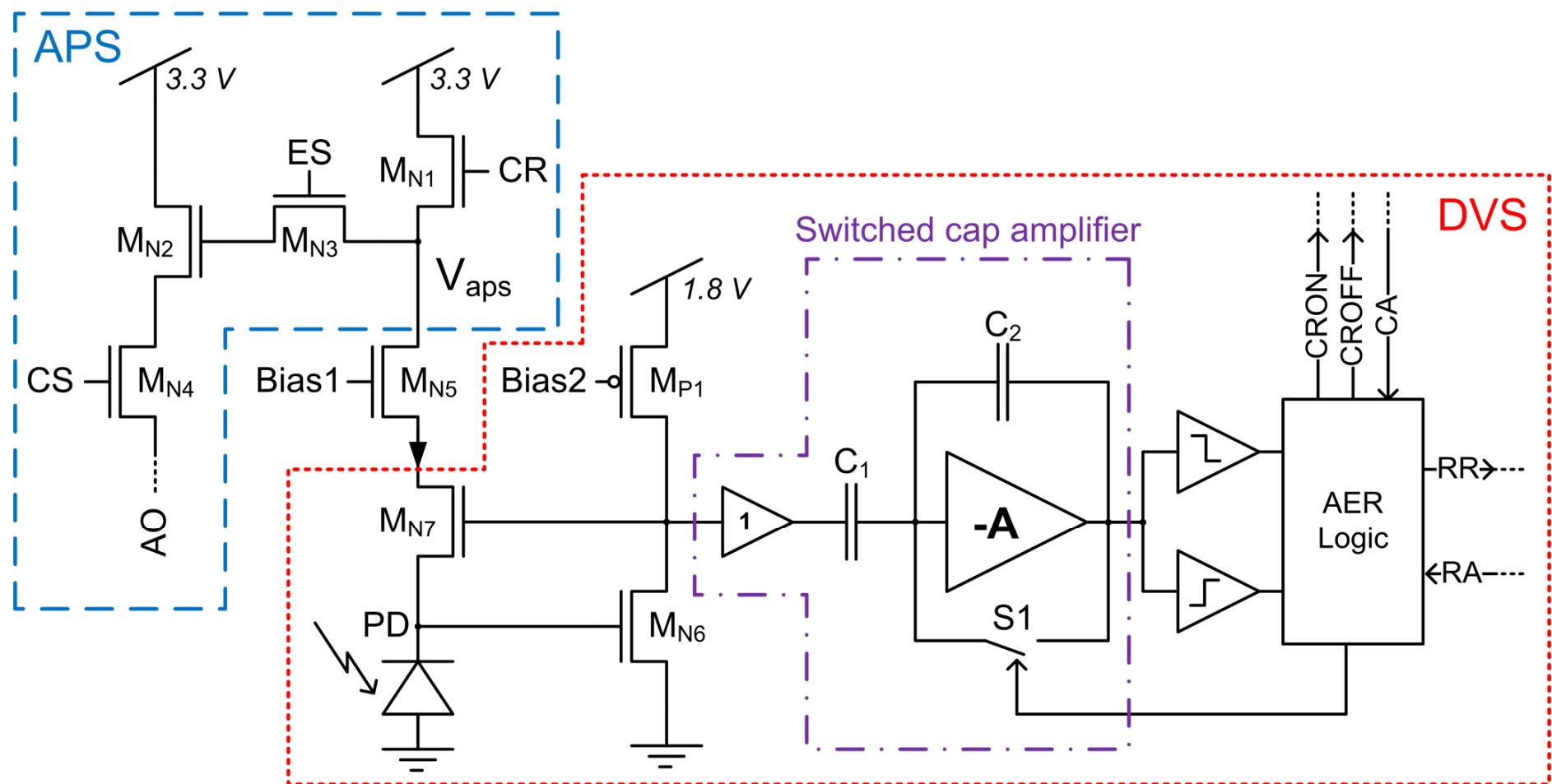
Delbruck et al.,⁵ 2009

The apsDVS chip adds an intensity readout to the DVS



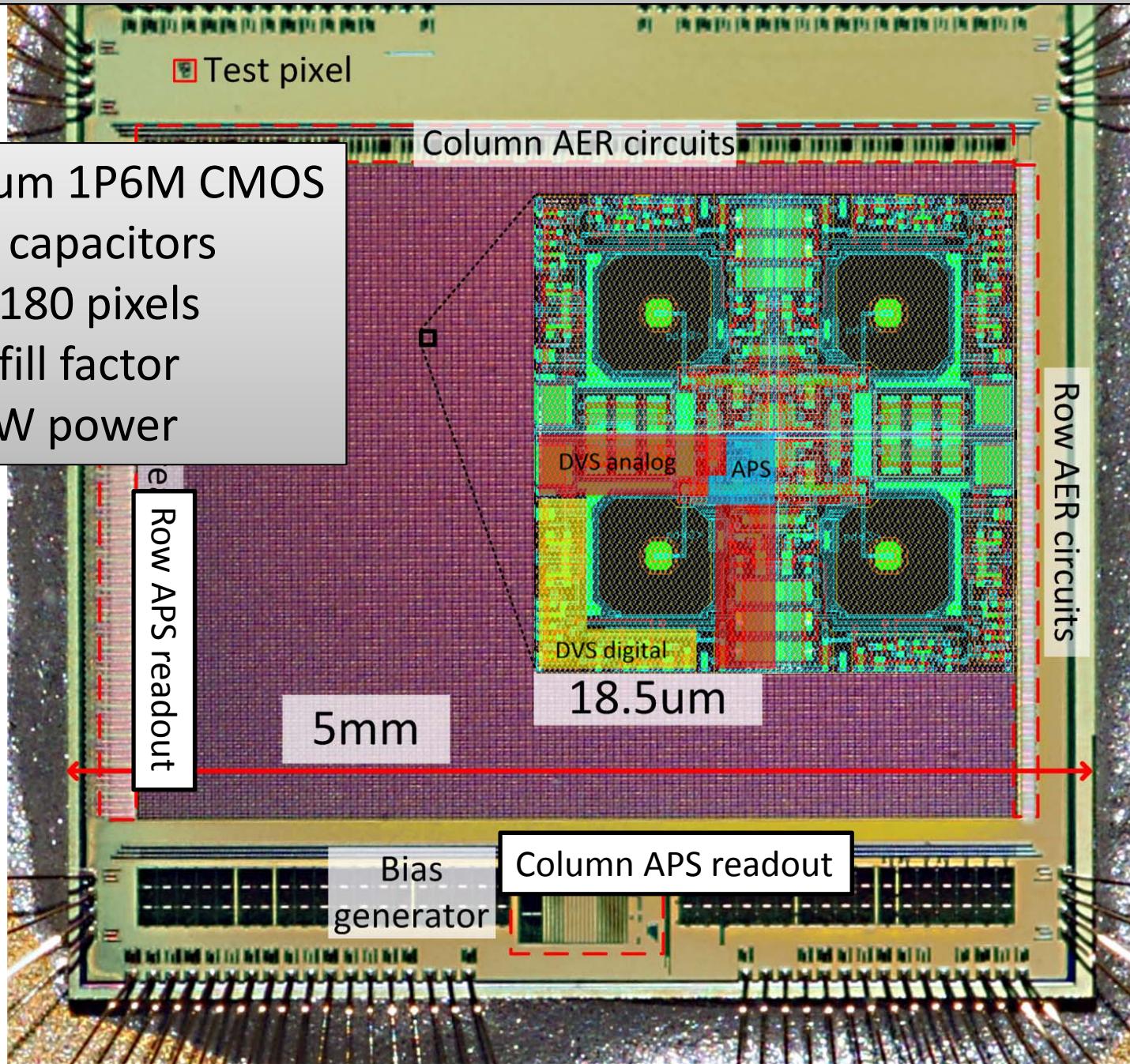
apsDVS pixel

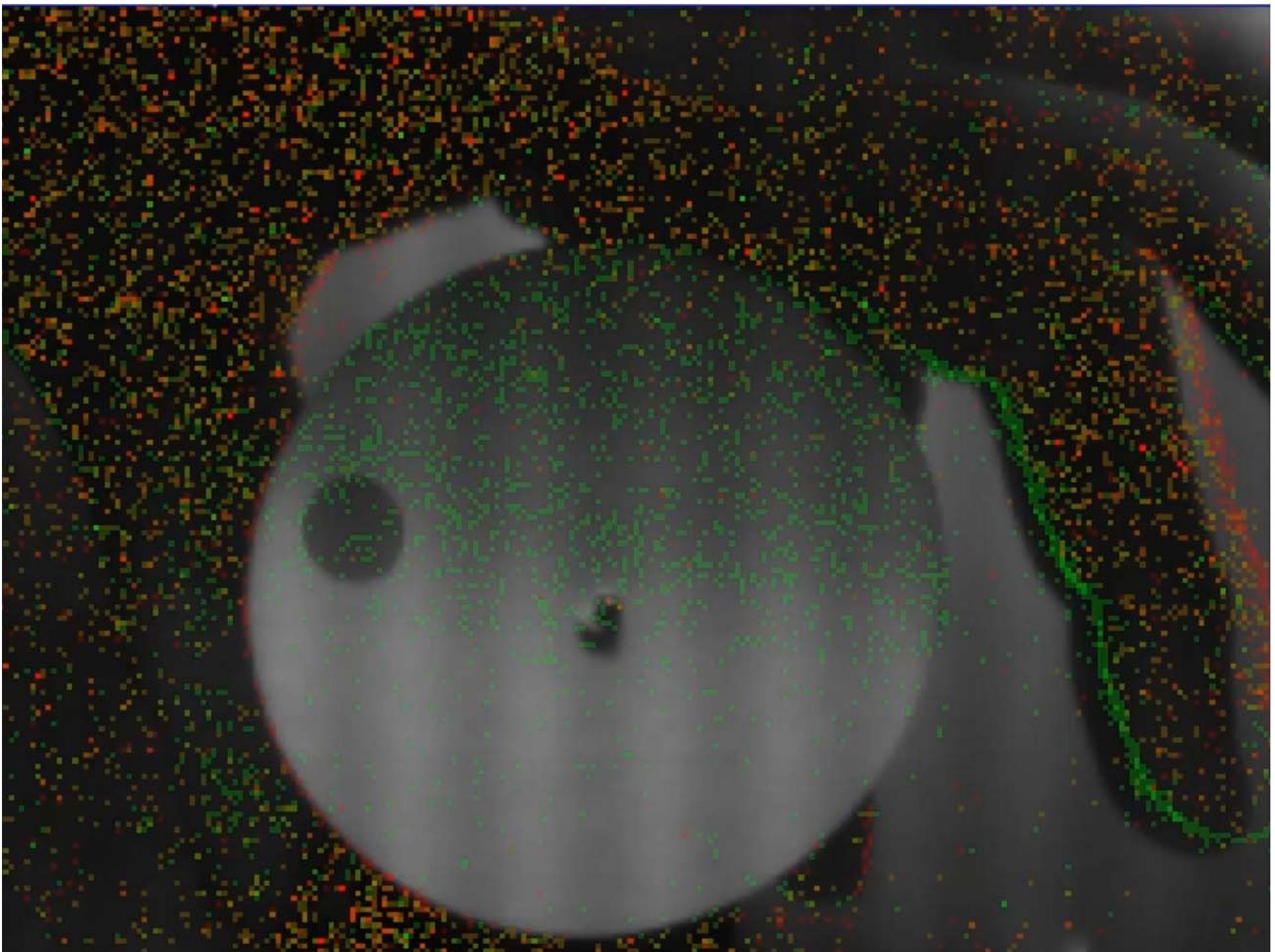
(aps=Active Pixel Sensor)



The apsDVS chip SBRET10

- 0.18um 1P6M CMOS
- MiM capacitors
- 240x180 pixels
- 22% fill factor
- 12mW power







Frame: 2531; Exposure 9.09 ms; Frame rate: 1.32 Hz



The apsDVS can enhance machine vision in several ways

- Low APS frame rate → **Low power**
- DVS output → **Low latency, sparse data**

Combined advantages:

1. DVS delivers motion features for free
2. Continuous tracking solves correspondence problem
3. DVS can be used to control frame rate or ROI



The apsDVS in Comparison

	This work (apsDVS)	ATIS (Posch et al.)
Intensity readout	APS	Time domain
Image Dynamic Range	57 dB	125 dB
Image FPN	1 %	<0.25 %
Pixel size [μm^2]	18.5 x 18.5	30 x 30
Fill factor	22%	15%
Pixel complexity	44 FET, 2 C, 1 PD	77 FET, 2 C, 2 PD
Fixed integration time	YES	NO
Power Consumption	~10mW (240x180)	~100mW (304x240)

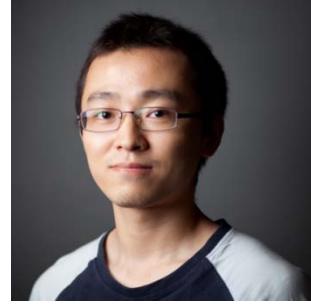
Thank you



Dr. Raphael
Berner



Christian
Brandli



Minhao
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Dr. habil.
Shih-Chii Liu



Prof. Tobi
Delbrück

sensors.ini.uzh.ch

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**Universität
Zürich**UZH

ETH

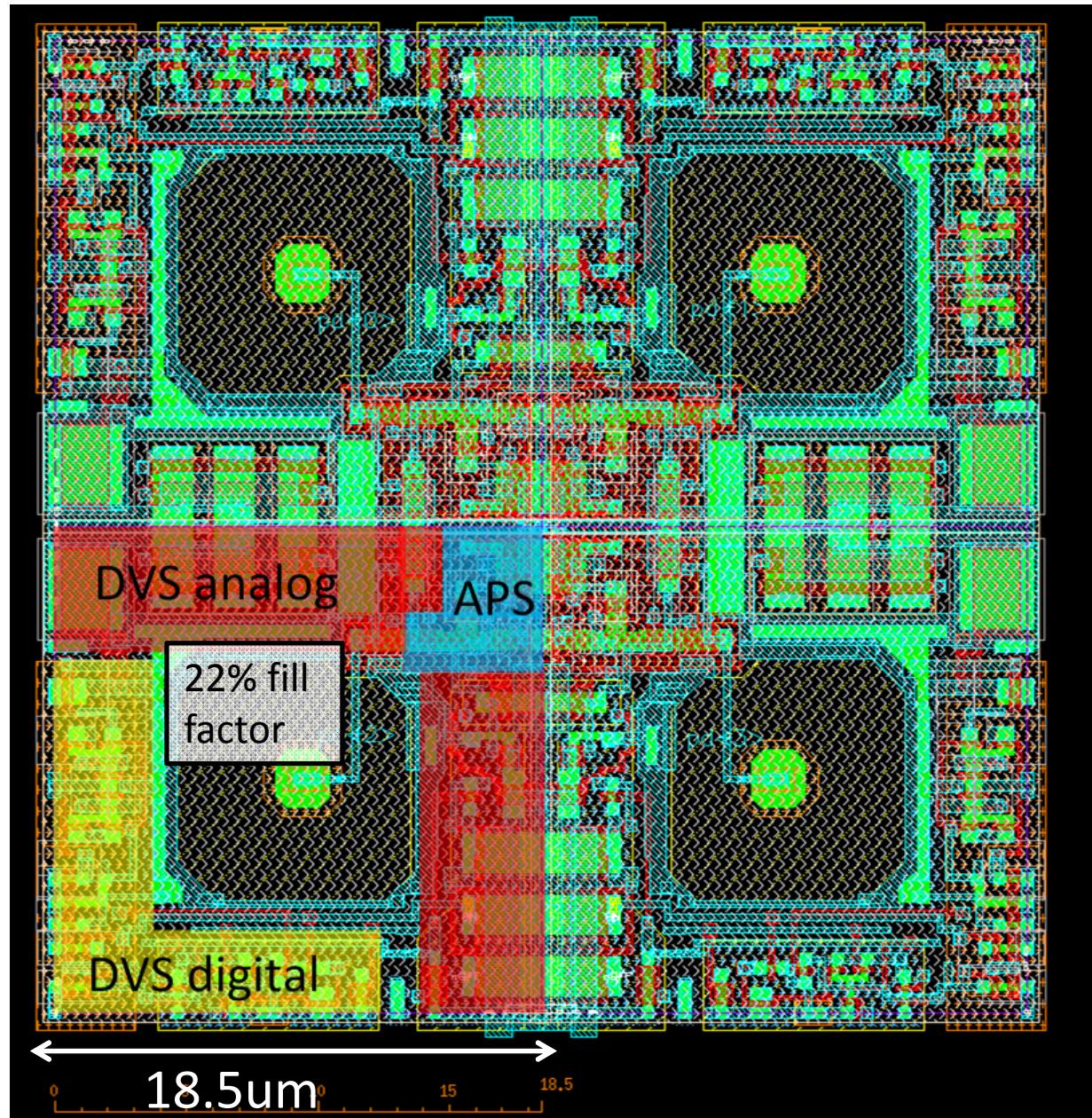
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich



robotics+

Swiss National
Centre of Competence
in Research

SBRET10 pixel layout



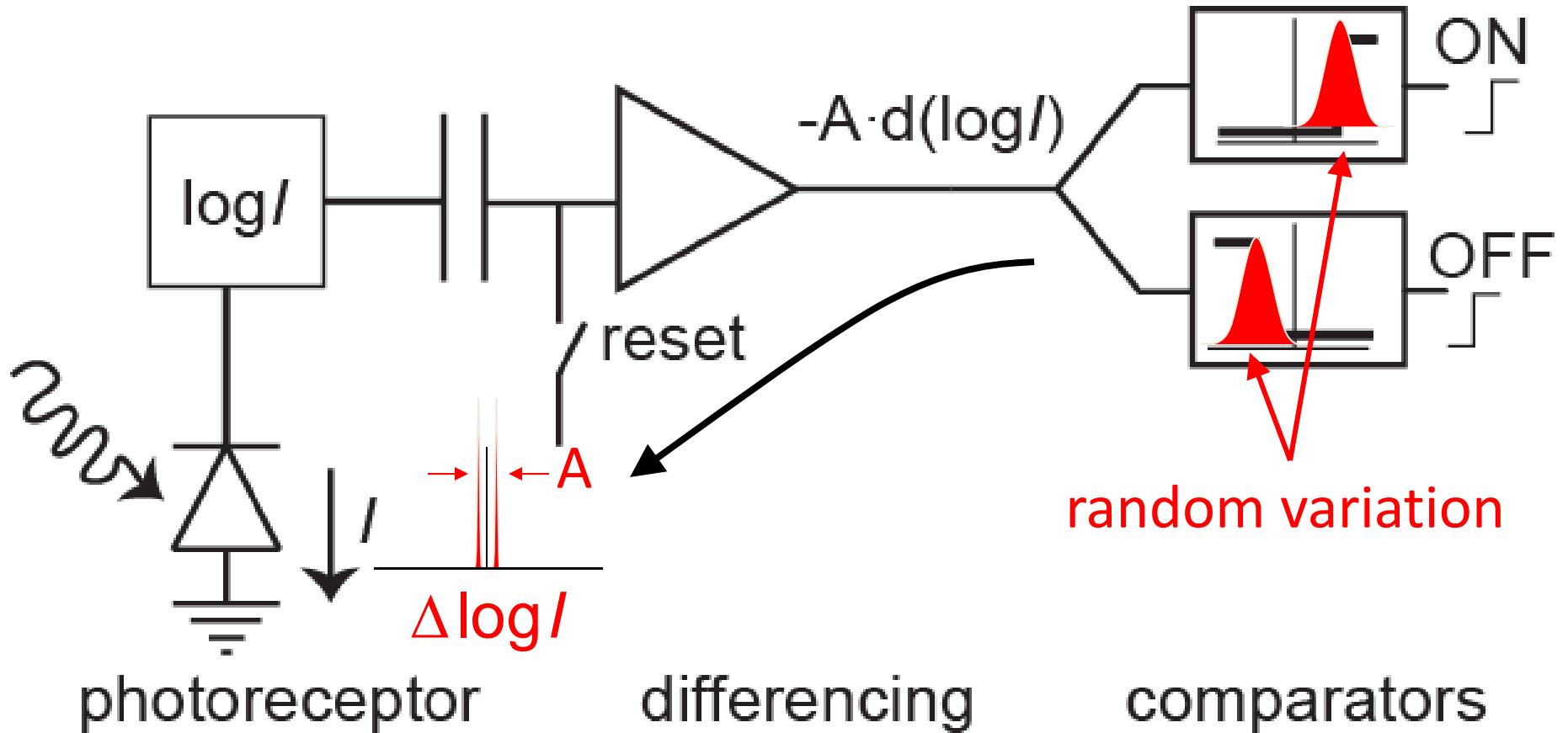
Design

Technology	UMC 180 6M 1P
Chip size	5x5mm
APS-DVS array size	240x180
Pixel size	18.5 x18.5 μm^2
Supply voltage(s)	3.3V/1.8V
Pixel architecture	apsDVS, 44T+2C.
Fill factor	22%

Measured

Power consumption	7.4mW low activity 13.5mW high activity
DVS event threshold limit	12% contrast
DVS illumination operating range	120dB (down to 0.1lux)
DVS latency	12us
APS readout frame rate	40 FPS
APS FPN (midlevel)	1% of full signal swing
Readout Noise	<2mV
Output Voltage Range	1.1V
APS Dynamic Range	~55dB

Simplified Dynamic Vision Sensor (DVS) pixel architecture



Lichtsteiner et al. JSSC 2009

