

# An Overflow Photo-gate Pixel Enables High FWC and Improved Proton Radiation Tolerance in CMOS Pixels

Yannick De Wit & Manuel Innocent

ON-Semiconductor, Schaliënhoedreef 20B, 2800 Mechelen, Belgium.  
Yannick.dewit@onsemi.com tel +32 15 448 773, fax +32 15 448 780

**Abstract** This paper presents a pixel/photodiode structure that enables high full well charge (FWC) storage with small pinned fully depleted photodiodes that can be manufactured in a standard CMOS image sensor process. Traditionally, pinned fully depleted photodiodes exhibit limited FWC due to the fact they need to be able to fully deplete at relative low voltages. The pixel architecture described in this paper uses an extra gate (an overflow photo-gate) over a part of the photodiode. This gate is operated at a relative high voltage during integration. This extends the full well charge without significantly increasing the photodiode or pixel size. Silicon results confirm a significant increase in full well charge as well as a reduction in proton radiation induced dark current when compared to traditional photodiodes with similar FWC.

## 1. Introduction

Today, most CMOS image sensor pixels consist of a pinned photodiode able to fully deplete of charge at a relative low voltage. This enables low noise (due to correlated double sampling) and low dark current. A disadvantage of such photodiodes is that only a limited amount of charge can be stored within the diode due to the relative low depletion voltage and limited volume.

Today, process solutions are available to increase the full well charge of small photodiodes, for example [1], but they require additional process steps which brings additional costs. Also, these solutions have disadvantages such as an increase in dark current and most likely a worsened proton radiation tolerance.

The solution presented in this paper consists of an extra gate on top of part of the photodiode to extend the photodiode capacitance during integration. The advantage is that no extra processing is required (in other words: no extra manufacturing costs) and that the extra charge is stored in a small volume close to the silicon surface which reduces proton radiation induced dark current. A disadvantage is the requirement of an extra control line.

## 2. An overflow photo-gate (OFG) to extend the photodiode FWC

Figure 1 presents a schematic of the overflow photo-gate pixel. Figure 2 presents a top layout and cross section example of an overflow gate pixel implementation where the gate is located at the top of the photodiode, partially overlapping the photodiode. Figure 3 shows a timing diagram to operate the pixel in rolling shutter mode of operation.

The principle of operation can be understood from the timing diagram shown in figure 3 and the fluid-analogy diagram in figure 4. First, the photodiode and overflow gate are reset (see Figure 4, A) to deplete them from all charge. Then, during integration, the overflow gate is operated at a voltage that enables inversion. Photon induced charge can be captured by this extra capacitance once the photodiode charge has dropped beyond a certain threshold voltage (see Figure 4, C). Due to the fact that the gate to inversion channel capacitance area density is significant higher than the photodiode capacitance area density, total full well charge of the structure can be significantly increased with the use of the overflow photo-gate according to Eq [1].

$$FWC_{extra}(e^-) = (V_{OFG} - V_t) \cdot Area_{OFG} \cdot Cox \quad [1]$$

With:

**FWCextra:** extra FWC in electrons [e<sup>-</sup>] from the overflow photo-gate.

**Vofg:** Voltage [V] applied on overflow photo-gate during integration.

**Vt:** threshold voltage [V] of overflow photo-gate.

**Area\_ofg:** Area [um<sup>2</sup>] of overflow photo-gate overlapping the photodiode.

**Cox:** Oxide capacitance per area [fF/um<sup>2</sup>].

As can be seen from the timing, during transfer of charge from the gate structure and photodiode to the floating diffusion, the gate voltage is pulsed down to a lower voltage. This pushes the charge out of the gate's inversion channel into the photodiode and eventually into the floating diffusion(see Figure 4, D).

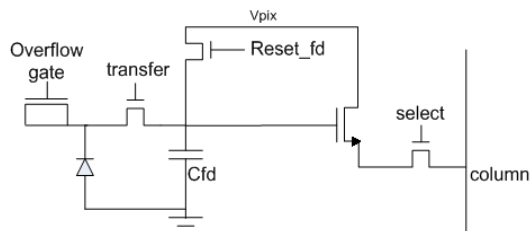
### 3. Silicon results confirm FWC increase and improved proton induced radiation tolerance

Figure 5 show different response curves for different OFG operating voltages (during integration). Figure 6 presents the linear full well charge in function of these operating voltages. Figure 7 presents the dark current with and without proton radiation. Figure 8 presents the image lag measurement. Figure 9 shows an overview of the overall results for the OFG pixel and two comparison pixels.

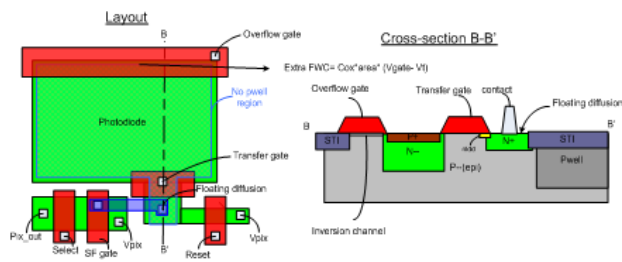
As can be seen, the overflow photo-gate structure allows to extend the FWC significantly without increasing image lag and noise while having a significant reduction in proton radiation induced dark current when compared to a normal photodiode with similar full well charge.

## 4. Summary

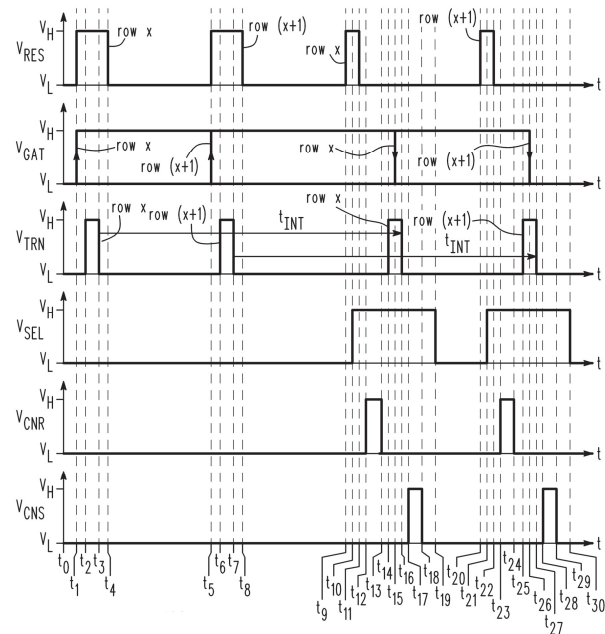
An overflow photo-gate structure can increase the full well charge of a pinned photodiode significantly and improves proton induced radiation tolerance for similar FWC pixels. The structure can be beneficial in CMOS pixels that require high SNR and/or improved proton radiation tolerance.



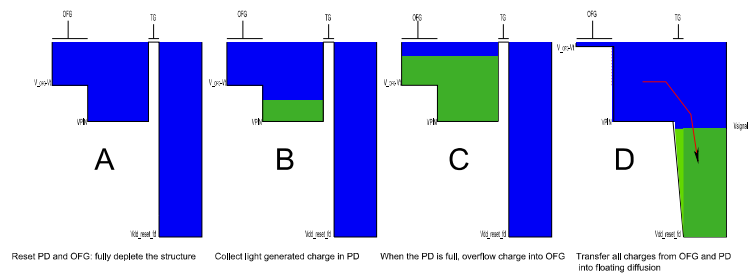
**Figure 1: Overflow-gate pixel schematic**



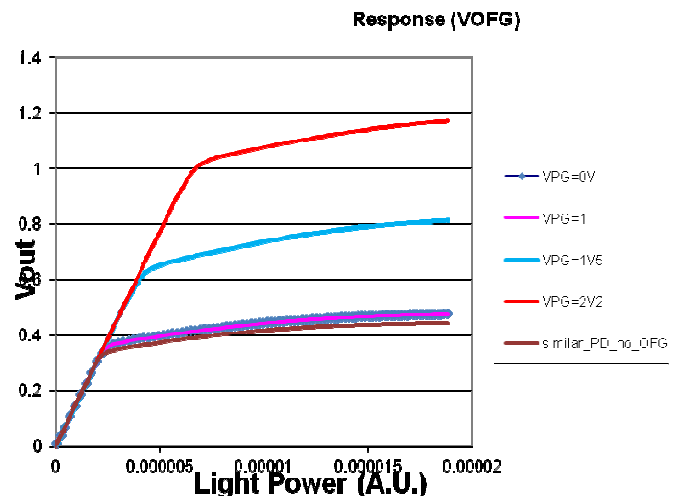
**Figure 2: Overflow-gate pixel top layout and cross section**



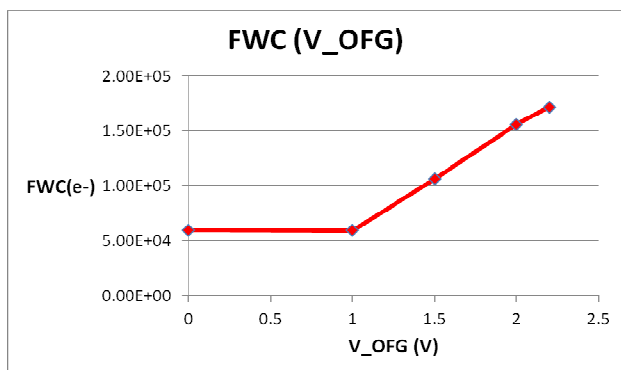
### Figure 3: Rolling shutter timing



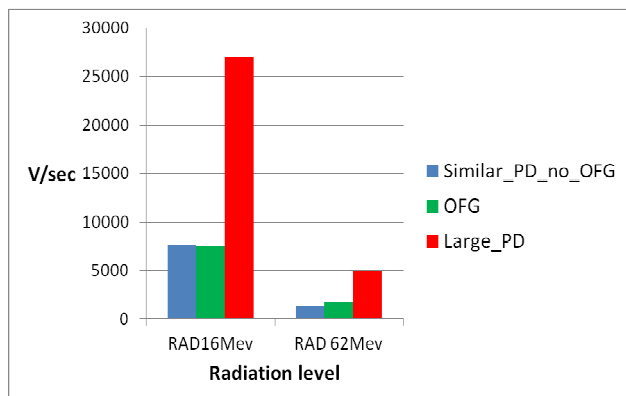
### Figure 4: Fluid-analogy diagrams



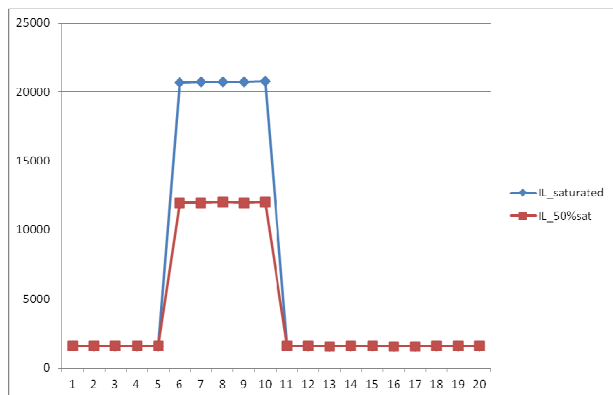
**Figure 5: Response comparisons: Full well charge increases with OFG voltage**



**Figure 6: FWC in function of OFG voltage**



**Figure 7: Proton radiation tolerance comparison**



**Figure 8: Image lag measurement (DN(Frame): no image lag observed)**

Parameter	Small PD + OFG pixel (2.2V)	Small PD, no OFG	Large PD, no OFG
Pixel size (um)	10	10	10
FWC (e-)	172K	57K	190K
Conversion gain (uV/e-)	6	6	6
Noise (uV) System noise included (~300uV)	350	350	350
Image lag (% Full Swing)	< 0.35	< 0.35	< 0.35
DC 20C (e-/sec)	~30	~30	~30
DC 20C 16MeV (e-/sec) Fluence 1e11 p/cm2	7K	7K	27K
DC 20C 62MeV (e-/sec) Fluence 1e11 p/cm2	1.6K	1.4K	5K

**Figure 9: Overall results comparison**

#### References:

[1] *J. Michelot*<sup>1</sup>, Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage. In Proc. 2011 International Image Sensor Workshop, Hokkaido, Japan , June 2011.

