Global Shutter Pixel with Floating Storage Gate

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The new generation global shutter pixel must have a built-in correlated double sampling (CDS) circuit. One popular technique is to use a dual pinned diode pixel [1-3], the other is to build the CDS using ordinary capacitors [4-5]. The first topology allows small pixel size and potentially small dark current. The advantage of the other design is an extremely low shutter leakage.

In this paper, we will discuss a different way to implement the CDS in-pixel, which is based on a floating resettable Storage gate.

1. *Floating Gate Readout*

Floating gate was a popular readout in Charge Injection Devices (CIDs) and in Hybrid IR FPAs of 1970s [6,7] and was also considered for the CCD output amplifier [8]. A Resettable Floating Gate includes a reset switch, a MOS (CID) gate/photogate over a thin oxide on a substrate, and an amplifier (Fig.1). This simple structure operates as follows:

a) Accumulation and holding of the charge. Signal charge may come by photo-collection or by transfer from a neighbor CCD cell. The gate is held at a fixed potential. The amount of the accumulated charge Q_s relates to the change in the surface potential under the gate through the formula $Q_s = (C_{ox} + C_d) * \delta\phi_s$, where $\delta\phi_s$ is the change in the surface potential between the state being fully depleted and the one with the charge. C_{ox} is the thin oxide, and C_d is the depletion layer capacitances.

b) Readout. During the readout, the charge is removed from under the floating gate, by injecting into the substrate or by a transfer out through a neighboring gate. Before the charge is removed, the Storage gate is made Floating, and the potential at the gate is measured twice, first with the charge and then without the charge. This implements the CDS function. Due to charge conservation, the mobile charge which is gone must be replaced with the charge of ionized acceptors, so the depletion layer grows, and the potential change V_{sig} at the gate could be estimated as $V_{sig} = (C_{ox} + C_d)/C_d * \delta\phi_s$. In case of a lightly doped substrate (e.g. 10^{15} cm^{-3}) and a thin dielectric (e.g. 70A), a 1V "layer" of accumulated charge could translate into a 10V signal when the charge is removed.

A high capacitance of the gate for storage and a small capacitance for readout makes the floating gate a very interesting concept to try in the pixel design.

2. *The Schematic and the Operating of a 7T Pixel.*

We developed a 7T global shutter pixel with floating resettable Storage Gate, drawn in Fig.2. The photodiode, the Anti-blooming (shutter) gate AB, the transfer gate TX, the source follower SF with Row enable, are the standard components of a 5T pixel. New are the storage gate SG, and the second transfer gate TX2. Assuming a CCD-like functionality of the 7T pixel, one needs to execute the following controls: a) Turn RST switch ON and pulse SG High during the global charge transfer TX. This transfers the charge from photodiode into the storage. After TX returned to Low, SG gate may also be turned into a Hold state with a lower fixed storage voltage on it while the RST switch is still ON. To read from the pixel, SG gate is left floating, and the first sample from the pixel is read out through the SF. Then TX2 gate is turned ON, and the charge is removed from under the Storage Gate area into vdd.

As the electrons are leaving the storage, the potential on the floating gate rises. After TX2 transfer is completed and TX2 is returned to Low, the potential on the floating gate is read for the second time.

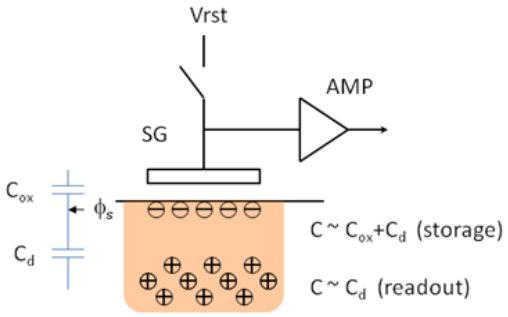

Fig.1. Floating gate readout.

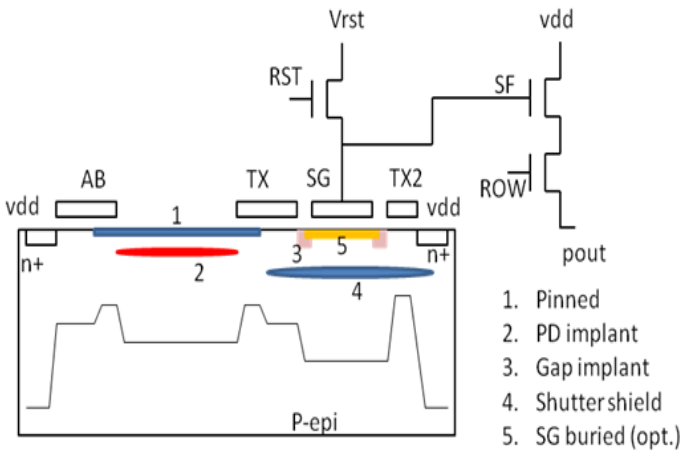

Fig.2. A 7T global shutter pixel that uses a floating storage gate.

3. The Layout and the Process.

The layout of the pixel's key layers is presented in Fig.3. Pixel is drawn in a 1P4M 0.18um process. Pixel size is 7um. The gap between gates is 0.24um. Photodiode area is 50% of the pixel. Size of the storage gate is 2.4um^2 , and we expected ~ 1-2fF readout capacitance of the floating Gate itself and the parasitic capacitance of 1-1.5fF.

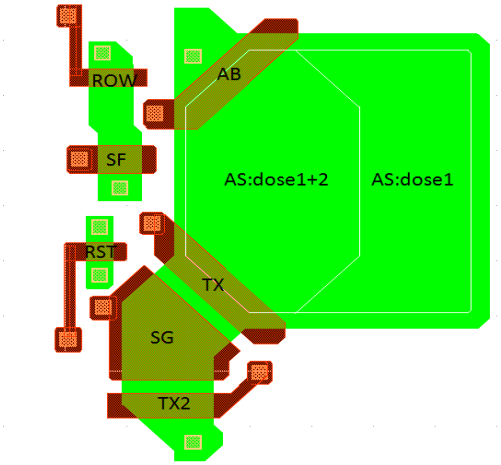

Fig.3. Pixel layout (Diff., Poly, Cont.).

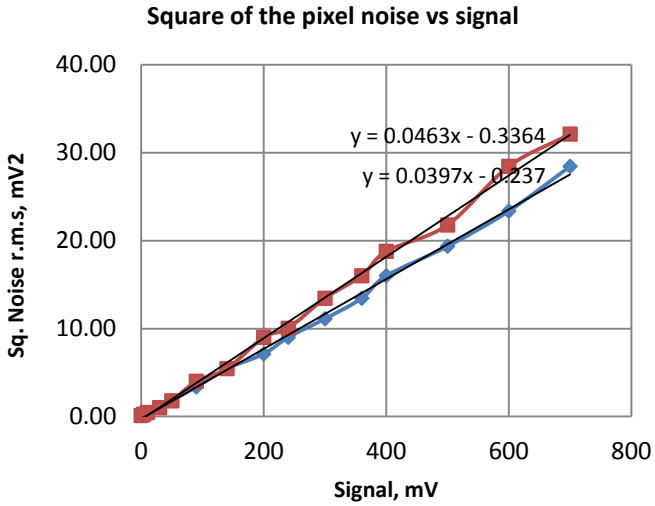

Fig.4. Conversion gain data for BSG (top) and SSG

The process to manufacture the 5T pixel includes a photodiode surface BF2 done twice before Poly and after. The implant before Poly overlaps with TX and AB gates, creating a barrier (see in Fig.2.) preventing the back-spill of the transfer charge flowing via TX/AB. The photodiode's buried arsenic implant is done with 2 masks, one covering all protodiode area, the other – only the area shared by TX and AB gates in their proximity (Fig.3.). The primary goal of doing so is to avoid the formation of the potential pocket in the middle of the photodiode. This may not be needed for a small pixel, but for a 7-14um pixel, a 100-200 mV potential "bowl" in the center of the photodiode occurs

naturally. Other benefits of having a dual AS implant are a) creating an electric field towards AB/TX gates, and b) the control of the Photodiode Capacity. The area with the single implant serves for photo-collection while the area with the dual implant serves as the photodiode storage.
7T pixel requires 2 more masks. One mask is the Storage Gate Buried channel mask. This operation is optional. The storage gate could be either Surface channel (SSG) or Buried channel (BSG). The second mask defines Gap implant. A little dose of arsenic is implanted after Poly to compensate for the barriers in the Gap areas between the Poly gates. The first use of the Gap mask is before Poly to deep implant the Shutter Shield boron.

4. Experimental results

A test structure with 3x3 pixel array was manufactured in the periphery of our custom sensor product. The test keys were assembled and tested using a custom test jig. The pixel was loaded on a 40 kOhm/ 10pF load and followed by a CDS sampler.
Calibration. With RST switch ON, applying a pulse to Vrst input, one may measure its amplitude at the output and calibrate the source follower. All the following data is referred to the Storage gate node.
Conversion gain. The standard procedure (Square of the noise vs signal, Fig.4.) was used to estimate the pixel Conversion Gain, Noise, and Charge Handling Capacity of the pixel. The conversion gain for the Surface channel SSG device was 40 uV/e-, and 46 uV/e- for BSG, giving a readout capacitance of 4fF and 3.5fF, respectively.
Saturation voltage. For Surface Storage gate, the saturation was at 1.2V, for Buried channel Storage at 1.4V.
Saturation charge. The measured saturation charge was 30,000e-. Based on the SG area of 2.4um2, we expected the Storage capacitance be 12 fF. Including the parasitic capacitance, and the gap area as the storage, we calculated the designed Surface Storage Gate should be able to keep up to a 90,000e- charge with 1V filling. Why did the measured saturation charge was much lower? – Our explanation is that we were photodiode capacity limited.
Noise. The noise measured with the unity gain was 8e- for the surface-channel storage and a little less, yet still rounded to 8e- for the BSG.
Shutter efficiency. Static shutter efficiency was estimated by comparing the signal from the pixel at full exposure with the signal from the pixel with AB gate ON. The signal ratio was 600:1, translating into the shutter efficiency of 99.84%. This is not sufficient to many industrial applications, and the pixel needs further work on reducing leakage.
Dark current The dark leakage signal due to dark current was relatively high in the device with surface channel storage ~1mV/ms at 60^{o} C, the Buried Storage leakage was much smaller <0.1 mV/ms at 80^{o} C
Image Lag. We did not notice any image lag associated with the Storage gate and Poly gaps.
Wide Voltage Range operation. If the photodiode capacity matched the calculated capacity of the storage gate of 90,000e-, we should be seeing a 3.6V-4.2V signal swing from the pixel floating node, on top of the Reset voltage of 1.2-1.5V. This would be way above the 3.3V process tolerance. One way to handle the large voltage swing is to develop a high voltage pixel/column storage readout. The other option is to read the large signal charge in portions. If the charge is so large and cannot be removed in one attempt, the remaining charge can be read in the second read which would include the repetition of the preset of the SG gate, turning TX2 ON, and taking the difference in SG potential before and after the charge spill. The total signal can be obtained by summating of the partial reads.
We emulated the proposed partial readout by lowering the TX2 High voltage so that the storage node could not be fully emptied in one readout cycle. The remaining charge could then be read in the next read cycle. This is illustrated in the oscillogram of Fig.5. The LED light was pulsed once in 4 readout cycles. We see the first and then the second signal coming out, generated with one LED pulse.
DC operation of Vrst. We checked we do not necessarily need a high voltage at the Storage gate during the charge transfer from photodiode through TX. The DC voltage of 1.2-1.5V which is optimal for the hold operation, could also be used during the TX charge transfer. The trick is when TX gate goes High it sucks all the photodiode charge under it and then pushes it into the Storage area with no spill-back into the photodiode because of the barrier built under the TX gate on its left side adjacent to the photodiode.

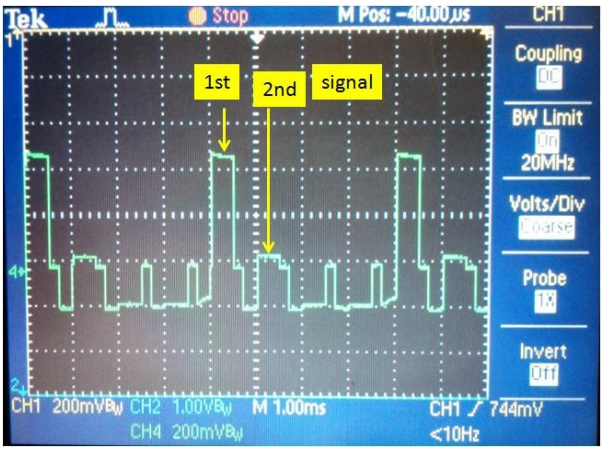

Fig.5. An oscillogram of the pixel output showing the possibility of a dual (multiple) read of a large stored charge.

Pixel	7um 7T global shutter
Process	0.18um 1P4M
Conversion gain (SSG/BSG)	40 /46 uV/e-
Saturation charge	30,000e-
Noise	8e-
Shutter efficiency	99.84%
Dark signal (BSG) at 80° C	<0.1 mV/ms
Responsivity (SSG/BSG)	8 /7 V/Lux-s
Linear Dynamic range	71 dB

Table 1. Measured pixel parameters.

Conclusions:

We have developed and implemented a new type of the Global Shutter Pixel with a built-in Correlated Double Sampler in the Standard CMOS technology with 2 additional masks and implant steps. The pixel uses a floating storage gate readout, originating from the circuit ideas of the early Charge Injection Devices and CCDs.

The storage gate may have a high charge capacity in combination with low readout capacitance thereby providing the combination of a large signal and low noise (due to CDS). The pixel may be promising for scientific and industrial imaging applications requiring high speed, high charge handling capacity, a reasonably large pixel size of 5-15 um, and a low noise. The conventional techniques of sharing the readout and sharing the controls could be further used to increase the efficiency of the area usage, especially in smaller pixel designs.

Based on this pixel technology, we designed a high speed 1 Mpixel CMOS image sensor which will be tested some time soon. We expect an additional information on the pixel uniformity, noise with a column amplifier, and on the distribution of the dark current, missing in the testing of the single pixel reported here.

The author would like to acknowledge useful discussions with Jaroslav Hynecek when developing the pixel.

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