# 3.5 µm global shutter pixel with transistor sharing and correlated double sampling

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#### Introduction

We report on a global shutter pixel with in-pixel voltage domain sampling of the signal and reset levels and 3.5  $\mu$ m pixel pitch. To shrink the pixel dimensions to 3.5  $\mu$ m pixel pitch, a CMOS image sensor process with 110 nm front-end and 90 nm back-end design rules was used, and transistor sharing between two neighboring pixels was implemented.

### Discussion

CMOSIS has been developing over the past years several high speed global shutter image sensors with pixel pitch down to 5.5  $\mu$ m [1]-[3]. These sensors were all manufactured in 0.18  $\mu$ m CIS technologies and using the 8-transistor pixel architecture that allows to combine pipelined global shutter operation with CDS. Apart from the noise performance advantage [4] compared to widely used 5-transistor global shutter pixels [6], this type of pixel also has typically better shutter efficiency than pixels where the signals remain stored in the charge domain after the exposure time. This makes this global shutter pixel compatible with backside illumination [4]. Charge-domain global shutter pixels have been scaled to 3.75  $\mu$ m pitch [7], but scaling with 8-T voltage domain global shutter pixels is more difficult due to the capacitor area and interconnect routing. In order to shrink the pixel size, we made use of a more advanced technology and readout transistor sharing [8,9]. A high resolution custom-designed sensor has been manufactured and is now in mass production. The process technology is ST Microelectronics with 110 nm front-end and 90 nm Cu back-end technology, a process originally developed for 1.75  $\mu$ m (rolling shutter) pixels. In this technology, only 2 metal layers are used in the pixel array (see also [5]).

Due to transistor sharing in the front-end of the pixel readout, the effective number of transistors per pixel is 6.5 (and two capacitors). Figure 1 shows the circuit diagram of two horizontally adjacent pixels, which share the floating diffusion sense node Cfd and the transistors M3, M4 and M5. The charges of the two adjacent photodiodes PDa and PDb are sampled sequentially into a set of in-pixel capacitors C1a/b and C2a/b at the end of the exposure time. The 2x1 pixel ensemble contains 13 transistors, of which 3 source followers M4, M10 and M11. The timing diagram is shown in Figure 3. At the end of the exposure time, the floating diffusion is reset a first time and its reset level is sampled on C2a. Charge from PDa is transferred and sampled on C1a. Then this sequence is repeated for the readout of PDb, with sampling of signal and reset levels on C1b and C2b. Due to the sequential operation and the floating diffusion sharing, there is a small time shift between the sampling of the pixels sharing their floating diffusion. It can range from few microseconds for small arrays up to few tens of microseconds for very high resolution sensors, and is not an issue for the majority of the applications. This shift is implemented in two different ways, optimized for monochrome or color image sensors, as shown in Figure 4. In monochrome mode the exposure time shift occurs between odd and even columns. For color image sensors the shift occurs between pairs of neighboring columns. In this way, a pair of 2x2 pixels of the Bayer color filter kernel is acquired without time shift, which avoids color errors at moving objects.

While the floating diffusion is shared between horizontally neighboring pixels, the select control line is shared between two diagonally neighboring pixels, as shown in Figure 2. One vertical output bus connects the signal of the left-side positioned pixel to the column amplifiers at the bottom side of the pixel array, while the other output bus connects the signal of the right-side positioned pixel to the column amplifiers at the top side. The diagonal select sharing also allows to increase frame rate by 2x when 2x1 horizontal charge binning on the shared floating diffusion is used. In the sensor, column ramp ADCs are used to readout the pixel array in 12, 10 or 8-bit mode (see also [1][5]).

To make optimal use of the available area, the spatial sampling is slightly non-uniform, i.e. the photodiodes are in horizontal direction placed at non-equidistant positions. This is illustrated in Figure 5. Micro lens design and processing were optimized to reach the measured peak quantum efficiency of 46 % (monochrome) and 34 % (green color).

## Conclusions

Table 1 summarizes measured performance parameters on the pixel. Despite the small pixel pitch, the dynamic range remains close to 60 dB and the shutter efficiency is excellent. The parasitic light sensitivity of the in-pixel storage nodes is about 1:5000. This is measured as ratio in sensitivity of the pixel during readout (when the photodiodes already capture the next image) and during exposure. This corresponds with a shutter efficiency of above 99.98%.

Figure 6 shows an example image taken with the custom-designed high resolution sensor using the described 3.5  $\mu$ m pipelined global shutter pixel (raw data, no correction applied, only basic color processing).

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## References

[1] X. Wang, et al, "A 2.2M CMOS Image Sensor for High Speed Machine Vision Applications", proc. SPIE vol.7536, San Jose, Jan. 2010

[2] G. Meynants, et al, "Backside illuminated global shutter CMOS image sensors", IISW 2011.

[3] J. Bogaerts, et al, "High speed 36 Gbps 12Mpixel global pipelined shutter CMOS image sensor with CDS", IISW 2011.

[4] G. Meynants, "Global shutter pixels with correlated double sampling for CMOS image sensors", Advanced Optical Technologies, Volume 2, Issue 2, Pages 177–187, March 2013.

[5] G. Meynants, et al, "24 MPixel 36 x 24 mm<sup>2</sup> 14 bit image sensor in 110/90 nm CMOS technology', IISW 2013.

[6] "Five Transistor CMOS Pixel", US patent 7,045,653

[7] J. Solhsuvik, et al, "A 1.2 MP 1/3" Global Shutter CMOS Image Sensor with Pixel-Wise Automatic Gain Selection", Proc. ISW 2011, Hokkaido, June 2011.

[8] R.D. McGrath et al., "Shared Pixels for CMOS Image Sensor Arrays," IEEE Workshop on CCDs and Advanced Image Sensors, pp. 9-12, 2005.

[9] J. Aoki, et al, "A Rolling-Shutter Distortion-Free 3D Stacked Image Sensor", proc. ISSCC, 2013







Figure 2: Schematic view on pixel sharing for charge sensing and readout



Figure 3: Pixel timing for start and end of exposure and during readout



Figure 4: Integration shift implementation for monochrome and color mode operation.



Figure 5: Global shutter pixel layout at 3.5  $\mu m$  pitch.

Parameter	Value / comment
Technology	110 nm front-end / 90 nm Cu back-end
	2 Cu metal layer in pixel array
	3 Cu + 1 Al metal layers in periphery
Pixel	3.5 $\mu m$ pipelined global shutter
Temporal noise	17.6 e- rms
Linear Full Well Charge	14,800 e- (< 1% deviation from linear slope)
Linear Dynamic Range	58.5 dB
Dark current	151 e-/s @ 25ºC; 3330 e-/s @ 60ºC
Shutter Efficiency	> 99.98 %
QE (550 nm) monochrome / color	46% (monochrome) / 34% (green channel)
FPN	0.24 % rms
PRNU	1.2 % rms (monochrome and color)
Lag	0.2 %

### Table 1: Measured pixel characteristics



Figure 6: Example image taken with the high resolution sensor using the described global shutter pixel (raw data, only basic color processing).