A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converters

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This paper presents a high speed CMOS image sensor design targeting various industrial applications. Targetted for a 0.18 um CMOS process, the sensor captures frames at 1000fps at the target resolution of 5 Megapixel and supports rolling and global shutter modes. The sensor design has 4480, 14-bit column A/D converters, supporting a line rate of >2.2 million lines per second. Full digital CDS and an intrinsically gain-matched column parallel architecture allow the sensor to output a pattern- and artefact-free raw image. Targeted peak QE is >50%. A dark temporal noise of 5e- can be achieved over a FWC of 20ke- resulting in a dynamic range of 72dB. Typical visually disturbing column and row patterns are all targeted to be at least 3x below the noise floor in raw uncorrected images captured at 1000fps. In HDR mode, at half the frame rate, the linear DR will approach 80dB.

Until recently the highest speed, multi-gigapixel/s imagers being reported had analog outputs [1]. Gradually 8-bit and 10-bit A/D convertors were being integrated [2-4]. By the IISW in 2009, 12-bit A/D converters at pixel rates up to 2Gpx/s were reported [5], and [6] suggested frame rates of digital imagers would be fundamentally limited for various reasons. In 2011, many reported > 2 Gpx/s sensors [7-11]. In [8] 12-bit A/D converters were reported for 2Gpx/s and even 3.6Gpx/s in 10-bit mode. In [10] a 2000fps 1.3Mpx sensor was reported with 12-bit A/D converters but [12] was the first sensor to show 12-bit performance at a staggering 3.96Gpx/s pixel rate.

The sensor reported here will break the 5Gpx/s barrier and does so with 4480 oversampling 14-bit A/D converters on-chip, 2240 on each side of the array.

A dedicated protocol layer prepares the data for transmission over a 70 lanes LVDS interface with 1Gbps pairs. A distributed clock generation scheme ensures all A/D converters run perfectly synchronously to avoid artefacts.

In digital CDS mode, converting both Reset and Signal values takes around 900ns, allowing to reach >2.2 million lines per second. In analog CDS mode, conversion time can be reduced to 450ns only. At this point, however, column settling requirements limit the line rate at the current performance requirements and the I/O becomes a bottleneck.

The A/D is based on a 3rd order Delta-Sigma Modulator. A CIFF structure was selected for its excellent loop stability over an acceptable range. A single bit quantizer ensures calibration free linearity and minimizes the complexity of the digital filter. The gain and linearity of a delta sigma modulator have a very weak dependence on capacitor ratios and is therefore very well suited for imaging due to the inherent uniformity from column to column. The gain depends merely on the reference voltages which are shared between all converters and therefore, as in a ramp converter, are identical for each column.

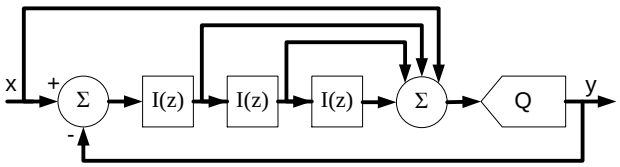

Figure 1: 3rd order CIFF modulator with 1-bit quantizer

A delta sigma modulator has the advantage of scaling very well for the ever higher word-resolution, demanded from industrial, cinematography and broadcasting applications, all in need of high speed accurate data conversion. In order to increase the resolution from 12-bit ENOB to 14-bit, it is sufficient to increase the oversampling ratio (OSR) from ~70 to ~120 for a third order modulator.

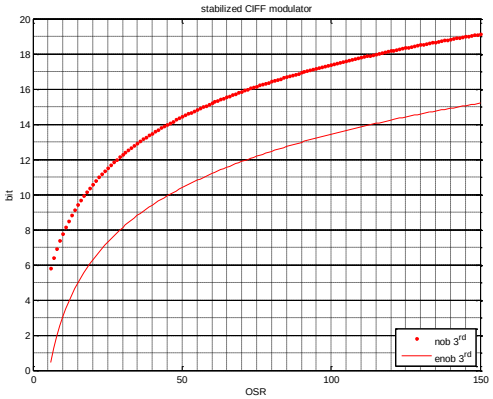

Figure 2: Raw resolution and effective number of bit (ENOB) vs. OSR for a third order modulator

Since any error on the references translates directly into an error in the conversion, the reference level settling is highly critical. The load of each reference signal depends on the analog levels being converted. Those levels in

turn depend on the actual scene. Incomplete settling would lead to various scene dependent artefacts (banding, ghosting, ...). As a result of this tough settling requirement, a trade-off has to be made between performance and extra power consumption in the reference buffers. Further design work will focus on methods to optimize this trade-off.

In order to maintain good uniformity in settling behaviour across the array, the reference voltage buffering is distributed. As this might lead to channel mismatches causing highly disturbing non-uniformity in the DC level, all distributed references are shorted. In support of various power down modes when reading smaller ROI, the connections between the various channels can be broken as shown in *Figure 3*.

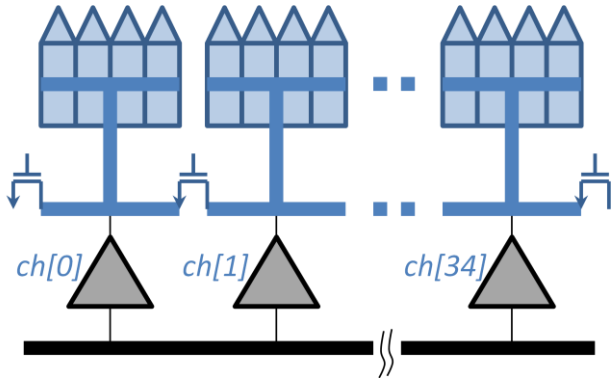

Figure 3: Distributed Reference Buffer Scheme

Column settling at these line rates is non-trivial, especially considering the total number of lines. In order to alleviate the line rate constraints, two column lines are foreseen for every pixel as shown in *Figure 4*

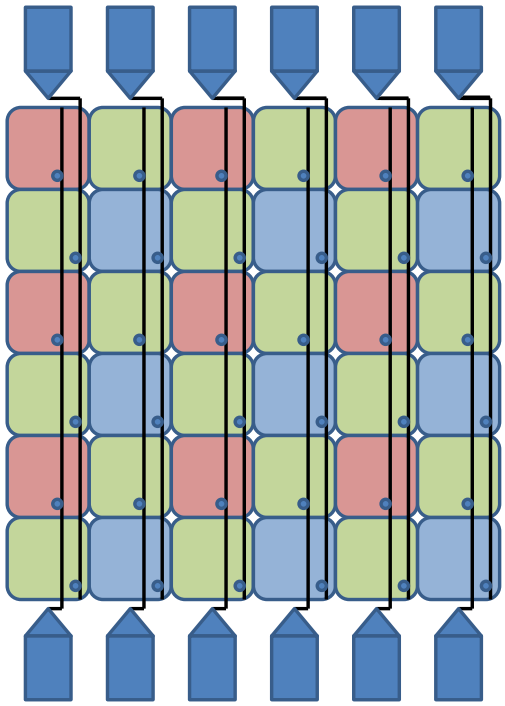

Figure 4: Dual Column Read-Out

At the line rates involved, however, the columns will not completely settle. Therefore, care must be taken that any memory effects are removed and that the cross-talk between neighbouring columns and crossing control signals is minimized. For this sensor a combination of careful shielding and memory removal through column discharge was applied.

Simulations show that column charging by the pixel SF column can best be performed without applying a current load in the column. This is preferred for several reasons:

- The pixel SF has more gain. This improves noise performance in e-.
- The pixel SF exhibits less noise itself, due to reduced bandwidth operation and because of the absence of the current load transistor.
- The output swing is higher due to a smaller Gate-Source voltage difference.
- The absence of a current source takes out a component that can introduce column-wise non-uniformity, both in DC and settling behaviour

In order to maintain maximum flexibility in pixel timing, a standard shift-register based addressing scheme is not suited. Therefore, a directly addressable pixel driver with line based memory elements was implemented as shown in *Figure 5*.

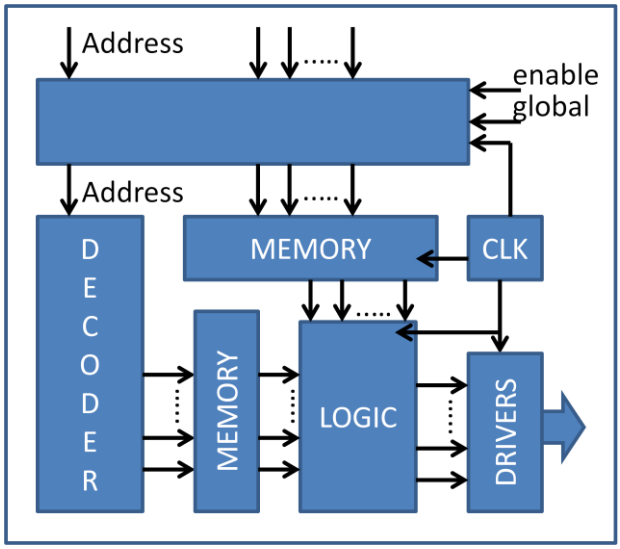

Figure 5: Directly Addressable Pixel Driver

This driver allows overlapping control of pixel operations at multiple line addresses. In order to maximize the speed of the control signals, drivers are placed on both sides of the array.

In nominal mode, the sensor will be able to capture 1000fps at full resolution. Other configurations of the array and data conversion allows capturing HD format images at more than 2000fps.

In global shutter mode, the Reset and Signal frames can be captured separately, such that, at half the frame rate, (limited only by the interface), rolling shutter noise

levels are achieved in global shutter mode by performing off-chip CDS using a frame-buffer. In this operating mode, HD movies at 1000fps can be achieved in global shutter with 5e- noise.

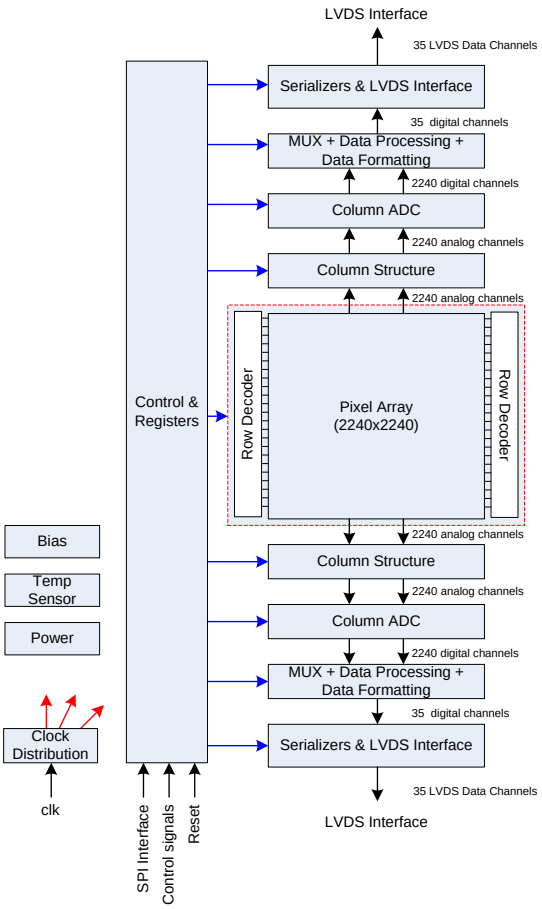

Figure 6: Sensor Block Diagram

Figure 7: Sample Artefact Free Raw Image

Table 1: key specifications

Parameter	**Value**	**Remark**
Pixel array	2240 x 2240	
Interface	Serial LVDS	
Frame Rate	1000fps	
Data Rate	70Gbps	
Main power supply	1.8 & 3.3 V	
Full well	20 ke$^-$	
Temporal noise	5 e-	
QE	>50%	@633nm
MTF	63%	@633nm
DR	72dB	Intra-scene
ADC resolution	14-bit	12-bit ENOB after rescaling

References

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