

High speed, backside illuminated 1024x1 line imager with charge domain frame store in Espros Photonic CMOS™ technology

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Abstract: In this paper, the performance figures of the Espros Photonics epc901 1024x1 line imager are presented. The epc901 is fabricated in the proprietary Espros Photonic CMOS™ Technology, and features back-side illumination (BSI) and charge domain frame stores (FS). This enables key benefits such as high quantum efficiency, especially in the NIR range and high speed read-out, with burst reads up to 500k lines/s. The effects of BSI on QE, fill factor, resolution and parasitic light sensitivity (PLS) are shown.

Key words: BSI, CCD-CMOS technology, line imager, frame store, QE, high-speed readout, NIR imaging

Introduction

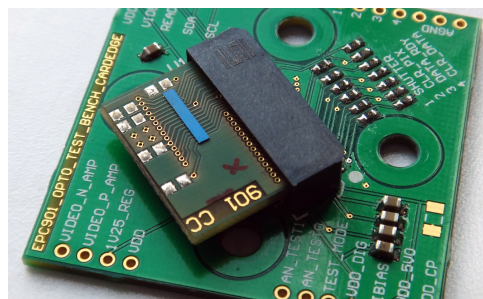
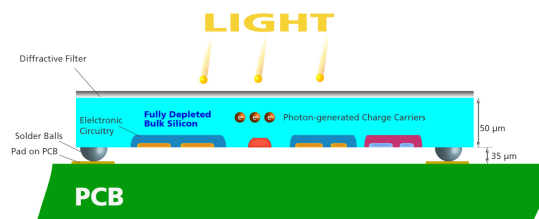
Espros Photonics has developed a dedicated IC process flow that is optimized for industrial imaging applications that commonly operate in the IR wavelength range[1]. The goal of this process concept is to enable high-performance imaging applications by targeting specific user requirements that are key to industrial imagers, such as timed imaging and high sensitivity in the IR range. The epc901 is one example of an implementation of this process flow, and it demonstrates the opportunities for other possible applications.

Process concept

The Espros Photonic CMOS™ process is based on a typical 150nm CMOS node. By adding dedicated process modules and choosing a specific wafer material, CCD structures, as well as BSI, are enabled. Special care has been taken not to compromise on the parameters of the baseline device portfolio. The process also features a very cost-efficient assembly technique suited for industrial-scale production of BSI devices. This is done via solder balling, enabling bare die flip-chip assembly directly on a PCB (Fig. [1]).

CMOS Device portfolio

The process includes both low-voltage (1.8V) and high-voltage (5V/12V) devices. The main devices that are available for design have been described in Ref. [1]. Due to the availability of three device classes, both logic control and analog driving and readout circuits can be implemented efficiently. The 12V devices are drain extended MOS devices (DE-devices), which are included in the process to enable switching of higher voltage levels common to CCD applications.



*Fig 1: top: concept of epc Photonic CMOS BSI
 below: epc901 on application board*

epc901 line imager architecture

The epc901 is a single line imager for industrial applications with a pixel pitch of 7.5μm and an effective pixel height of 120μm. The IC comprises a frame store in the charge domain, a 1024x1 MUX/CDS stage, an output buffer, as well as a I2C digital interface to configure the device (Fig. [2]). The output buffer has a 3dB frequency of 16MHz at 2V output swing. It can be operated with a readout clock frequency up to 55MHz, providing a line rate of 50klines/s. The external supply voltage is 2.5...3.3V, with a current of $I_{DD}=30\text{mA}$ (measured with a line rate of 1klines/s). The internal biasing, necessary for operation of the CCD and MUX/CDS block is provided by on-chip regulators and an on-chip charge pump. Acquisition and readout is controlled by a 5-pin digital interface.

Operation

To trigger the acquisition of a line, the SHUTTER signal is asserted. The integration period is defined by the time the shutter signal is high. After pulling down the shutter signal, the acquired charge packet is stored in the lowest empty frame store and the DATA_READY signal is asserted by the chip. Conversion of the charge to voltage by CDS of a line is initiated by a first pulse

on the READ signal. Subsequent pulses on the READ signal trigger the settling of the video output to the next valid pixel level.

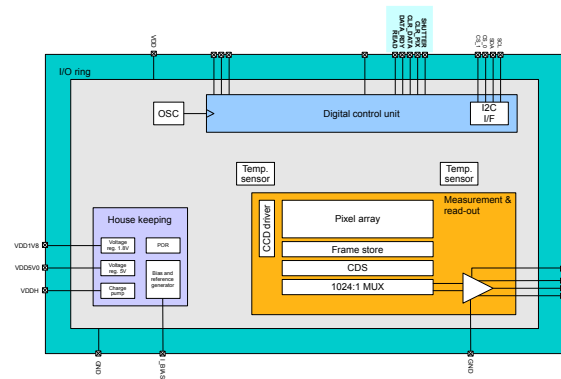


Fig 2: Block diagram of epc901 line imager

This concept provides a very simple interface to a data acquisition chain. The two other signals, CLR_PIX and CLR_DATA, are only used to initialize the imaging array and the FS, respectively.

Pixel and Frame store concept

The pixel array is organized as a CCD structure of subpixels to make fast charge transfers possible. The architecture of the pixel field is shown in Fig. [3]. The analog signals are multiplexed by a 1024x1 MUX to a single output buffer with programmable gain.

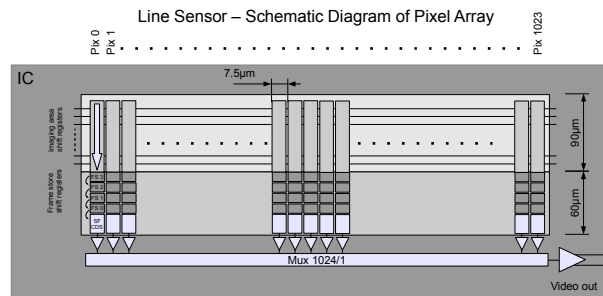


Fig 3: Block diagram of imaging array

Due to the availability of CCD structures in the technology, a bank of FS elements for all pixels in the charge domain is implemented. The design enables the storage of up to 4 lines. The FS can be operated asynchronous to the acquisition of new lines and acts like a FIFO register. That means it is possible to trigger the acquisition of a new line independent of the state of the FS, provided that an empty FS line is available. Overflow of the FS is avoided by ignoring shutter signals when no empty line is available.

Readout can be triggered independent and asynchronous to the line acquisition. An illustration of the operation is shown in Fig. [4]. Control of the internal CCD operation and frame store elements are handled on-chip by the digital engine in the IC, so no external sequencer or FPGA is required.

The analog device portfolio is used to provide on-chip CCD gate drivers. Therefore, no external high-voltage driver circuits are necessary. This makes the integration of the device into a system extremely simple.

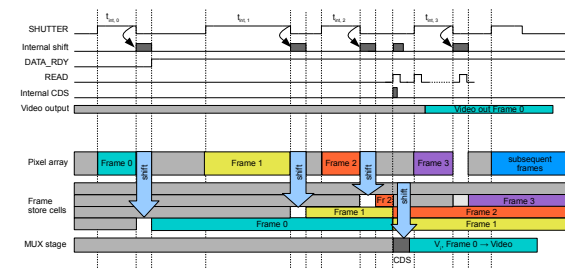


Fig 4: Simplified operation of FS and read-out. Note the asynchronous read operation after frame 2

Performance figures

Despite the column-wise readout, Fixed pattern noise (FPN) is better than 3%. The Charge to voltage conversion factor (CVF) was designed to be 5µV/e-, based on the requirement specifications. The noise level of the system is 1mV rms at the full bandwidth of 16MHz

QE and fill factor

The technology concept makes it possible to achieve a high QE over a broad range of wavelengths reaching into the NIR (see also Ref. [2]).

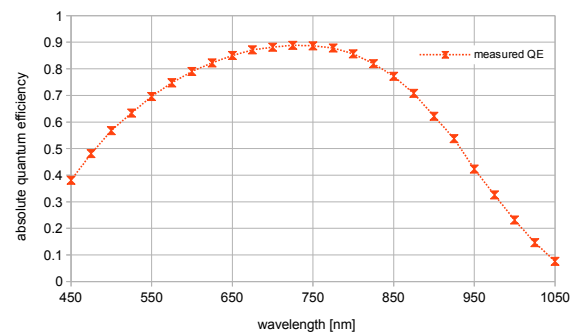


Fig 5: measured external QE for epc901 line sensor. The AR coating is optimized for NIR

Based on the requirements, the backside processing and coating was optimized for the NIR range. The measured QE is shown in Fig. [5], indicating values larger than 50% from 470nm up to 930nm. Note that no interference patterns are visible because the entrance layer on the backside is very thin. No microlenses are needed to achieve this result, facilitating fabrication. Due to BSI, a high fill-factor is expected. Indeed, we can show that even the areas under the channel stops are fully sensitive to light. This was demonstrated using a measurement setup in which a point-spread function (PSF) is shifted laterally across the pixels. The result is shown in

Fig. [6], where the signals and the sum of several adjacent pixels are plotted against the position of the PSF centroid. If there were gaps of lower sensitivity, the summing curve would show characteristic drops at the edges of the pixels. Obviously, no such drops are observed.

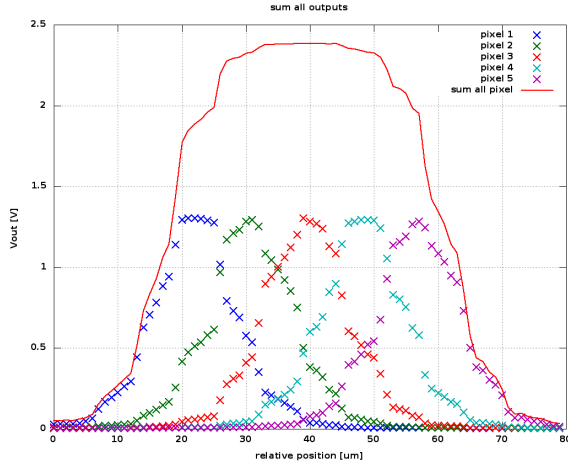


Fig 6: scanning a PSF across several pixels results in no drop in recorded intensity, demonstrating 100% fill factor

Cross-talk

In order to achieve a high QE in the NIR range, the sensitive layer of the device is approx. 50 μm thick, which results in a geometrical aspect ratio (height of sensitive layer/pixel pitch) of the pixels of nearly 7.

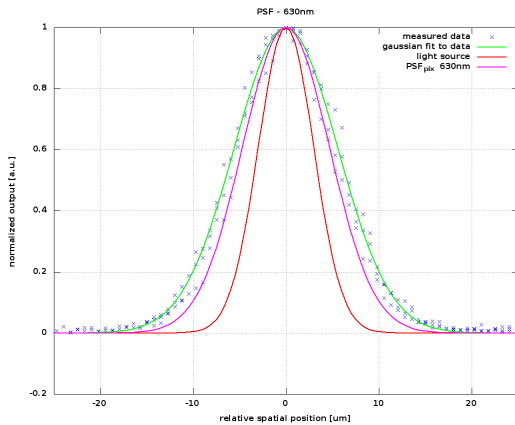


Fig 7: spatial resolution of line sensor for $\lambda=630\text{nm}$: The data-points are achieved by spatial oversampling. The measured width is 5.5 μm , the deconvolved width is 4.7 μm

Typically such a configuration bears the risk of poor spatial resolution due to diffusion of the charge carriers. In order to estimate the spatial resolution of the sensor, the epc901 was illuminated with a diffraction limited PSF. The width (sigma of Gaussian fit) of the source PSF was characterized with a commercial image sensor

with 1.75 μm pitch and was determined to be 3.0 μm . The effective contribution by the sensor was then analyzed by deconvolution of the measured spatial output with the known source PSF, (Fig. [7]). This was repeated for six different wavelengths from 400nm to 850nm.

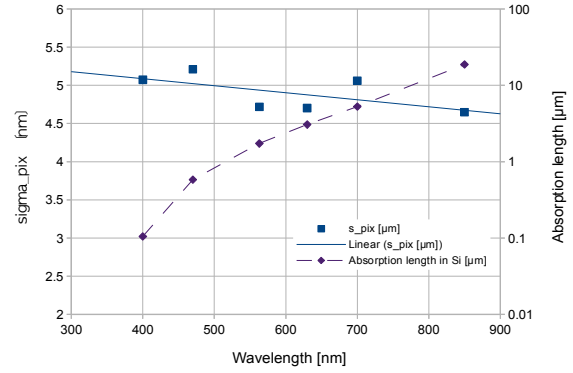


Fig 8: measured spatial distribution by pixel (left axis) vs. absorption length (right axis). Note the log scale for the absorption length.

The resulting spacial redistribution (σ_{pix}) by the sensor is better than 5.5 μm over the full wavelength range, (Fig. [8]). For comparison, the absorption length is included in the plot. Note the wide range of absorption depth over which this performance is achieved.

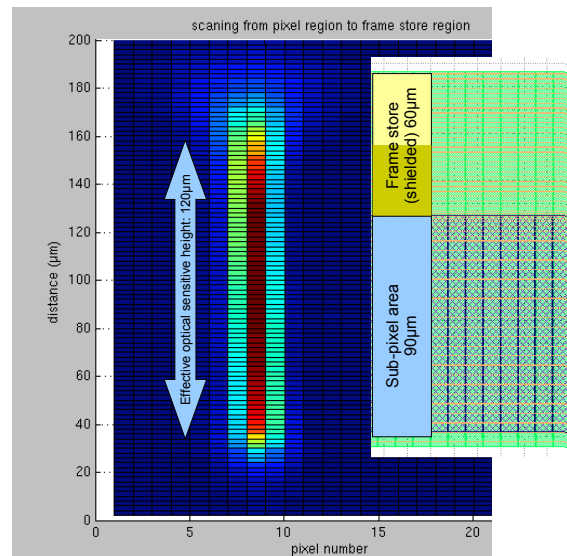


Fig 8: Intensity plot when a PSF is scanned vertically across a pixel column; vertical axis: travel distance of the light source.

The pixel redistribution σ_{pix} even improves slightly for longer wavelengths. We assume that this is due to the fact that the photons penetrate deeper into the silicon, and thus the travel distance to the CCD collection well is therefore shorter, causing less diffusion. As a

consequence we can combine good spatial resolution with high QE in the NIR wavelength range.

Sensitive area

The FS area is protected from collecting directly incident photons. Photoelectrons that are created underneath the FS area are directed into the CCD collection well. In order to prove this and verify if the spacial resolution suffers, a point light source was scanned in the (vertical) column direction across the pixel field. The response of the nearby pixels is plotted in Fig. [8]. The effective pixel height (vertical extension) is determined to be $120\mu\text{m}$. Notably there is practically no additional spread of the charge packets if light is absorbed under the FS.

Parasitic light sensitivity (PLS)

It is important to investigate if incident photons have an influence on the charge in covered FS elements, which would result in temporal crosstalk. In order to prove a good temporal separation, the FS was operated according to the listing in the Table [1]:

Step	Illumination	epc901
1: 2ms t _{shutter}	Off	Take frame 1 (empty)
2: 2ms t _{shutter}	On, variable LED time, $\lambda=630\text{nm}$	Take frame 2 (with signal)
3: 2ms t _{shutter}	Off	Take frame 3 (empty)
4: 2ms t _{shutter}	Off	Take frame 4 (empty)
5, 6, 7, 8: 1ms x 4	Off	read out all 4 Frames

Table 1: operation sequence for PLS

First, an empty frame 1 is acquired in step 1. During step 2, a flat-field LED illumination ($\lambda=630\text{nm}$) was used to expose a wide area of the chip, including both the active pixels and the frame store holding charge from frame 1. The illumination energy was varied simply by changing the pulse duration of the LED. The power of the LED was chosen such that signal saturation (SS) in frame 2 was reached for $t_{\text{LED}} = 100\mu\text{s}$. The subsequent frames were again taken without illumination. Note that the shutter time was kept constant at 2ms in order not to change charge transfer. After acquisition of four consecutive frames, the full FS is read out with 1MSa/s pixel clock frequency. The resulting data is shown in Fig. [9]. Obviously the signal in frame 2 rises

linearly until saturation is reached at $100\mu\text{s}$. By then, none of the adjacent frames have a measurable deviation from the noise offset level. The first effect is lag in the trailing frame 3, which becomes noticeable at about $2\times\text{SS}$. At $4\times\text{SS}$, the full well limit of the FS element is

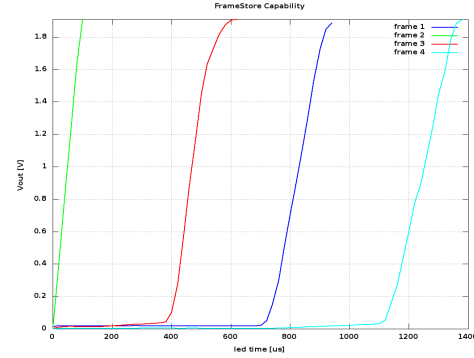


Fig 9: signal in frames under increasing illumination of frame 2. Full well is reached at $t_{\text{LED}}=100\mu\text{s}$

reached and spill-over happens. Even then, the signal in the leading empty frame 1 is still comparable to the noise level. Only at a level of $7\times\text{SS}$ does spill-over occur to frame 1. Therefore, the influence of PLS can be excluded up to $7\times\text{SS}$.

Conclusion:

We have demonstrated the key performance parameters of a novel type of CCD/CMOS line sensor which has excellent properties in the NIR range. Due to the high integration, cost efficient systems can be built. The performance of the charge domain FS was investigated and the concept is verified to work well under the required conditions. The sensor is therefore ideally suited for machine vision or spectroscopy applications. The concept is straightforward to extend to include efficient anti-blooming or TDI for other applications.

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