Ultra-high speed imaging at megaframes per second with a megapixel CMOS image sensor.

J. Crooks[a], B. Marsh[a], R. Turchetta[a], K. Taylor[b], W. Chan[b], A. Lahav[c], A. Fenigstein[c]
[a]STFC Rutherford Appleton Laboratory, Didcot, Oxfordshire, UK
[b]Specialised Imaging, Unit 32, Silk Mill Ind. Est. Brook Street, Tring, Hertfordshire, UK
[c]TowerJazz Semiconductor Ltd, P.O.Box 619, Migdal Haemek, Israel

Thanks to the continuous improvement in CMOS sensor design, pixel rates around or in excess of 10 Gpixel/sec are currently achieved by a few sensors (Figure 1). Recently a new approach [1], based on a bank of capacitive memories located on-chip on the side of the pixel array, has gone beyond the limit of Tpixel/sec in burst mode. In this paper, we present a highly scalable approach that also achieves pixel rate in excess of 10^{12} pixel/sec. Designed for generic use in ultra-high speed imaging, this sensor, called Kirana [2], works by storing 180 consecutive frames in each pixel at a speed of up to 5 Mframe/sec. This approach is similar to that found in some existing CCD sensors [3][4]. Here we will present the imager design and its performance, while technical details of the CCD-in-CMOS technology are more thoroughly discussed in [5].#

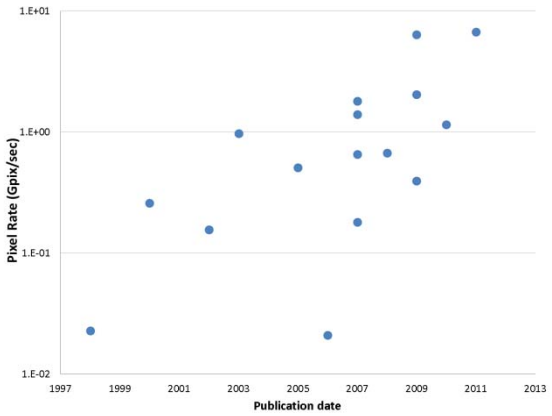

Figure 1: Survey of recent publications: pixel rate vs publication date

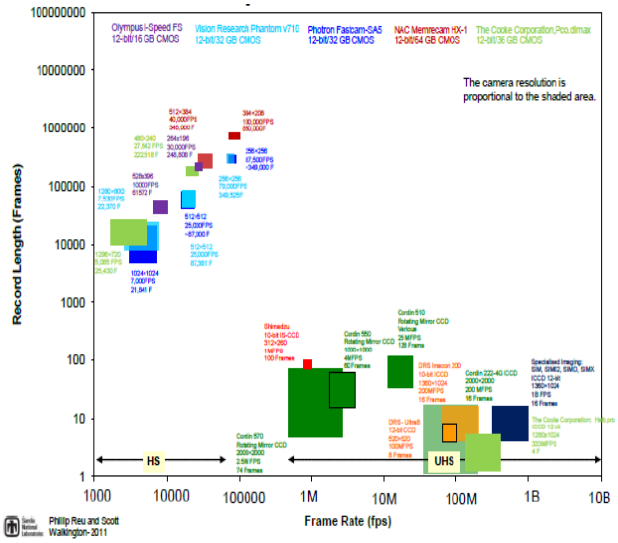

Figure 2: Summary of recent devices: record length vs frame rate & imager size

As can be seen from Figure 2, in ultra-high speed imaging there is a clear need for high resolution, megaframe-per-second sensors with a decent record length. It is this gap that our Kirana sensor aims to fill. It has 924x768 pixels for a total of 0.7 Mpixels, and a format optimised for use with standard 35mm optics. It also matches well the size of the reticle in the chosen technology.

CMOS TECHNOLOGY

The Kirana sensor (shown in figure 4) was designed and manufactured in 0.18 micron CMOS imaging technology, utilising a 5V transistor option which is beneficial for the operation of the CCD cells: In order to increase the flexibility of operation, we designed on-chip CCD drivers with four-level outputs that are able to work with negative voltages as well as with voltages exceeding the maximum rated voltage of the technology.

High speed burst-mode imaging is achieved by means of integrated CCD cells in a 2-dimensional memory bank. Figure 1 shows the layout of vertical and lateral 3-phase CCD registers between the more conventional pinned photodiode and a floating diffusion/source follower output node. The manufacture of CCD cells in CMOS technology is discussed in greater detail in [2], [5].

During burst-mode operation, the vertical register acquires 10 frames at the burst-mode frame-rate (i.e. minimum 100ns per frame) then they are transferred in parallel to the first lateral register. The lateral register therefore operates at $1/10^{th}$ the burst rate (i.e. minimum 1us). In order to maintain contiguous frames of equal length, every 10^{th} transfer from diode to CCD also includes the transfer to lateral register in the same time period. During continuous-mode operation, the signal charge may be swiftly transferred through to the output node for readout, since storage of intermediate frames is not

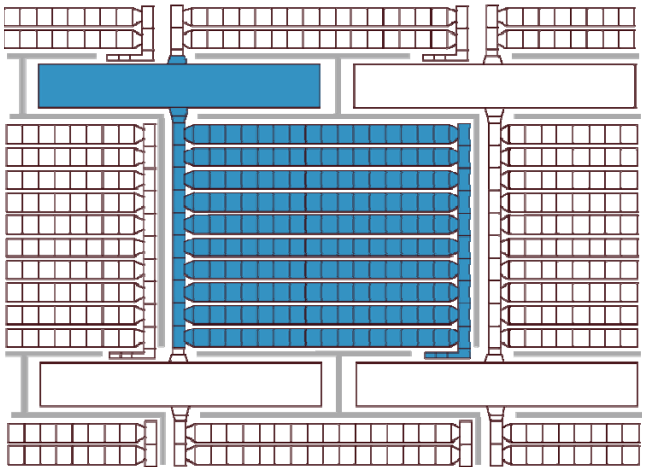

Figure 3: The layout of a single Kirana pixel is highlighted within the regular array

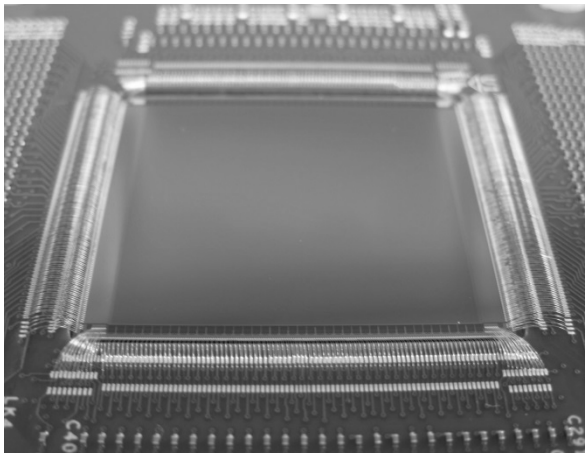

Figure 4: Photograph of Kirana sensor mounted on printed circuit board

necessary.

PIXEL ARRAY READOUT

The pixel array is divided into two halves, so the sensor is read out on both sides in parallel. 84 differential analogue output channels work at a maximum rate of 10Msamples/sec to achieve a maximum pixel read-rate of 840Mpixel/sec. This allows a full 180-frame sequence to be read in 152 milliseconds, or a sustained frame rate of 1,180 fps at full sensor resolution. A number of array subsections may be deactivated to achieve higher frame rates at a proportionally reduced image resolution.

The pixel array is operated in global shutter mode: all pixels receive the same control signals to initiate diode and CCD transfers. During readout, the vertical exit register is operated in a rolling mode, such that only the active (addressed) row initiates a reset of the floating diffusion (FD) node, followed by a vertical transfer of charge onto the FD node. This allows correlated double sampling (CDS) for low noise operation. All other rows hold their frame data in the vertical register until addressed. The column readout circuits include 1pF sample capacitors for reset and signal sample. This circuit is then duplicated for ping-pong (pipelined) operation to maximise output bandwidth. Four rows of pixels are addressed simultaneously, via 4 vertical read lines in each pixel column to further reduce read time. The four rows from each 22 columns are multiplexed to a differential output amplifier pair at 10 Mhz, thus making up the 42 analogue outputs per side. In the future, the design may be stitched in the x direction only to achieve 1Mpixel resolution in a 16:9 image format, which corresponds to 64 analogue output channels per side.

IMAGING PERFORMANCE

The sensor gain was measured to be 80 uV/e- with a noise level below 10 e- and a full well in excess of 11,000 e-, thus giving a dynamic range beyond 10 bits. The diode is fully pinned and designed with a graded doping improve transfer speed. The fill factor is just over 10 % but we are designing microlenses that will allow recovery of most of this. Full sensor performance measurements are presented in table 1.#

Parameter	Unit	Value
Pixel pitch (X)	um	30
Pixel pitch (Y)	um	30
Pixel format (X)		924
Pixel format (Y)		768
Number of pixels		709,632
Frame rate (burst mode)	fps	5,000,000
Frame rate (continuous mode)	fps	1,180
Pixel rate (burst mode)	Pixel/sec	3.54 T
Pixel rate (continuous mode)	Pixel/sec	0.84 G

Parameter	Unit	Value
Noise	e- rms	<10
Full well capacity	e-	11,700
Camera gain	µV/e-	80
Dynamic range		>1,170
	dB	61.4
	bit	10.2
Fill Factor	%	11
Quantum efficiency (Without microlenses)	% @ 430 nm % @ 540 nm % @ 635 nm % @ 850 nm	2.05 2.13 1.51 0.38

Table 1: Summary of the main Kirana parameters

A contrast transfer function method was used to evaluate spatial resolution: a test chart image (as shown in Figure 5) was used in two orientations to evaluate line-pair/mm resolution. The geometry and spacing of the diodes (as seen in figure 3) means we expect different spatial resolution in the two axes. A second technique, obtained from the Fourier transform of a diagonal knife-edge under blue (470nm) illumination was also tried. Preliminary results from both methods and comparison with the Nyquist limit are presented in table 2 for the x and y directions.

Direction of measurement	Resolution (Nyquist)	Resolution (test chart) (MTF 10%)	Resolution (knife edge) (MTF 10%)
Horizontal	16.6 lp/mm	11 lp/mm	10 lp/mm
Vertical	16.6 lp/mm	10 lp/mm	11.4 lp/mm

Table 2: Preliminary results on spatial frequency

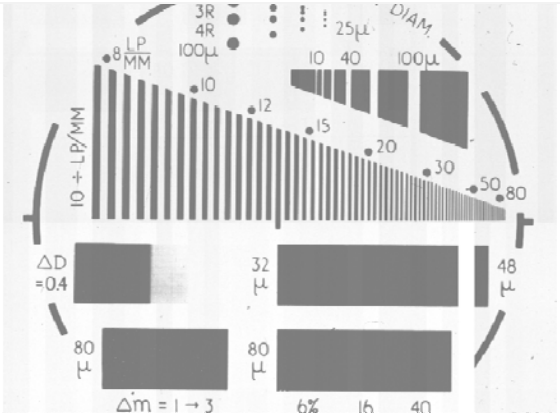

Figure 5: Horizontal test chart image acquired with Kirana sensor

Figure 6. The camera commercialized by Specialised Imaging, UK

SAMPLE IMAGES AT 5MHZ

Sample frames are shown below (Figure 7) from a high-speed video taken with the Kirana camera, also shown. The images show the progress of an ink-jet taken at 5 million fps.

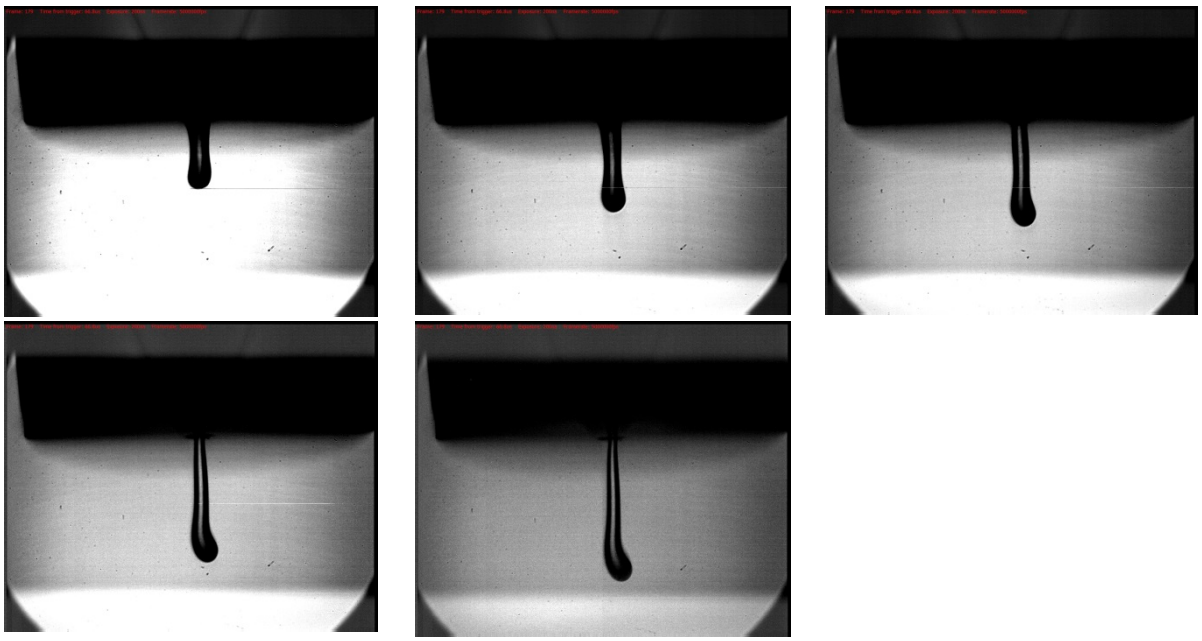

Figure 7: Sample frames from high-speed video of an ink jet, acquired at 5 million frame/sec

CONCLUSION

In this paper we have presented the novel prototype imager for ultra-high speed imaging: "Kirana". The sensor was manufactured in a 180 nm CMOS Image Sensor process, and comprises 0.7 million pixels, each containing 180 CCD memory cells for high frame-rate acquisition. We have demonstrated this architecture is capable of capturing a burst of 180 images at 5 million frames per second. The imager may also be used as a high-speed video sensor, supporting continuous operation at 1,180 frames per second. The prototype sensor is currently under evaluation in a dedicated high speed camera system (Figure 6) by Specialised Imaging [1] to fully exercise this new technology in key applications in the ultra-high-speed field.

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