A CMOS Image Sensor for In-Pixel Background Suppression and Frequency and Phase Detection for Structured Light 3-D Acquisition Systems

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Abstract—

We designed and demonstrated the operation of a CMOS image sensor for modulated light detection and frequency and phase detection. These two quantities can be used to code the angular information in an active 3-D acquisition method based on structured light. Each pixel is equipped with a pulse-frequency modulator (PFM) [1] and two up/down counters in order to perform frequency and phase calculation in pixel parallel. The sensor is also capable of obtaining gray scale images by turning off the phase calculation. The sensor is fabricated in 65nm standard CMOS. A 45×30 array of 28μ m×37 μ m pixels is integrated on a 2 mm×2 mm die. The measurement results show signalto-background ratio (SBR= $10 \log(\text{signal/background})$) of -5.5dB at the frame rate of 10 fps, and maximally -21dB at slower rate. We have demonstrated the demodulated 2-D image, the results of distance measurement with range accuracy of 0.68cm at the average distance 18-24cm and reconstructed shape using this sensor.

I. INTRODUCTION

Among many 3-D acquisition methods, structured light is a popular one due to its high precision and robustness [2]. Structured light is similar to stereo matching. The main difference is that in structured light systems, one of the camera is replaced by a projector that projects a known pattern of light onto an object, and a camera takes an image of the pattern reflected on the surface of the object. Since the pattern contains sufficient information to reconstruct the 3-D image, by processing the camera image of the projected pattern the 3-D shape of the surface can be reconstructed. The angular information is encoded in temporal or spatial variation of physical quantity such as light intensity or colors at each point of the projected pattern.

Modulated pattern projection has several advantages for structured light systems: an ability to distinguish itself from ambient light in the frequency domain, and two new dimensions to encode the information, namely the frequency and the phase (Fig. 1). The drawback of modulation is that multiple images are required in order to extract the projected pattern and calculate the frequency and phase, thus overall speed is degraded by the factor of the number of images required for this operation.

In this work we will present a new CMOS image sensor for in-pixel frequency and phase detection. In contrast to the conventional method where many frames must be read from the sensor in order to calculate the frequency and phase of the input light, our sensor can eliminate this necessity by calculating these quantities within each pixel.

II. SENSOR DESIGN

In this section we describe the design and operation of the image sensor specialized for modulated light detection and the frequency and phase extraction in detail.

As shown in Fig. 2, our proposed sensor is consists of two components: pixel array and readout circuit. Each pixel in the array has a demodulation circuit that detects the modulated light and extracts the frequency and phase information.

The pixel consists of a photodiode (n-well/p-sub), a pulse frequency modulator (PFM), two 20-bit up/down counters and tristate buffers that are connected to the two 20-bit columnwise-shared digital readout lines. The STOP signal, counter RST signal and two up/down control signals, UD1 and UD2, are shared over the entire array while RE are independent per each row.

Figure 4 shows the diagram of each node in the pixel. The PFM circuit outputs pulse train with frequency proportional to the intensity of incident light. Two counters are used for frequency and phase calculation as shown in the Fig. 4 (d) & (f). These counters have independent up/down control signal, enabling detection of up to two frequencies. In frequency detection operation, UD1 and UD2 are toggled at two different

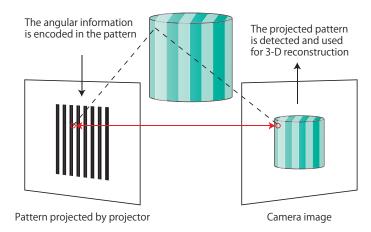


Fig. 1. Concept of structured light

TABLE I SUMMARY OF SPECIFICATION AND MEASUREMENT RESULTS

Design parameters	Values
Pixel area	30um x 37um
Photodiode	N well / P sub
Photodiode area	3.2um x 30um
Process	65nm Standard CMOS
Meas. Results	Values
Meas. Results SBR at 10fps	Values -5.5dB
SBR at 10fps	-5.5dB

frequencies so that the phase can be obtained by inverse tangent of the ratio of the two counter values. In phase detection operations, UD1 and UD2 are toggled at the same frequency but 90 degree out of phase, so that the final counter value can be considered as a complex number, whose argument represents the phase. Gray scale image is obtained using one counter with UD signal tied to 0.

The image sensor is controlled in a global shutter operation by counter RST signal and the STOP signal. All the pixels receive the same control signal (except for RE) and perform the operation described above in parallel.

The readout circuit is just a simple shift register that transfers column data from the shared digital readout lines to off the chip.

The chip specifications are summarized in table I. The chip photograph is shown in Fig. 5, 6. Note that counters are embedded into the pixel for scalability of pixel array this time, still they can be located off the pixel array for better uniformity of pixel layout [3].

III. MEASUREMENT RESULTS

First we measured the performance of the pulse frequency modulator by illuminating the sensor using an white high-power LED (32.8W, 3000K). The result shows that the dynamic range is at least 33 dB which is limited by the maximum current of LED.

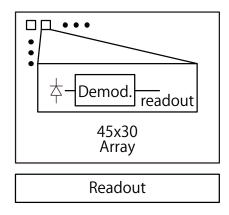


Fig. 2. Sensor architecture

Next, we set up the measurement system for 3-D image acquisition. The measurement system consists of a DLP Discovery 4100 Development Kit with ViALUX ALP-4.1 high speed [4] [5] to project modulated patterns, our proposed image sensor and controller FPGA board, the target object, and the white high-power LED to produce artificial large background light(Fig. 8).

All the control signals are generated by the FPGA. The readout signal is also connected to the FPGA, which in turn transfers the data to PC.

Patterns projected by the DMD projector is a modulated time-multiplexed stripe pattern generated on the PC. The DMD projector is synchronized to the trigger signal generated by FPGA. Therefore the FPGA can control both the timing of the projected pattern and the control signal, which is necessary for the proper phase detection.

The gray scale image of a wooden turtle (Fig. 9) under large background light and weak signal light (SBR of -5.5 dB) obtained by the proposed sensor is shown in Fig. 10. The result of phase-detection using binary phased projection is shown in Fig. 11 The color represents the phase, where red and blue represents 0 and 180 degree respectively.

We measured the 3-D distance of a plane to evaluate the accuracy of the 3-D acquisition. The demodulated 2-D pattern is shown in Fig. 12, and the ideal versus measured distance in Fig. 13. Average error of distance is 0.68cm cm. Another reconstructed 3-D image of a plane with 1cm step is shown in Fig. 14.

IV. CONCLUSION

We have demonstrated a CMOS image sensor with in-pixel background suppression, frequency and phase detection using pulse-frequency modulation and in-pixel counters. The best background suppression performance was $-5.5 \mathrm{dB}$ at 10fps, and $-21 \mathrm{dB}$ at slower rate. The ability to reconstruct the 3-D from the pattern is also demonstrated and its performance is evaluated.

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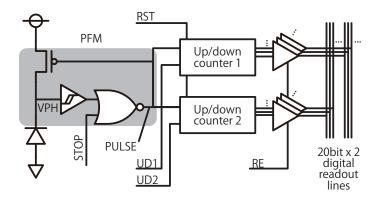


Fig. 3. Pixel schematic

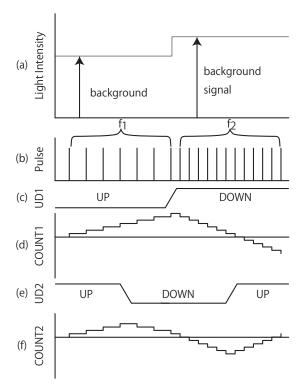


Fig. 4. Operation of the in-pixel circuit

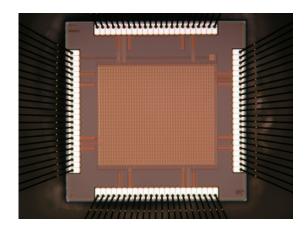


Fig. 5. Chip photograph

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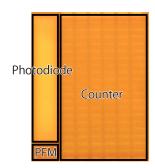


Fig. 6. Pixel photograph

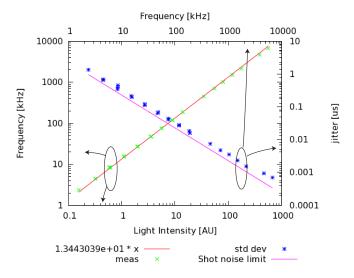


Fig. 7. The sensitivity and jitter of PFM circuit

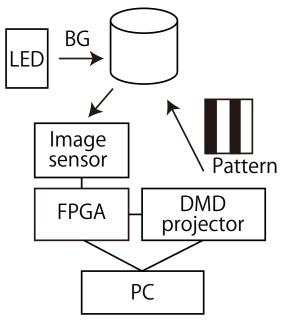


Fig. 8. Measurement setup



Fig. 9. Target object



Fig. 10. Gray scale image taken by the sensor

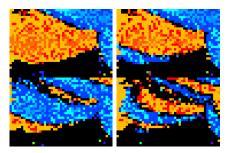


Fig. 11. Detection of stripes (red: 0 degree, blue: 180 degree) under signal-to-background ratio of $-5.5 \rm dB$

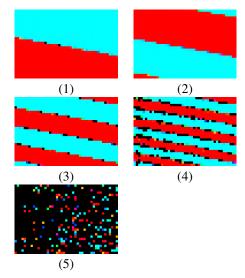


Fig. 12. Detection of stripes for a plane

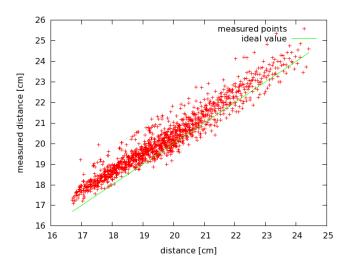


Fig. 13. The accuracy of the distance measurement

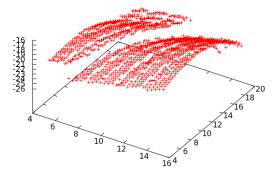


Fig. 14. Reconstructed 3-D image of 1cm step