A 1.1e$^-_{rms}$ temporal noise 87.5dB DR CMOS image sensors with low-noise transistors and column-parallel ADCs

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I. Introduction

In scientific imaging applications, the low-noise [1], [2] and the wide dynamic range imagers [3]-[7] are favored for their ability to distinguish low contrast signal from high back ground illumination and to reconstruct an image that covers a wide illumination range from various light emitting objects. The 1/f noise of in-pixel amplifiers is a dominant noise at low frequencies. Under the low-illumination conditions, the temporal noise is determined by 1/f noise and random telegraph signal (RTS) noise because these noises are very difficult to eliminate. One of solutions for reducing these noises is to use a buried-channel transistor [8]. If the imperfection for gate oxide has to be accepted, the alternative will have to take the conducting carriers away from the Si-SiO_2 interface. However, the additional process is inevitable to make the buried-channel under the ordinary pixel structure. A high conversion gain is also enabled to lower the readout noise and achieve excellent image capturing performance at the low light intensity.

In this paper, a new type of the pixel structure with the low-noise transistor such as a native transistor is developed for wide dynamic range (WDR) CMOS imager. And extra-ordinary pixel structure, which is to optimize the floating diffusion (FD) node capacitance in the pixel for high conversion gain (HCG) CMOS imager, is also introduced and demonstrated with video rate operation.

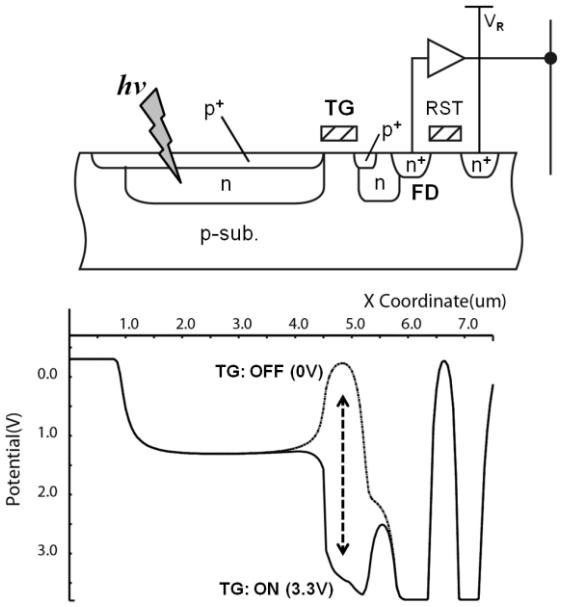


Figure 1: Proposed pixel structure and its potential distribution for HCG imager.

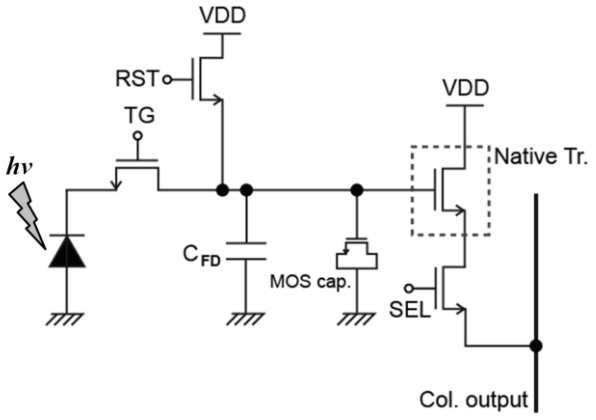


Figure 2: Schematic diagram for WDR imager.

II. Architecture of imagers

An active pixel includes a photodiode formed in a semiconductor substrate. A transfer transistor is formed between the photodiode (PD) and the FD and selectively operative to transfer a signal from the photodiode to the FD node. Generally, the FD is formed from an n-type implant, and the conversion gain is controlled by the FD node capacitance.

Fig. 1 shows the cross-sectional structure and the potential diagram of the proposed pixel structure for achieving high conversion gain. As putting a fully depleted diode structure between the transfer gate (TG) and the FD, the coupling

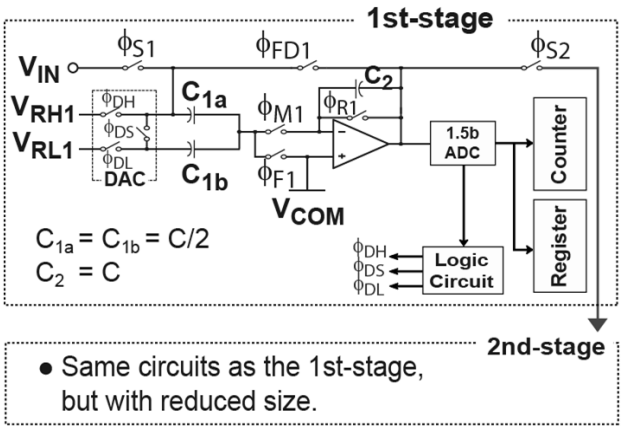


Figure 3: Schematic diagram of the column readout circuit using folding-integration/cyclic ADC.

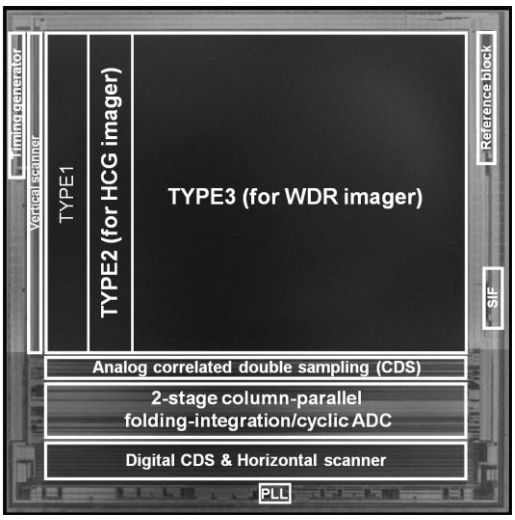


Figure 4: Chip micrograph of the prototype imager.

capacitance which is generated between the TG and the FD is minimized, because the proposed pixel structure allows us to separate interface of two components. As a result, high conversion gain is achieved by the minimized FD node capacitance and the noise performance is improved by removing one of noise sources from power supply.

A schematic diagram of the proposed pixel structure with the native transistor for achieving the wide dynamic range and low noise is illustrated in Fig. 2. An extra capacitor is added to the FD node for expanding the dynamic range by decreasing the conversion gain on purpose. Simultaneously, the proposed pixel structure has a small occurrence of the number of noisy pixels due to the 1/f noise (or RTS noise) because of the native transistor used in the pixel source follower amplifier. The HCG and WDR imagers are based on a high performance column-parallel folding-integration/cyclic ADC [9], [10] which is illustrated in Fig. 3.

III. Measurement results

A CMOS image sensor with two-type special pixels for obtaining high conversion gain and wide dynamic range is implemented with 0.18-μm standard CMOS technology. The die micrograph of the fabricated sensor chip is shown in Fig. 4.

The whole pixel array consists of three-type imagers and each pixel array has its own distinct characteristics. Among them, type 2 and type 3 are for the HCG and WDR imagers, respectively. Fig. 5 shows the measured noise performance of the HCG imager. A very low temporal noise of

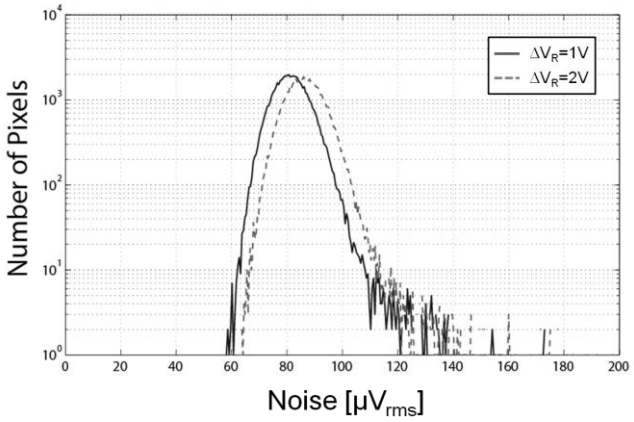


Figure 5: Measured noise histogram of HCG imager.

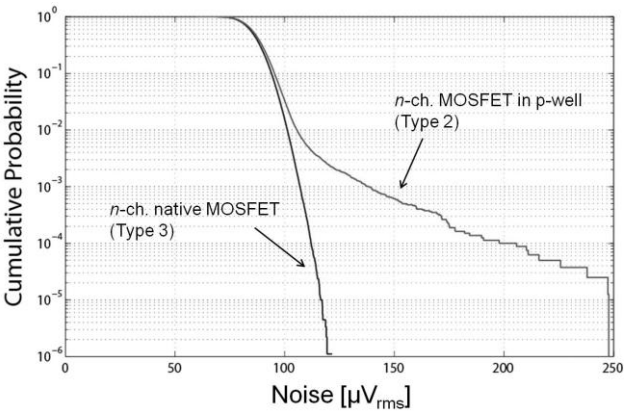


Figure 6: Comparison of noise characteristic between WDR and HCG imagers (@ ΔV_R=2.0 V).

1.1e$^-_{rms}$ (80.5μV_{rms}) is obtained with the sampling number M=32 and ADC reference voltage ΔV_R=1.0 V. Fig. 6 shows the comparison of noise characteristic with n-ch. native MOSFET and n-ch. MOSFET in p-well as an in-pixel source

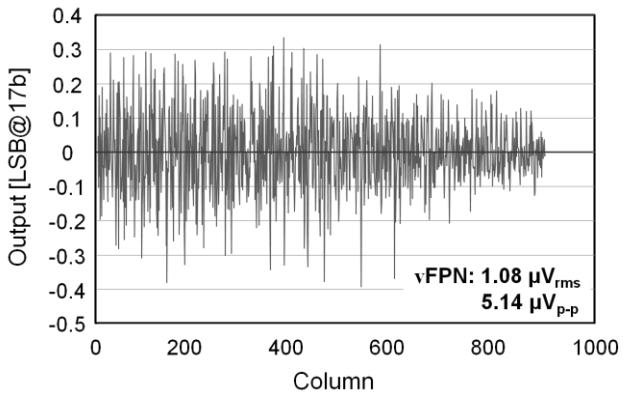
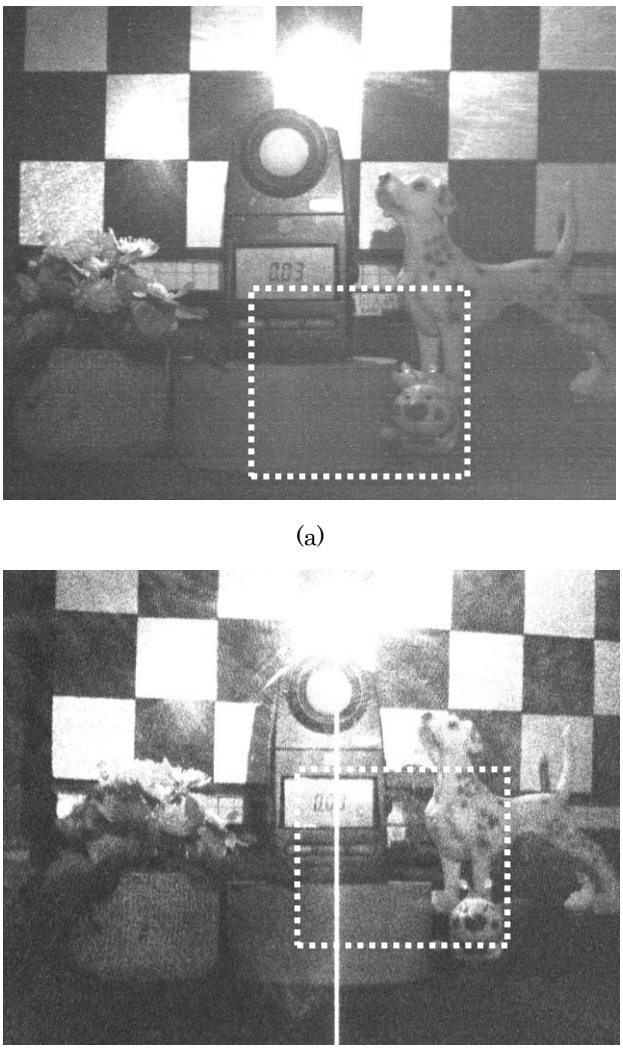


Figure 7: Column-wise plot of the measured vFPN of WDR imager (Type 3).

follower amplifier at M=32 and ΔV_R=2.0 V. As shown in this measurement result, the RTS noise (or 1/f noise) is dramatically decreased by the effect of used native transistor in comparison with that of HCG imager which is used the n-channel MOSFET in the p-well as an in-pixel amplifier. In addition, a very wide intra-scene dynamic range of 87.5 dB is obtained, although the measured noise level is increased in this case (3.7 e^-_{rms}, median at ΔV_R=2.0 V) because of the low conversion gain. Fig. 7 shows the measurement result of the vFPN of the WDR imager. Extremely low vFPN is achieved by the hybrid CDS and high-resolution ADC of 17 bits. And the n-ch. native transistor which uses as an in-pixel amplifier also helps to achieve the very low vFPN because it has good linearity. The measured vFPN under the dark condition is 1.08-μV_{rms} and 5.14-μV_{p-p}.

Fig. 8 shows the captured images in the prototype WDR imager [Fig. 8(a)] and the conventional electron multiplying (EM) charge coupled device (CCD) [Fig. 8(b)]. The EM-CCD is specialized for observing the dark scene due to low noise characteristic. However, the dynamic range is a narrow compared with the proposed WDR imager, relatively. For the comparison of their dynamic range, the center of the subjects was illuminated by very intense light. Fig. 9 shows the enlarged images of the dotted line part shown in Fig. 8(a) and Fig. 8(b). Unlike the EM-CCD (TC285SPD), the proposed imager which has wide dynamic range of 87.5 dB represents the targeted objects without the loss of the information at the dark and the bright area.



(a)

(b)

Figure 8: Comparison of captured images between the WDR imager [fig. (a)] and the EM-CCD [fig. (b)].

(a) (b)

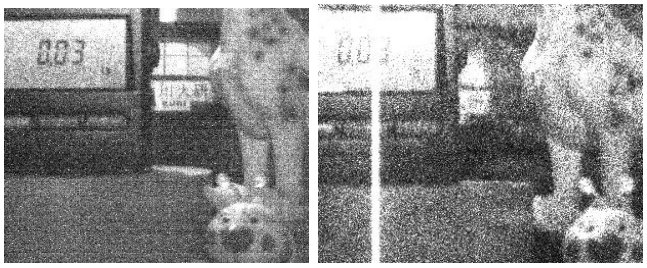


Figure 9: Enlarged results of the dotted line part shown in Fig. 8. (a) WDR imager. (b) EM-CCD.

The performance summary is shown in Table I. The pixel-type of HCG and WDR imagers are a 4-transistor pinned photodiode active pixel. And the implemented HCG and WDR imagers have the pixel conversion gain of 73.2-μV/e- and

Parameter	Value
Technology	0.18 μm 1P4M CIS process
Total area	12.0 (H) mm X 12.0 (V) mm
Power supplies	1.8V (Digtal), 3.3V (Analog, Digital)
Number of pixels	100 (H) X 1028 (V) (Type 2 for HCG)
	1000 (H) X 1028 (V) (Type 3 for WDR)
Pixel type	4-TR (Pinned Photodiode)
Pixel size	7.1 μm X 7.1 μm
Fill factor	45 %
ADC resolution	17b (Max.)
Input referred noise (Type 2)	1.10 e^-_{rms} (# of samplings=32, ΔV_R=1V)
	1.17 e^-_{rms} (# of samplings=32, ΔV_R=2V)
Conversion gain	73.2 μV/e^- (Type 2)
	22.8 μV/e^- (Type 3)
DR (Type 3)	87.5 dB (# of samplings=32, ΔV_R=2V)
Frame rate	30 fps (# of samplings=32)
Power consumption	466.3 mW

Table I: Performance summary of the imagers.

22.8-μV/e-, respectively.

IV. Conclusion

An extremely low temporal noise and wide dynamic range CMOS image sensor is developed by using low-noise transistors and high gray-scale resolution (17b) folding-integration/cyclic ADC. Two types of pixel have been designed. One is a high conversion gain pixel with optimized FD node structure and the other is a pixel for achieving the wide dynamic range with an n-ch. native transistor. The CMOS image sensors which are in combination with the proposed pixels and the high performance column-parallel hybrid ADC have achieved a low pixel temporal noise of 1.1 e^-_{rms} (type 2) at ADC reference voltage ΔV_R=1.0 V and a wide dynamic range of 87.5 dB (type 3) at ADC reference voltage ΔV_R=2.0 V with the video rate operation.

Acknowledgment

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