Fabrication of large format, fully depleted CCDs for the Dark Energy Survey Camera

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***Abstract*—In this work we describe the fabrication of the fully depleted, back-illuminated charge-coupled devices for the Dark Energy Survey Camera, a 570 Mpixel camera installed on the 4-m Blanco telescope at the Cerro Tololo Inter-American Observatory. The methods to produce high quality wafers with extrinsic gettering layers are described as well as the hybrid CCD manufacturing model utilizing a commercial CCD foundry and a specialized facility to produce 250 µm-thick CCDs. The wafer-level screening methodology is described, and yield results for the large format CCDs are presented.**

I. Introduction

The 570 Mpixel Dark Energy Survey Camera (DECam) was installed and commissioned at the Cerro Tololo Inter-American Observatory (CTIO) in late 2012. The main elements of the camera are an optical corrector system with a three square degree field of view, a filter changer that can choose from a set of five filters covering the wavelength range from about 400 nm to 1.1 µm, a mechanical shutter, a precise six-axis positioning system to support and focus the camera, a steel support structure, and an array of 74 fully depleted, back-illuminated charge-coupled devices (CCDs) with associated control and readout electronics [1]. Figure 1a) shows a picture of the camera installed on the 4-m Blanco telescope. An image of the Small Magellanic Cloud taken during commissioning of the camera in September 2012 is shown in Fig. 2b).

The CCDs are operated with a substrate bias voltage of 40V that is sufficient to fully deplete the 250-µm thick substrates. The CCDs are back illuminated and have especially high quantum efficiency at red and near-infrared wavelengths when compared to standard, scientific CCDs [2]. There are 62, 2048 × 4096 and 12, 2048 × 2048 CCDs in DECam. The pixel size is 15 µm resulting in a die size for the 8 Mpixel CCDs of about 19 cm^2, and the CCDs are operated in full-frame mode and contain two source-follower readout amplifiers per device. The specifications include a read noise of less than 15 electrons rms at a readout speed of 250 kpixels/sec, a full-well capacity of more than 130,000 electrons, and a dark current of less than 35 electrons/pixel-hour at the operating temperature of -100C [3].

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a) b)

Figure 1. a) Photograph of the Dark Energy Survey Camera installed on the 4-m Blanco telescope at CTIO. The primary mirror of the telescope is at the lower left, and the telescope dome is visible in the background. b) Image of the Small Magellanic Cloud taken during early commissioning of the camera.

The CCDs were fabricated primarily at Teledyne DALSA Semiconductor. In order to produce back-illuminated CCDs, some fabrication was done at the Lawrence Berkeley National Laboratory (LBNL) MicroSystems Laboratory. In this work we describe in detail the fabrication methods used to produce the 74 scientific-quality CCDs required for DECam.

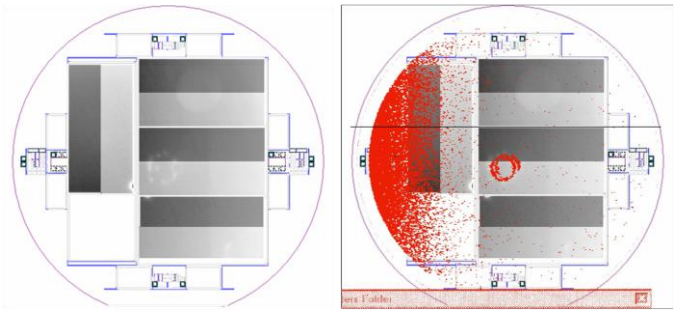
II. CCD FABRICATION

The CCD fabrication for DECam was divided into three steps – gettering of the starting material, partial CCD fabrication at Teledyne DALSA Semiconductor, and completion of the wafers at LBNL. These are described in the following.

A. Gettering process

The starting material for this work was 150 mm diameter, <100>, float-zone refined, n-type silicon with resistivity greater than 5000 Ω-cm. The wafer manufacturer was Siltronic.

In order to preserve the high resistivity and minority-carrier lifetime during the CCD processing, it is necessary to incorporate robust gettering from the beginning of the process. The method used previously at LBNL for charged particle detectors and CCDs was the deposition of a 1 µm-thick layer of in-situ doped (phosphorus) polysilicon (ISDP) [2] on the back side of the wafers. Attempts were made to procure gettered wafers directly from the wafer supplier, but only



a) b)

Figure 2. a) Dark current images taken at -45C superimposed on a drawing of the wafer layout. b) Map of particles added to the back side of the wafer by the plasma ashing equipment used in the Teledyne DALSA process superimposed on the items shown in a).

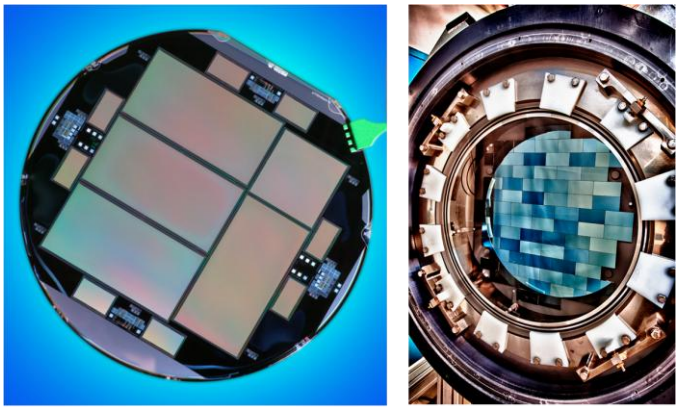
undoped polysilicon as a gettering layer was available. The ISDP process did exist at Teledyne DALSA, and it was decided that the gettering steps would be done on the starting material at Teledyne DALSA prior to the actual CCD fabrication.

The two main challenges associated with the implementation of the gettering process were particles produced during the ISDP deposition and contamination issues. The deposition of such a thick layer in a low-pressure chemical vapor deposition reactor resulted in high particle counts on the front sides of the wafers. An initial, pre-production lot showed low yields with large numbers of blocked columns and gate-insulator flaws that could be correlated with particle locations by methods described later.

The solution to this problem was to remove the particles by re-polishing the front surface of the wafers at a company specializing in wafer polishing services [4]. In order to ensure that no metallic contamination was added during this process, a sample wafer from each re-polished lot was sent to a testing laboratory where total reflection x-ray fluorescence was used to test for metallic contamination on the wafer surface [5]. This method is sensitive to concentrations as low as a few times 10^9 atoms/cm^2 of metals such as Fe, Ni, Cr, Cu, and Zn.

Contamination effects were observed when the back surface of the wafers came in contact with wafer handling equipment prior to the deposition of the ISDP layer. Figure 2 shows one example. Figure 2a) shows dark current images taken during completed wafer-level testing at -45C superimposed on a map of the wafer layout. High dark current was observed in localized regions near the center of the wafer. More detailed testing also revealed the presence of traps that were correlated to these regions.

It was suspected that the high dark current was due to contamination from wafer handling, and particle maps of the various types of equipment used in the gettering process were generated at Teledyne DALSA and compared to the dark current patterns. Figure 2b) shows a match of the dark current pattern to particles added to the back side of the wafer by the plasma equipment used to remove photoresist from the wafers. A second source of back-side contamination was observed [6], and both were eventually eliminated by process flow changes.



a) b)

Figure 3. a) Photograph of a 150 mm diameter DECam wafer that contains one 2048 × 2048 and four 2048 × 4096 CCDs. b) Photograph of the DECam focal plane.

B. Fabrication at Teledyne DALSA Semiconductor

Once the wafers were re-polished, the majority of the CCD fabrication was performed at Teledyne DALSA Semiconductor. A triple-polysilicon process using 1X, projection lithography was used. The CCD gate dielectric consisted of 50 nm each of SiO_2 and Si_3N_4. Wafers were processed in lots containing 24 wafers. Three wafers from each lot were completely finished at Teledyne DALSA to serve as quality control references. The remaining 21 partially processed wafers in a lot were sent to LBNL in order to produce 250 µm-thick, back-illuminated CCDs. Figure 3a) shows a photograph of a wafer fully processed at Teledyne DALSA. Figure 3b) shows the 74 back-illuminated CCDs installed in the DECam vacuum cryostat.

Given that the majority of yield loss for these large format devices was expected to occur in the gate insulator formation and polysilicon etching steps, the overall yield of the process was mainly dependent on the processing at Teledyne DALSA. As described in more detail later, the total yield for CCDs meeting the DECam specifications was about 25%. Yield improvement efforts led to a 35% yield for the final two production lots.

C. Fabrication at the LBNL MicroSystems Laboratory

A simplified cross-sectional diagram of the fully depleted CCD is shown in Fig. 4. The n+ contact on the back surface that consists of an ~25 nm-thick ISDP layer, and must simultaneously terminate the electric field in the fully depleted substrate while allowing for high light transmission [2]. Since the deposition temperature of 650C is too high for aluminum metallization, this step must be done prior to the aluminum deposition. In addition, the final thickness of the DECam CCDs, 250 µm, is much thinner than the standard wafer thickness of 675 µm for 150mm diameter wafers. As a result it was not practical to fabricate fully depleted, back-illuminated CCDs entirely at Teledyne DALSA due to equipment compatibility issues with the non-standard thickness wafers.

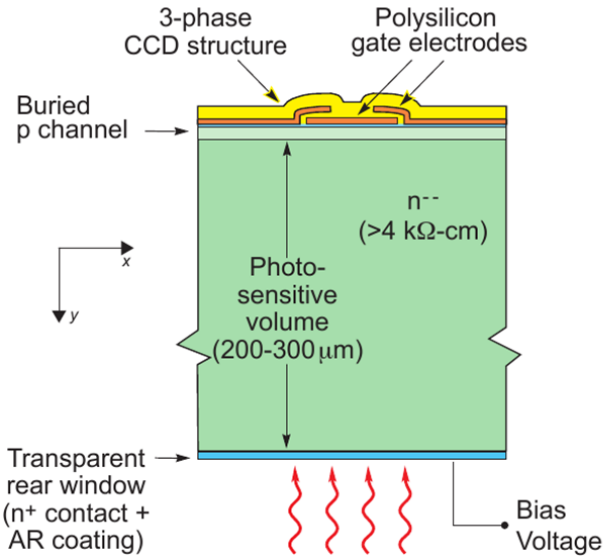


Figure 4. Simplified cross-sectional diagram of the fully depleted, back-illuminated CCD described in this work. The back side n+ contact is ≈ 25 nm thick and is formed by ISDP.

The approach taken was to remove wafers from the Teledyne DALSA foundry after processing through 8 photomasking steps, thin them to 250 µm, and complete the processing at the LBNL MicroSystems Laboratory where special care could be taken to process the 250 µm-thick wafers.

The wafer thinning consisted of a back-grinding step to remove most of the material followed by a chemical-mechanical polish step to remove the subsurface damage from the backgrinding. The polishing step removes about 10 µm of silicon. These steps were done at commercial companies.

At LBNL the first step was the deposition of the thin ISDP layer. This layer was then coated with SiO_2 to protect the back surface during the remainder of the processing. Modifications to the wafer-handling equipment were made to both protect the back surface from mechanical damage that can lead to localized regions of high dark current, and to avoid the use of materials in contact with the back surface of the wafer that could leave residues. Materials such as stainless steel and silicone were found to leave residues that could not be removed when the backside protective SiO_2 layer was etched off near the end of the process.

After the deposition of the protective layer of SiO2 on the back sides of the wafers, the remainder of the process was done including contact and metal photolithography and etching steps. After a conventional alloy step at 400C of the aluminum contacts, the back side protective oxide layer was removed in buffered hydrofluoric acid. Anti-reflecting coatings consisting of 55 nm of indium tin oxide (ITO) and 80 nm of SiO2 were deposited by sputtering.

A total of 7 lots were processed at Teledyne DALSA. Nominally 21 wafers per lot were thinned and subsequently processed at LBNL where the typical lot contained five wafers. A total of 125 wafers were processed at LBNL.

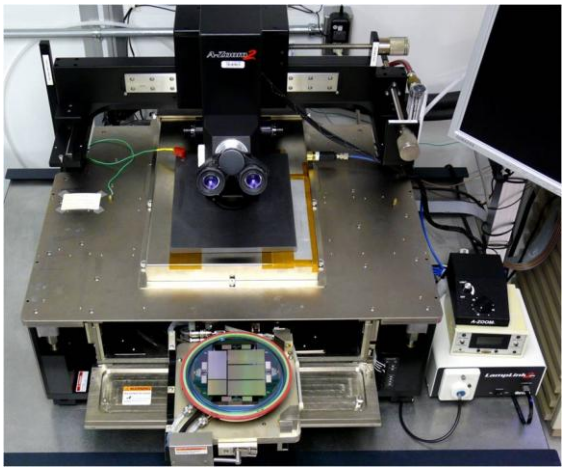


Figure 5. Photograph of the wafer-level probing equipment used to screen CCD devices for defects. A wafer mounted on a dicing-tape fixture is shown at the bottom of the photograph.

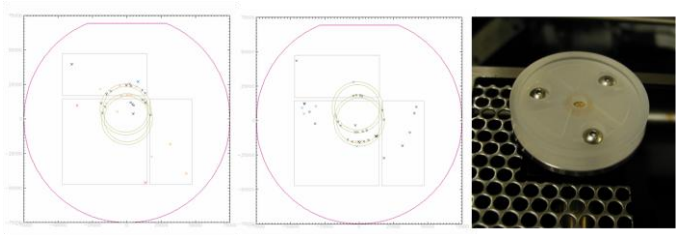
III. Wafer-level screening

In order to screen out defective devices prior to packaging the CCDs were tested at -45C at the wafer level. It was necessary to protect the back surfaces from mechanical damage and particle deposition during the testing, and this was accomplished by mounting the wafers on dicing-tape fixtures. Figure 5 shows a photograph of a wafer mounted on a tape frame about to be inserted in the wafer-level testing equipment. After the wafer-level screening the die were sent to Fermi National Accelerator Laboratory (FNAL) for packaging and detailed testing [7].

The testing methodology was designed to screen devices for short circuits, subtle gate-insulator flaws, and back-side defects [8]. The largest yield loss was due to clock shorts, which is to be expected for these large-area devices. A total of 460 2048 × 4096 die were screened for shorts, and 25.9% were found to have clock shorts. The shorts percentage improved over time to 19.7% for the final four Teledyne DALSA lots, and of these the best lot had only 9.5% shorts.

Gate-insulator and back side defects were detected by taking advantage of the exponential dependence of the corresponding current with electric field. In the case of the gate-insulator defects, the current-voltage relationship is a combination of Fowler-Nordheim tunneling in the SiO_2 portion and Poole-Frenkel and field emission of trapped electrons in the Si_3N_4 [9]. The testing method was to take a series of dark current images at the nominal clock voltages, followed by an identical set but with increased clock levels**;** **t**he nominal clock levels were +5V/-3V, and for the gate-insulator tests the levels were +6V/-4V. Median-filtered images for each clock level were compared, and columns with increased dark current in the higher-bias test were flagged automatically in the software analysis program. The yield loss due to this type of defect was 12.9%.

Back-side defects were detected during the wafer-level probing in a similar way to the gate-insulator defects described above but with substrate voltage varied in the two sets of images from the nominal value of 40V to 50V.



a) b) c)

Figure 6. a) – b) Wafer maps superimposed with the locations of back-side defects as determined by wafer-level testing done at -45C. Also superimposed is a ring-shaped region corresponding to the vacuum channel of the robotic wafer handling tool shown in c).

Columns with higher dark current at a substrate bias voltage of 50V were classified as back-side defects. Since the high dark current arises from the back surface of the device, typically 3 or more columns would show high dark current due to the diffusion of the charge carriers during the transit to the potential wells on the front side of the CCD. The gate insulator defects described earlier were typically limited to one column.

The back-side defects are strongly temperature dependent, with the dark current decreasing exponentially with temperature [10]. As a result of the strong temperature dependence, CCDs with only back-side defects were not considered defective and were packaged at FNAL for detailed testing.

The back-side defects also would often occur in repeatable positions on the wafer as determined by superimposing wafer-level dark current images on a map of the wafer layout as was shown in Fig. 2. This could occur from mechanical damage arising from the robotic wafer alignment tools and vacuum chucks that the wafers come in contact with during the processing at LBNL.

Figure 6 shows an example of back-side damage due to wafer handling equipment. Figures 6 a) and b) show the location of back-side defects superimposed on a wafer layout that was also used to fabricate CCDs during the DECam production. Also shown is a ring whose size corresponds to a vacuum groove in a wafer centering chuck that is part of a dielectric etch system used at LBNL. The back-side defects attributed to this equipment were eliminated after the vacuum groove was modified to reduce stress on the wafers.

The association of many back-side defects with mechanical damage was further suspected in that the density of back-side defects dropped dramatically when the back-side SiO_2 layer used to protect the back surface during processing at LBNL was upgraded from a 100 nm thick sputtered film to a 1 µm thick layer deposited by plasma-enhanced chemical vapor deposition [6]. The latter film was shown to have higher resistance to mechanical scratching.

Table 1 shows some of the major results from the CCD fabrication. The overall yield was about 25%, with this improving to about 35% for the final two Teledyne DALSA lots. The discrepancy between the number of CCDs passing the wafer-level screening tests and the final count is due to limitations in the former for detecting subtle effects such as charge transfer efficiency losses at -100C.

TABLE I
FABRICATION SUMMARY

Total number of wafers processed	125
% 2048 × 4096 die with clock shorts	25.9%
% 2048 × 4096 die with gate insulator defects	12.9%
# CCDs passing wafer-level screening tests	154 (30.8%)
# scientific grade CCDS after testing at FNAL	124 (24.8%)
# scientific grade CCDs produced from the final two lots	58

Summary of the fabrication results for DECam.

IV. Summary

We have described the methods used to produce 74 scientific-grade CCDs for the Dark Energy Survey camera including the gettering process and fabrication at Teledyne DALSA Semiconductor and Lawrence Berkeley National Laboratory. The techniques used for wafer-level screening have been described, and the correlation of back-side defects that are unique to fully depleted CCDs with mechanical damage from processing equipment has been discussed.

V. ACKNOWLEDGEMENTS

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