Digital Calibration Algorithm for 2-Stage Cyclic ADC used in 33-Mpixel 120-fps CMOS Image Sensor

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***Abstract* – This paper proposes a digital calibration algorithm for a 2-stage cyclic analog-to-digital converter (ADC) with 12-bit resolution used in a 33-Mpixel 120-fps CMOS image sensor. A simulation was performed to verify the algorithm with the large values of errors that we set. Results showed that the maximum differential nonlinearity (DNL) was improved to 0.49 LSB from 4.5 LSB, and that the integral nonlinearity (INL) improved to +0.23/−0.27 LSB from +6.27/−1.92 LSB.**

I. INTRODUCTION

We have been researching and developing a 33-Megapixel, 120-fps CMOS image sensor for full-spec SUPER Hi-VISION. 12-bit AD conversion within one horizontal scanning period of 1.92 μs is required for the ADC used in the full-spec SUPER Hi-VISION. To meet this specification, a column-parallel 2-stage cyclic ADC was developed, and a prototype sensor in which the ADC was implemented showed a sufficient image quality in conjunction with a low power consumption value of 2.45W at 120 fps [1][2].

If we can improve the output characteristics of the ADC without increasing the power consumption or chip size, it should be possible to increase the pixel count or bit-resolution much more, besides improving the signal-to-noise ratio of the sensor. However, the output characteristics of the ADC are very sensitive to the accuracy of the analog circuits, which results in large chip area and power consumption. Calibration techniques of ADC output characteristics and robust ADC architecture have been proposed to overcome these problems [3-5]. A digital calibration technique is one of the best ways to compensate for errors caused in the analog circuits in the digital domain with high accuracy. We therefore propose a digital calibration algorithm for the 2-stage cyclic ADC and verify the calibration effect by simulation.

II. 2-STAGE CYCLIC ADC

A schematic diagram of the 2-stage cyclic ADC with 12-bit precision is shown in Fig. 1. The single-ended cyclic ADC with internal reference and return-to-zero (RTZ) digital-signal feedback technique [6] is used in each stage of the ADC. Each stage uses 1.5-bit architecture, which generates 3-state redundant binary (RB) codes expressed with two decision levels (2 bits) for each cycle to relax the comparator's precision demand [7]. The ADC consists of a single-ended amplifier, two

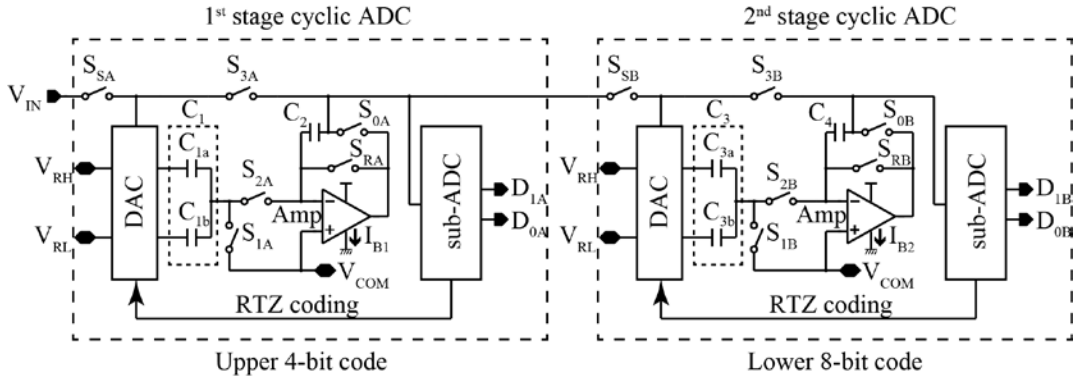


Fig. 1 Schematic diagram of the 2-stage cyclic ADC with 12-bit precision.

capacitors (C_1 and C_2 for the 1st-stage ADC; C_3 and C_4 for the 2nd-stage ADC), a sub-ADC with two comparators, switch transistors, and a digital-to-analog converter (DAC) with a decoder. The sampling capacitor C_1 is divided into C_{1a} and C_{1b}, and C_3 is divided into C_{3a} and C_{3b} for the internal reference generation with high accuracy.

The operation of the 2-stage cyclic ADC is as follows. 1) After resetting all the capacitors in the 1st-stage ADC, the analog input signal is sampled by turning on the S_{SA} and S_{3A} to introduce the signal into the sub-ADC that outputs the most significant digit. 2) Then, the code determines the switches in the DAC that must be turned on, and the input is multiplied with a gain of two and subtracted from a reference level. 3) After the amplification phase, the residual signal is returned to the input node of the 1st-stage ADC and the second significant digit is determined by the sub-ADC.

The amplification and the feedback phases are repeated three times to obtain the first 4 bits of resolution. During the amplification phase of the last cycle, the 1st-stage ADC is connected to the 2nd-stage ADC by turning on the switch S_{SB} to transfer the analog residue of the 1st-stage ADC to the 2nd-stage ADC. After this sampling phase of the 2nd-stage ADC, S_{SB} is turned off and the amplification and feedback phases are repeated eight times in the 2nd-stage ADC to obtain the last 8 bits of conversion, for a total of 12 bits. While the 2nd-stage ADC processes the AD conversion, the 1st-stage ADC can sample and convert the next pixel signal, which means these two ADC stages can process in parallel with this architecture.

III. DIGITAL CALIBRATION

A. *Algorithm*

In the amplification phase described above, the ideal output of the amplifier can be represented as

$$X_{out} = 2X_{in} - D \qquad (1)$$

where D denotes the output RB code of the sub-ADC and X_{out} and X_{in} are respectively the output and input signal of the amplifier, both of which are quantized by a radix-2 algorithm.

However, the analog components in the ADC have a variety of errors, so the actual output is not expressed as (1). Figure 2 shows the cause of these errors in a single stage cyclic ADC, which contains sampling capacitor C_c (divided into C_{c1} and C_{c2}) and C_f, amplifier with open loop gain G_0.

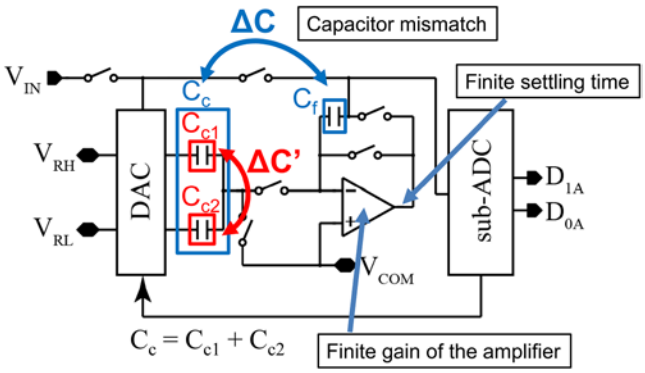


Fig. 2 The cause of errors in a cyclic ADC.

The ideal capacitance of C_c is identical with that of C_f, and the ideal capacitance of C_{c1} is also identical with that of C_{c2}. However, there is a capacitor mismatch ΔC between C_c and C_f and $\Delta C'$ between C_{c1} and C_{c2} due to a process variation. The capacitor mismatch errors e_{cm} and e_{cm}' are defined by

$$e_{cm} = \frac{\Delta C}{C_f} \quad , \quad e'_{cm} = \frac{\Delta C'}{C_c}$$

The error due to the finite gain of the amplifier G_0 causes the difference from the gain of two in the amplification phase. The error e_{fg} is defined by

$$e_{cm} = \frac{C_c + C_f + C_i}{C_f G_0}$$

where C_i is an input capacitance of the amplifier.

The finite settling time causes the settling error e_{st} of the amplifier, which also results in the difference from the gain of two in the amplification phase.

These errors increase the DNL and INL of the ADC, which degrades the bit resolution. To compensate for the errors and improve the output characteristics of the ADC, we applied the digital calibration algorithm to the 2-stage cyclic ADC. Input referred total error is calculated from digitized output of the ADC. Although digitized output without errors is desirable for

accurate calibration, errors would be negligible if they are small enough. The calibrated final output is obtained by subtracting the total error from the digitized output.

An actual output of the amplifier in the amplification phase, which includes the errors caused in the analog circuits, is expressed as

$$X_{out} = (2+e_{cm})(1-e_{fg})(1-e_{st})X_{in} - (1+e_{cm})(1-e_{fg})(1-e_{st})\left(D + Ds \cdot \frac{e'_{cm}}{2}\right) \qquad (2)$$

where Ds is a constant that is equal to 0 as D = (0, 1) and equal to 1 as D = 1/2. X_{out} is the input for the (i + 1)-th conversion step and X_{in} is the input for the i-th conversion step, so equation (2) is given by

$$\begin{aligned} X(i+1) &= (2+e_{cm})(1-e_{fg})(1-e_{st})X(i) - (1+e_{cm})(1-e_{fg})(1-e_{st})\left(D(i) + Ds(i) \cdot \frac{e'_{cm}}{2}\right) \\ &\approx 2X(i) - D(i) + (e_{cm} - 2e_{fg} - 2e_{st})X(i) - (e_{cm} - e_{fg} - e_{st})\left(D(i) + Ds(i) \cdot \frac{e'_{cm}}{2}\right) \\ &= X(i+1)_{ideal} + E(i+1) \end{aligned} \qquad (3)$$

where $D(i)$ denotes the output RB code of the sub-ADC for the i-th conversion step, $Ds(i)$ has the same definition as Ds mentioned above, and $X(i+1)_{ideal}$ and $E(i+1)$ are defined by

$$X(i+1)_{ideal} = 2X(i) - D(i)$$

$$E(i+1) = (e_{cm} - 2e_{fg} - 2e_{st})X(i) - (e_{cm} - e_{fg} - e_{st})\left(D(i) + Ds(i) \cdot \frac{e'_{cm}}{2}\right)$$

An actual input for the (i + 1)-th conversion step $X(i+1)$ represents the summation of the ideal input $X(i+1)_{ideal}$ and the error $E(i+1)$ due to the three kinds of errors mentioned above. Total error after repeating 12 conversion steps is given by summing up $E(i+1)$ for i = 1 to 11. To calculate the summation, it is important that the three kinds of errors caused in the 1st-stage ADC are used as summing it up from i = 1 to 3 and the errors caused in the 2nd-stage ADC are used as summing it up from i = 4 to 11. The resulting input-referred total error due to the capacitor mismatch, the finite gain of the amplifier, and the finite settling time are expressed as equation (4):

$$\begin{aligned} E_{total} = {} & e_{cm1}2^{-2}\left(-D(0) + D(2)2^{-2} + 3\sum_{i=3}^{11} D(i)2^{-i}\right) + e_{cm2}2^{-5}\left(-D(3) + \sum_{i=2}^{8}(i-1)D(i+3)2^{-i}\right) - e'_{cm1}2^{-2}\sum_{i=1}^{3} Ds(i)2^{-i} - e'_{cm2}2^{-4}\sum_{i=1}^{9} Ds(i+3)2^{-i} \\ & - e_{fg1}2^{-1}\left(\sum_{i=1}^{2} iD(i)2^{-i} + 3\sum_{i=3}^{11} D(i)2^{-i}\right) - e_{fg2}2^{-4}\sum_{i=1}^{8} iD(i+3)2^{-i} - e_{st1}2^{-1}\left(\sum_{i=1}^{2} iD(i)2^{-i} + 3\sum_{i=3}^{11} D(i)2^{-i}\right) - e_{st2}2^{-4}\sum_{i=1}^{8} iD(i+3)2^{-i} \end{aligned} \qquad (4)$$

where e_{cm1} and e_{cm2} denote the capacitor mismatch error between C_1 and C_2 for the 1st-stage ADC and C_3 and C_4 for the 2nd-stage ADC, e_{cm1}' and e_{cm2}' denote the capacitor mismatch error between C_{1a} and C_{1b} for the 1st-stage ADC and C_{3a} and C_{3b} for the 2nd-stage ADC, e_{fg1} and e_{fg2} denote the finite amplifier's gain error of the 1st-stage ADC and the 2nd-stage ADC, and e_{st1} and e_{st2} denote the settling error of the 1st-stage ADC and the 2nd-stage ADC. The digital calibration is performed by subtracting E_{total} from the digitized output.

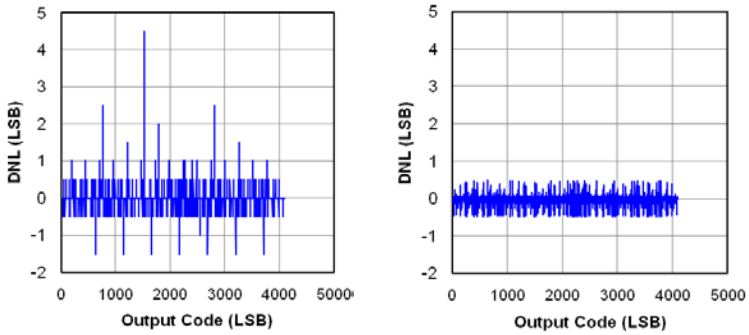
B. Calibration performance

A simulation was performed to verify the effectiveness of the proposed calibration method. Figure 3(a) shows the simulation results of the DNL with errors whose values are superimposed in Fig. 3. With the large values of errors that we set for simulation, the maximum DNL is 4.5 LSB, and several codes are missing due to the errors. Figure 3(b) shows the simulation results after the digital calibration. The missing codes are repaired, and the maximum DNL is reduced to 0.49 LSB. The INL is also improved to +0.23/−0.27 LSB from +6.27/−1.92 LSB, as shown in Fig. 4(a) and (b).

The values of the errors used in the simulation were calculated by the design parameters of the ADC circuit. The parameters were set to make the errors large compared to those of the actual ADC in the image sensor for verifying the digital calibration algorithm performance. This means the capacitance C_1 − C_4 and the bias current of the amplifier I_{B1} (1st-stage ADC), I_{B2} (2nd-stage ADC) are designed smaller than those in Ref [1][2]. Therefore, the simulation results show that the proposed calibration method not only improves the output characteristics but also reduces the power consumption and layout area of the ADC in the image sensor.

IV. CONCLUSION

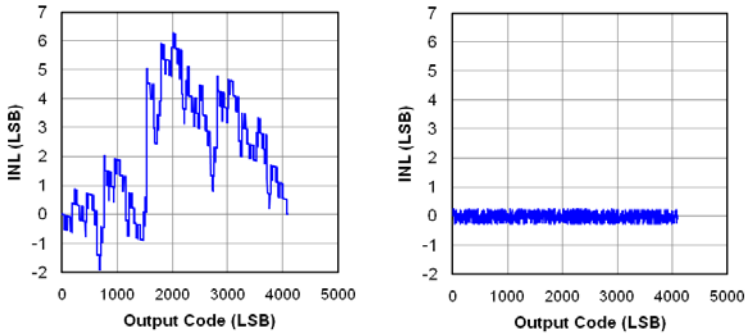
We proposed a digital calibration algorithm for a 2-stage cyclic ADC with 12-bit resolution used in a 33-Megapixel, 120-fps CMOS image sensor for full-spec SUPER Hi-VISION. The algorithm can compensate for errors due to the capacitor mismatch, the finite gain of the amplifier, and the finite settling time, and it improves the output characteristics of



(a) Before calibration (b) After calibration

Values of errors for the simulation are as follows:
$e_{cm1} = 3.8 \times 10^{-3}$, $e_{cm2} = 7.5 \times 10^{-3}$,
$e_{cm1}' = 2.7 \times 10^{-3}$, $e_{cm2}' = 5.4 \times 10^{-3}$,
$e_{fg1} = 3.0 \times 10^{-5}$, $e_{fg2} = 8.7 \times 10^{-5}$,
$e_{st1} = 8.3 \times 10^{-5}$, $e_{st2} = 9.1 \times 10^{-4}$

Fig. 3 Simulated DNL plot with and without digital calibration when values of errors are set as stated in text.



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$e_{st1} = 8.3 \times 10^{-5}$, $e_{st2} = 9.1 \times 10^{-4}$

Fig. 4 Simulated INL plot with and without digital calibration when values of errors are set as stated in text.

the ADC dramatically. This technique enables the sensitivity against non-idealities of the analog circuits in the ADC to be reduced, which results in the reduction of power consumption and layout area of the ADC in the image sensor.

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