Radiation-hard Active Pixel Detectors for Tracking of Charged Particles based on HV-CMOS Technology

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This paper presents first results with radiation-hard, 100% fill-factor sensors for charged particle tracking exploiting deep-n-well structures of HV-CMOS processes. While monolithic active pixel sensors (MAPS) with this technology are conceivable, the complex functionality (sparse readout, trigger handling) and rad-hardness requirements are challenging. This is overcome by producing active sensors where the complex functions are outsourced to already existing tracker readout ASICs, focusing on the technological advantages of HV-CMOS processes for active tracking sensors: rad-hardness, resolution/pitch, material budget and cost.

I. INTRODUCTION

A. LHC and ATLAS upgrades

The Large Hadron Collider (LHC) at CERN near Geneva is currently the world's largest particle accelerator. After running some years at and even above its design luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and after having collected some hundred fb^{-1} of integrated luminosity, the increase in statistics will be slow. Improvements in the generation and collimation of high-intensity beams, however, indicate that a luminosity of up to $10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ might be achievable with some upgrades to the accelerator resulting in a high-luminosity LHC (HL-LHC). A large upgrade is foreseen for 2022 to reach this goal.

One of the four large experiments at LHC is ATLAS [1], a multi purpose detector which aims for new physics such as the recently discovered Higgs boson. Its innermost part is the inner tracker which is consisting of the transition radiation tracker (TRT), the silicon strip detector (SCT) and the Pixel Detector [2, 3], which is closest to the beam and is needed to cope with the large density of particle tracks near the interaction point.

For luminosities above roughly $3{\cdot}10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, the TRT will suffer from occupancy issues while the two silicon detector parts will have taken considerable radiation damage at this stage. Therefore, a complete replacement of the inner tracker is necessary. Currently, two detector technologies are foreseen: silicon strip detectors will be used outside of a radius of about 30 cm from the beam. For occupancy reasons, a subdivision in standard or 'long' strips ($\sim$ 10 cm) for the outer layers and 'short' strips ($\sim$ 2 cm) for the inner layers must be made. Inside of the 30 cm radius, where both occupancy and radiation damage become too large for strip detectors, pixel detectors will be used.

For radiation damage reasons, only hybrid pixel detectors were used up to now by ATLAS. These comprise a silicon pixel sensor fabricated on high-resistivity FZ silicon and a bump-bonded readout chip in deep submicron technology. The requirement for bump-bonding and mechanical demands constrained the pixel pitch/size to larger than 50 μm and also led to increased material budget (thermal mismatch during reflow requires stability) as well as to elevated costs which prevented the instrumentation of larger areas with pixel sensors.

The main challenges for future sensors are the required increased radiation hardness and granularity while at the same time a reduced material budget and minimized cost are mandatory. There are ATLAS Upgrade R&D projects exploring whether the radiation hardness of the established planar pixel sensors is sufficient for HL-LHC usage[4, 5] and on new detector technologies such as 3D silicon, diamond and gaseous detectors (GOSSIP, GridPix). Since 2011, active sensors in HV-CMOS technology are pursued as an additional alternative. They promise to be sufficiently radiation-hard while being an industrially available standard component and hence cheap. In addition, they offer some additional features standard (pixel) sensors cannot offer such as bump-less capacitive coupling, small cluster sizes also at large incidence angles and improved resolution.

B. HV-CMOS Active Sensors

Deep-submicron HV-CMOS processes feature moderate bulk resistivity and high-voltage capability and are therefore good candidates for drift-based radiation-hard monolithic active pixel sensors (MAPS)[6]. It is possible to apply 60-100V of bias voltage leading to a depletion depth of 10-20 μm. Thanks to the high electric field, charge collection is fast and nearly insensi-

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tive to radiation-induced trapping. Due to the dopant concentration, the depletion voltage is stable up to $\sim 10^{16}\,n_{eq}/cm^2$. In principle, the process could be used to produce cheap standard n^+-in-p type strip and pixel sensors (see Fig. 1), but due to the shallow depletion zone with only very little signal charge.

We explore instead the concept of using such a HV CMOS process to produce active sensors that contain simple circuits to amplify and discriminate the signal inside deep n-wells (see Fig. 2). A traditional readout chip (pixel or strip) is still needed to receive and organize the data from the active sensor and handle high-level functionality such as trigger management. Prototype chips can be made such that strip-like or pixel-like readout can be selected on the same device.

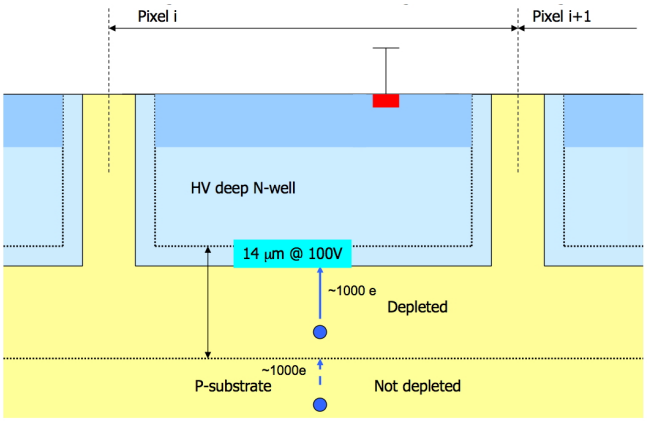

FIG. 1. Schematic cross-section of a standard planar n^+-in-p sensor fabricated with an HV-CMOS process. The HV deep n-well acts as pixel implant and up to $\sim$ 100 V can be applied to the substrate creating a depletion zone of about $10-20\,\mu$m which results in a collected charge of only about 1000 electrons – very challenging for a hybrid readout chip.

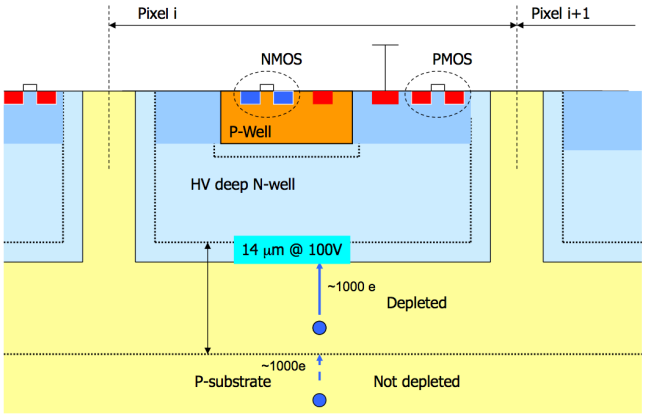

FIG. 2. Schematic cross-section of an HV-CMOS active sensor. Compared to Fig. 1, active circuit components are placed either within (shallow) p-wells (NMOS) or directly within the deep n-well (PMOS). A triple-well structure to better isolate the PMOS would be possible, but did not prove necessary up to now.

While a readout chip is still needed (unlike the case of an ideal MAPS device that contains all sensing and processing functionality in one), the active sensor approach offers many advantages: such sensors can be fabricated in a fully commercial CMOS process without need for special substrates or processing and will therefore cost less than traditional diode sensors, they can be thinned to the limit of the collection layer resulting in much lower mass, they require relatively low bias voltage, and they can operate at room temperature or with only moderate cooling after irradiation. In addition, they can contain sub-pixels[1] with smaller pitch than the readout chip and improve the spatial resolution compared to standard sensors by encoding the hit sub-pixels in the signal sent to the readout chip. From a practical perspective, maintaining the traditional separation between sensing and processing functions lowers development cost and makes use of existing infrastructure. Active sensors can also be seen as a first step towards 3D-integrated electronics in which the analogue tier contains the sensor.

II. EXPERIMENTAL SETUP

A. Prototype Sensors

To explore the performance and radiation hardness of active sensors, the HV2FEI4 ASIC (see Fig. 3) was produced in the AMS H18 process. It is compatible with ATLAS FE-I4 pixel readout chip, the ATLAS ABCN and the LHCb Beetle strip readout chips and provides some functionality also with the Medipix/Timepix family of readout chips. It features a matrix of 60 by 24 (sub-) pixels with a sub-pixel cell size of 33 by 125 μm. Thanks to relying on active circuits, capacitive coupling to the pixel readout chip appeared feasible and is explored with HV2FEI4 chips glued to FE-I4 and Timepix chips. The option to replace the expensive and time-consuming bump-bonding by gluing would significantly lower the cost of future large-scale Pixel Detector upgrades and enable the instrumentation of larger areas with pixel detectors. For comparison, bump-bonding the HV2FEI4 with gold stud-bumps is still possible.

The HV2FEI4 pixels are combined to match the readout multiplicity of the respective chips: for the pixel readout, three HV-CMOS pixels are multiplexed onto one FE-I4 pixel such that the position of the hit pixels are encoded by the pulse height. In this way, the position resolution of the HV-CMOS sensor can in principle be significantly better than the granularity of the readout chip suggests. For the strip readout, the pixel cells are combined to form virtual strips. Here, the z-position of

[1] The term 'sub-pixel' is used to differentiate the (small) pixels on the (active) sensor level from the (bigger) pixels in the readout chip.

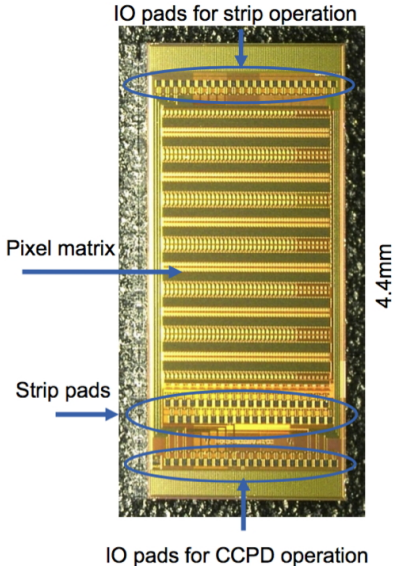

FIG. 3. Photograph of the first prototype chip HV2FEI4.

the hit is encoded via the discriminator's pulse height and can be evaluated by analogue strip readout electronics like the Beetle chip. For more details see [7].

B. Test setup

To examine the possibility of a capacitively coupled, ultra-fine pitch active sensor, several HV2FEI4 were glued to FE-I4 readout chips both with and without bumps. The gluing was done using Fineplacer Lambda die bonders with an estimated alignment accuracy of better than 5 μm and with radiation-hard liquid epoxy resin adhesives. The contact pressure was chosen in the range of a few Newton resulting in glue layer thicknesses of only few μm. The glued assemblies were mounted on PCBs which were derived from so-called FE-I4 single chip cards used within the ATLAS collaboration for sensor R&D purposes. While the FE-I4 wire bond pads were connected in the standard way, the HV2FEI4 pads were wire bonded from the backside of the PCB through a hole. In spite of being an uncommon procedure, no problems were encountered. For future applications, several alternatives are being explored to connect the supply voltages, among them through-silicon vias (TSVs), C4NP-based bump bonds, and conductive adhesives. The readout was done using USBPix test systems with ATLAS STControl software; the HV-CMOS was configured using a UXIBO FPGA interface board.

III. FIRST RESULTS

Already the first measurements showed that the capacitive coupling is working very well – actually better than expected. This is due to the very thin glue layer which up to now could only be measured to be below $\sim 5\,\mu$m while originally, a layer thickness between 10 and 25 μm was expected. In fact, the dynamic range of the discriminators' output stages was such that the step size at low ToT values is very coarse. Nevertheless, this result is very encouraging as the area of the receiving FE-I4 electrode/bump pad is fixed and the voltage amplitude on the HV2FEI4 is limited to 1.8 V with standard supply voltages.

To examine sub-pixel encoding, the on-chip 5-bit DAC values for the bias voltages of the output stages for the 3 sub-pixels were chosen to be 2, 4 and 20 to obtain a clear separation in ToT values – a consequence of the coarse and non-linear output stage behavior at low DAC values combined with the non-linear behavior of the FE-I4 at high ToT values. To avoid complications from non-perfect tuning and matching of the FE-I4 to the HV2FEI4, the measurement was performed using one (FE-I4) pixel only and will be extended to the full matrix later - but offline corrections for each pixel should be straightforward. As displayed in Fig. 4, a clear separation is reached between hits for the different sub-pixels proving that capacitively coupled devices with a granularity higher than the readout chip are possible. A similar measurement was performed using the strip readout configuration where not the individual sub-pixel is encoded, but rather the position along the virtual strip. Here, too, different pulse heights depending on the activated row were visible on the monitor output. Work is ongoing to use the Beetle-chip's abilities to decode the z-position of the strip.

While test pulser studies are valuable to understand the circuit behavior, source scans are important to ensure that the charge deposited in the shallow depletion zone is enough to safely trigger the discriminator already at threshold values compatible with a good noise occupancy. To mimic minimum ionizing particles (MIPs), a

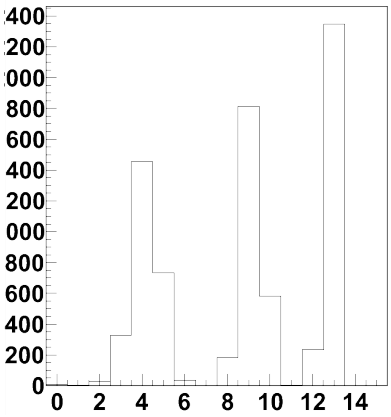

FIG. 4. Time-over-Threshold (ToT) spectrum obtained from a single FE-I4 pixel using the HV2FEI4 test pulser input. The 3 HV-CMOS sub-pixels can clearly be distinguished as peaks thus enabling the a position resolution beyond the granularity of the readout chip.

^{90}Sr beta-source was used which provides electrons up to an energy of 2.2 MeV. First measurements with a scintillator trigger below the assembly to exclude noise hits were successful, but at the expense of low rates. Subsequently, the FE-I4's self-trigger was used and rather homogeneous hit maps could be recorded (see Fig. 5) – in fact no bias voltage was necessary to achieve hits which is currently being further investigated. While the efficiency cannot be estimated up to now, this result clearly shows that the basic principle works well and particles can be detected in spite of the shallow depletion zone.

The first HV2FEI4 prototype chip (v1) has been irradiated with reactor neutrons, high-energy protons and x-rays. Results from the latter irradiations have shown that the deliberately standard (i.e. rad-soft) design suffers from ionizing dose. While the amplifier output is working (with more and more reduced pulse heights) up to 50 MRad, no discriminator signal is seen beyond 10 MRad. First radiation effects appear beyond 100 kRad; more details will be reported elsewhere.

IV. CONCLUSIONS AND OUTLOOK

A first prototype for radiation-hard active pixel detectors based on HV-CMOS technology has been produced and initial tests have been performed. These have shown that capacitive coupling between active sensor and pixel readout chip is working which allows to use gluing as a very cost-efficient hybridization method. The active sensor (sub-)pixels can be significantly smaller than the readout chip pixel size; it was shown that the position of the hit sub-pixel can be encoded and obtained from readout chips with pulse-height readout. This allows for new tracker concepts, e.g. single-sided strip sensor layers without stereo-angle, or for dedicated end cap sensors with square $50 \times 50\,\mu$m pixel footprint while still using the current ATLAS readout chip FE-I4 which has a pixel size of $50 \times 250\,\mu$m. The prototypes have been produced with a thickness of 260 μm but could easily be thinned down to reduce the material budget. The production is done on 8" wafers with a reticule size of about 2×2 cm enabling very cost-efficient production compared to standard silicon sensors.

A second version of the HV2FEI4 has been produced with a modified, rad-hard design. First tests are ongoing and an irradiation and testbeam campaign will follow. Future planned submissions include dedicated square forward pixels and an optimized virtual strip design.

HV-CMOS is also a promising candidate for applications where the pitch does not allow standard bump-bonding, e.g. with the CLICPix chip which has a pitch of only 25 μm. Future options include the use of HV-CMOS as analogue tier in a 3D-integrated readout-chip which includes already the sensor. Also a full-scale MAPS chip is conceivable in HV-CMOS technology and the baseline for the Mu3e experiment at PSI.

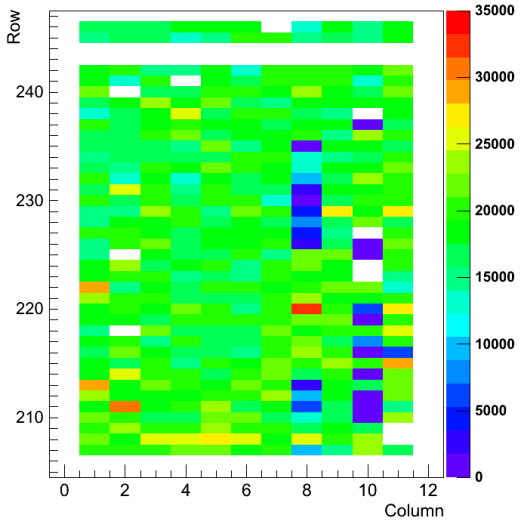

FIG. 5. Hit map of a source scan with ^{90}Sr. Only the region of the FE-I4 where the HV-CMOS chip was mounted (see row numbers) is displayed. A fairly homogeneous pattern of hits can be seen; some hot pixels were masked in the FE-I4 (white). The two columns with reduced hits are attributed to the specific FE-I4 as they were not seen with other samples. The two masked rows are containing a simplified pixel type which requires different threshold settings and was therefore excluded from this measurement.

V. ACKNOWLEDGEMENTS

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[1] [ATLAS collaboration], *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003
[2] [ATLAS Collaboration], *ATLAS Pixel Detector Technical Design Report*, CERN/LHCC 98-13, May 1998
[3] G. Aad et al. [ATLAS Pixel collaboration], *ATLAS pixel detector electronics and sensors*, JINST **3** (2008) P07007
[4] D. Muenstermann, *R&D on Planar Pixel Sensor Technology for the ATLAS Inner Detector Upgrade (PPS Proposal)*, CERN EDMS ATU-RD-MN-0019.
[5] M. Beimforde, *The ATLAS Planar Pixel Sensor R&D project*, Nucl. Instr. and Meth. **A636** (2011) S8-S14
[6] I. Peric, *A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology*, Nucl. Instr. and Meth. **A582** (2007) 876-885
[7] I. Peric, *Active pixel sensors in high-voltage CMOS technologies for ATLAS*, JINST **7** (2002) C08002