# Linear High-Dynamic-Range Bouncing Pixel with Single Sample

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***Abstract*—An alternative pixel topology for CMOS image sensors with High Dynamic Range (HDR) is presented. The pixel is based on an approach that allows the HDR sensor to operate with linear response and yet, with just a single sample, and achieve constant sensitivity, apart from noise effects, throughout the whole DR. The control is simple, automatic and on pixel, always yielding HDR images with no complex embedded algorithms or image post processing. The pixel was simulated in a 0.35µm standard CMOS technology, achieving a DR of up to 118dB. Pixel architecture and detailed operation are discussed, and simulation results are presented.**

***Index Terms*—Dynamic range (DR), CMOS image sensors, linear response, sensitivity**

## I. Introduction

One of the key requirements for many imaging applications is high sensitivity as well as High Dynamic Range (HDR). The latter is defined as the ratio between the brightest and the darkest resolvable points or regions on an image. While the feature size in CMOS technology continuously downscales, enabling high resolution imaging, usually limited by the camera lens, they also affect negatively the DR and sensitivity, by means of the increased leakage current, noise components, limited quantum efficiency and reduced signal swing [1]. Dealing with these issues and designing HDR sensors while keeping good sensitivity is not a straightforward task.

Regarding this matter, many solutions for HDR image sensors have been proposed. Generally, they are classified into seven different categories [2]: 1) The Companding sensors, or logarithm sensors, have a very simple control and high DR, but with signal non-linearity and poor sensitivity at high illumination levels, resulting in lower modulation transfer function over a scene [3]; 2) Multimode sensors operate in both logarithm and linear modes [4,5], achieving very high DR, while increasing sensitivity for lower illumination levels. However, they still have poor sensitivity at high light intensities, while demanding a more sophisticated control, and non-trivial signal processing; 3) Clipping sensors [6,7] use Capacitance Adjustment, which combines the response of different capacitances, i.e. different sensitivities, in order to achieve a HDR, which renders the control and signal processing more complex; 4) Frequency-based sensors [8,9] have linear response, while achieving HDR with a high frame rate. However, they have lower sensitivity to low illumination levels, since they just detect saturation events; 5) Time to first-spike (TTS) sensors [10,11] have very high DR, and high frame rate as well, but still suffer under low sensitivity at high illumination levels. Further, they need very precise time controlling and high resolution of the saturation time representation; 6) Global-control-over-the-integration-time sensors [12,13] and 7) Autonomous-control-over-the-integration-time sensors [14,15] implement multiple capture algorithms, which require complex signal processing and control, without solving the problem of the sensitivity at highlights. Besides that, they have lower frame rate due to the need of multiple exposures.

For the usual HDR approaches, the main drawbacks are poor sensitivity at higher or lower illumination levels, non-linear response, reduced frame rate (multiple captures required), sophisticated control and non-trivial image processing. The pixel that seems to fulfill all these requirements is the conventional linear APS (Active Pixel Sensor) topology which however features very low DR. If it was possible to increase the voltage swing to a very large extent, for a fixed integration time ($\Delta T$), the aforementioned issues would be solved, since the response would be linear, a single capture would be needed, and $\Delta T$ would not need to be shortened for high illumination levels, which seriously affects the sensitivity. But, the usually low chip supply voltage in standard CMOS processes precludes any considerable increase in the voltage swing.

However, the increase of the voltage swing can be emulated. For this purpose we have envisioned a pixel-circuit topology, based on the Current-Mirroring-Integration (CMI) architecture [16,17,18], which yields a very high DR within a pre-set integration time in the reset-integration cycle, with linear response, single sample, and constant sensitivity.

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## II. Pixel Design

### A. Principle of Operation

In order to reconstruct an image, voltage-mode CMOS image sensors must provide information about both time and voltage for each pixel. Usual solutions for HDR are to alter the integration time for different pixels in the same frame, keeping the voltage swing constant, or accommodate the signal in a constant voltage and time interval. What is not normally done is try to enhance the voltage swing [16,19] conserving a constant integration time.

The CMI topology uses a feedback structure based on current mirrors, featuring stable bias voltage across the photodetector and low input impedance, while mirroring the photogenerated current to an integration capacitor. As the current is integrated, the voltage increases over the integration time with a slope proportional to the pixel photocurrent.

The main idea of the circuit is to prevent that the integrated voltage reaches saturation; instead, the signal bounces at a reference upper signal and continues to integrate downwards, maintaining the slope, until it eventually reaches the lower reference limit and re-bounces upwards. This process repeats itself every time the signal would saturate within the boundaries of a stipulated voltage difference. Figure 1 illustrates the concept for different photocurrent values. The number of bounces is then counted and the output comprises two signals: a digital one, indicating the number of bounces; and an analog one, i.e. the voltage of an off-pixel capacitor ($V_{CAP}$). With these two signals a high DR can be achieved.

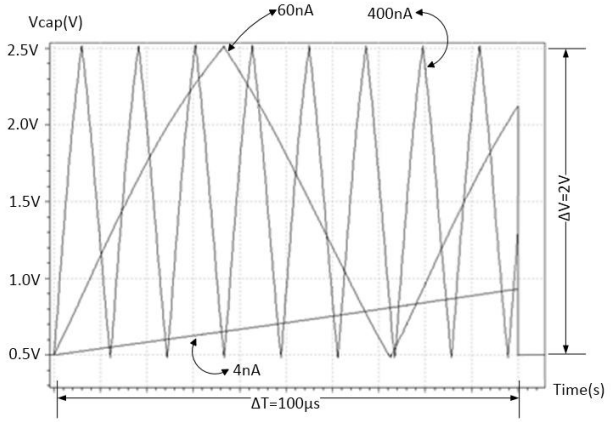


Fig. 1. Integrated Output Voltage across the capacitor for three different photocurrents.

The dynamic range extension factor (DRF) [2] is calculated as follows:

$$DRF = 20\log\left(\frac{I_N}{I_1}\right) = 20\log(N) \quad (1)$$

$$I_k = \frac{C\cdot(\Delta V\cdot k)}{\Delta T} \quad , \qquad k = 1,2 \ldots N \quad (2)$$

where $C$ is the value of the off-pixel integration capacitor, $\Delta V$ the stipulated voltage difference, $\Delta T$ the pre-set integration time, and $k$ is the emulated voltage-increase factor (i.e. the number of counted bounces); $I_k$ is the photocurrent when the $k^{\text{th}}$ bounce occurs, and $N = 2^b$ is the maximum number of rebounces, for a b-bits counter; $I_N$ represents the largest photocurrent measurable before the counter reaches saturation, and $I_1$ the photocurrent when the first bounce occurs. Hence, the DRF depends on the counter size $b$. For an 8-bit counter the DRF exceeds 48dB. The DRF measures how much the DR can be extended. For instance, for the normal pixel, without re-bouncing, with a $DR_0$ equal to 60dB, the maximum photocurrent before saturation will be $I_1$. So, for the bouncing pixel, the new $DR_N$ will be:

$$DR_N = 20\log\left(\frac{I_N}{I_{min}}\right) = 20\log\left(\frac{I_1}{I_{min}}\cdot\frac{I_N}{I_1}\right) = DR_0 + DRF \quad (3)$$

where $I_{min}$ is the minimum photocurrent. The above equation yields a $DR_N$=108dB.

To reconstruct the image, one must combine the analog and the digital values for each pixel. The analog one is the off-pixel capacitor voltage ($V_{CAP}$) and is read as usual at the end of $\Delta T$. The digital one is the number of bounces ($k$) that were counted. Then, the final reconstructed value ($V_R$) is:

$$V_R = \Delta V\cdot k + V_{CAP} \quad (4)$$

for $k$ even, or:

$$V_R = \Delta V\cdot(k+1) - V_{CAP} \quad (5)$$

for $k$ odd.

For a given photocurrent $i_{ph}$, let $t_{up}$ be the time spent by the signal to go from the bottom to the top of the voltage difference ΔV, and $t_{down}$ the time spent to go downwards. If the slope does not vary, meaning the photocurrent is constant, which we assume here, then:

$$t_{up} = t_{down} = t_1 \quad (6)$$

Likewise, let $t_2$ be the time spent from the last re-bounce ($k^{\text{th}}$) to the end of the integration time $\Delta T$. If no bounces occurs, then $t_2 = \Delta T$, and $t_1 = 0$. We can rewrite (4) as:

$$V_R = \left(\frac{i_{ph}}{C}\cdot t_1\right)k + \frac{i_{ph}}{C}\cdot t_2 \rightarrow V_R = \frac{i_{ph}}{C}\,\Delta T \quad (7)$$

since $\Delta T = t_1\cdot k + t_2$. In a similar way, it can be demonstrated that (7) is also true for $k$ odd. According to this equation, the relation between $V_R$ and $i_{ph}$ is linear.

Regarding optimal sensitivity, i.e. disconsidering noise effects, one can calculate it by the following equation [2], using the relation in (7):

$$S = \frac{dV_R}{di_{ph}} = \frac{d}{di_{ph}}\left(\frac{i_{ph}}{C}\,\Delta T\right) = \frac{\Delta T}{C} \quad (8)$$

The above equation yields the remarkable fact that the sensitivity is constant throughout the whole DR, as long as $\Delta T$ and $C$ are kept constant. Equations (7) and (8) are identical to those derived for the conventional APS topology in [2].

*B. Pixel Architecture and Analysis*

The unit cell (Figure 2) is composed of a few transistors based on the CMI topology. Further, the off-pixel components are shared by all pixels of one, or more, columns of an imager. These shared components consist of a comparison unit, a counter, a shift register and an integration capacitance, as seen in Figure 3.

The CMI pixel topology simplifies the internal and automatic control of the pixel, allowing the external control of the matrix to be very simple and conventional. It just needs two signals: the reset, for the pixels; and the clock, for the digital circuit of each column. Both of them are global, and the integration period ΔT, controlled by the reset, can be kept fixed, obtaining constant sensitivity throughout the full illumination range, as reported earlier. If needed, the integration time can be easily modified, preserving the same DRF, but modifying sensitivity and DR. Generally, for a constant *C*, shrinking $\Delta T$ will increase DR, and decrease sensitivity (and vice-versa). So, there must be a compromise. The circuit also needs a control signal for each cell on a row, the select signal (Line), which enables the output of each pixel.

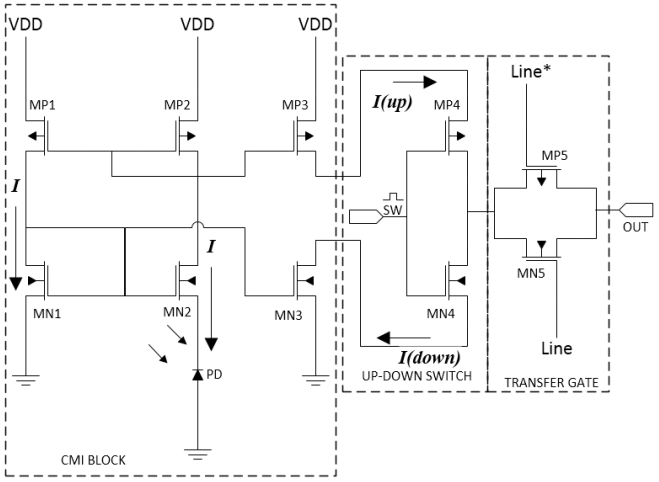


Fig. 2. CMI based pixel

*Circuit operation:* the photocurrent generated by the photodiode PD passes through MN2 and is mirrored to MN1 by the current mirror formed by MP1-MP2. But, since MN1 and MN2 are also connected as current mirrors, their gate-to-source voltage are forced to be the same, resulting in an almost-zero detector bias. To apply a stable non-zero bias through the PD, one must simply substitute the source connection of MN1 to a DC supply, instead of connecting it to the ground. Furthermore, this structure also results in low input impedance. Hence, most of the photocurrent generated by the PD is injected into the circuitry, even when the detector has low resistance. Transistors MN3 and MP3 are responsible for copying the photocurrent to the "up-down switch" formed by MN4-MP4. Basically, this switch selects which current will be delivered to the output through using the transfer gate (MN5-MP5). Both photocurrents have the same absolute value, but they are in opposite directions. When the digital internal control signal SW is low, then the current I(up) copied by MP3 passes to the output of the unit cell, and is integrated by the off-pixel capacitor *Cx*, shown in Figure 3. When the voltage $V_{cap}$ on the capacitor reaches the upper reference $V_{max}$, the first comparator sends a signal to the latch (NAND1-NAND2), which generates automatically the signal SW. That will be now high, and the "up-down switch" will now allow the current I(down) mirrored by MN3 to flow. Further, the capacitor will start to discharge until its voltage $V_{cap}$ reaches the bottom reference $V_{min}$, which sets SW to low again. This process repeats itself until the end of the integration period, defined by the signal RESET.

When the RESET signal is low, then the integration time starts, and during this period the counter will count at every edge of SW, i.e. every time the signal $V_{cap}$ reaches the top or the bottom reference. The two logic gates (INV1 and NOR1) between SW and the input clock of the counter is just to make sure that the counter will stop to count, after the last rebounce (when MAX is set to high). The counted value is then transferred to the Shift Register, which will write it out when RESET goes from low to high.

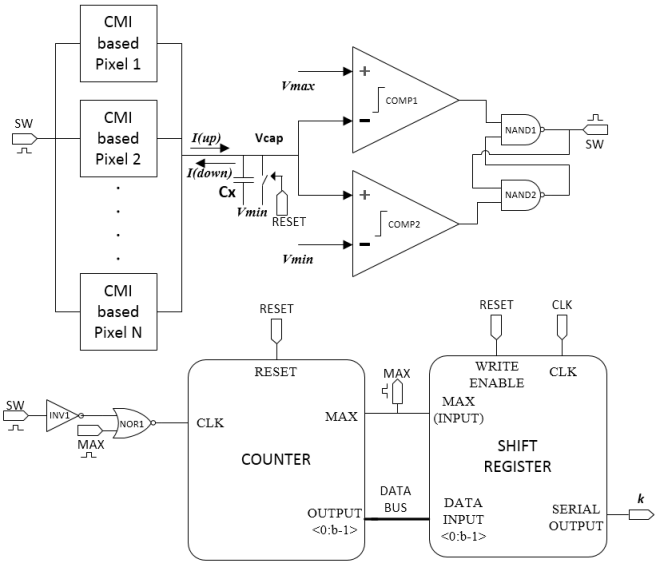


Fig. 3. One (or more) Column shared circuit.

In fact, the Shift Register has $b + 1$ bits, in order to read also the MAX bit, otherwise information of whether the pixel saturated or not would be lost, and would not have any difference in the final value between a very high photocurrent and a very low. After writing the counter value in its internal registers, the Shift Register starts to shift its value to the serial output at every cycle of clock (CLK). At the beginning it sends a start signal, composed by a binary 10, after that, it delivers the MAX bit followed by the other *b* bits. Before the end of the high period of the RESET, which has to be large enough to allow all bits to be transferred, the $V_{cap}$ value must be read, and the pixel operation is completed. As all pixels in one or more columns share the same components, the imager operates in rolling shutter mode.

As said before, the circuit has a linear response as can be seen in Figure 4, with photocurrents varying from 10pA to

8μA. This leads to a high DR reaching 118dB.The chosen parameters of the depicted example are: b=8, $V_{min}$=0.5V, $V_{max}$=2.5V, and $V_{DD}$=3.3V. The voltage difference $\Delta V$=$V_{max}$-$V_{min}$ is arbitrary. Increasing it, results in higher DR, but can also lead the capacitor to operate in a slightly non-linear region, affecting the final response, so there must be a compromise. The capacitance used was $C = 1pF$.

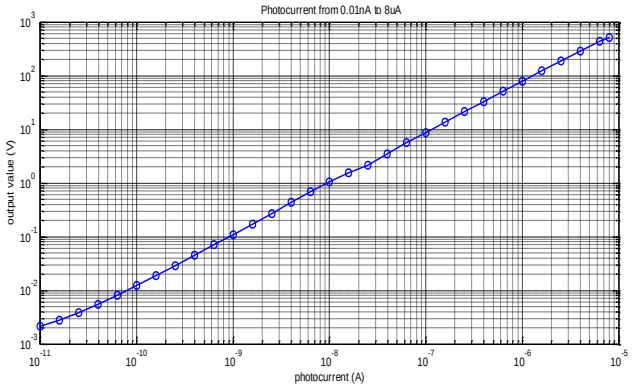


Fig. 4. Linear response through DR, from 10pA to 8μA, leading to DR=118dB. The output value in the y-axis is equal to $V_R$.

The response of figure 4 is the raw data extracted by the arithmetic equation described by (4) and (5). It is possible to render its linearity even better with some additional software corrections, but it is not the purpose of this work. Furthermore, the output value $V_R$ in Figure 4 is not the actual voltage across the capacitor, but the one that would have corresponded to full current integration if re-bouncing was not done and the supply voltage was not limited.

## III. Conclusion

In the present work, we have introduced an alternative approach for HDR image sensors. The bouncing pixel does not seem to fit in any of the seven categories presented in [2]. Simulations of the proposed pixel topology, designed in the AMS CMOS 0.35μm technology were presented to validate the concept. The pixel has constant sensitivity throughout the full illumination range, and at the same time, achieves a high DR of 118dB with just a single sample, making it possible to reach higher frame rates, and providing a linear response, allowing a homogeneous contrast reproduction over a scene. Moreover, the whole process to obtain the output value, and thus, the final processed image, can be automatically done, with no need of additional line control, nor any user input, achieving an always-on HDR image.

The pixel layout was already designed, and sent to fabrication. Further improvements and practical results will be presented in future work.

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