A Fully Depleted Backside Illuminated CMOS Imager with VGA Resolution and 15 micron Pixel Pitch

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Abstract – Presented is the development of a monolithic backside illuminated CMOS image sensor with a resolution of 640 x 512 pixels, fabricated on high resistivity silicon. Wafers with fully processed CMOS circuitry on the front side are thinned and a backside contact is added. By applying a bias voltage of 100V to this backside contact, the up to 200 micron thick silicon membrane can be fully depleted and a quantum efficiency up to 60% at a wavelength of 1000nm be achieved. The vertical PIN photodiode is predicted to have a characteristic response time of 2.8 nsec at that thickness and bias voltage, a bulk limited dark current of 4nA/cm^2 at room temperature and can be read out with very little noise due to its small specific capacitance of only a few aF/pixel. With the implemented charge domain 2x2 binning the signal to noise ratio increases by a factor 4, just like in CCD's. Different from CCDs though, also the frame rate increases by a factor 4 in our CMOS sensor. The highly programmable device can be read out through 1, 2, 4 or 8 analog output ports supporting frame rates up to 1000Hz at full resolution or 4000Hz at the binned resolution of 320x256 pixels. Electronic snapshot shuttering with less than 100nsec exposure time is possible with the integrated correlated double sampling shutter pixel.

Index Terms – Monolithic Scientific CMOS Sensor, NIR Response, High Speed Imaging, Low Noise Readout, High Resistivity Silicon, Binning

1. Introduction

Backside illumination has become the preferred approach for high resolution CMOS image sensors with small pixels targeting consumer applications like cell phone or web cameras. These image sensors are manufactured using special CMOS processes that offer pinned photodiodes with transfer gate to minimize dark current, readout noise and pixel size [1]. The combination of high light sensitivity with low noise, achievable because of these unique devices and processes, makes it possible to fabricate image sensors with a dynamic range sufficient for consumer cameras and pixel dimensions as small as 1 micron. Also, single electron noise performance, achievable with such CMOS sensors, has led to the development of low light level cameras, serving applications where traditionally electron multiplication CCDs or APD arrays are used.

Despite these significant advances, pixel arrays fabricated using state of the art 4T BSI CMOS image sensor processes, have some fundamental limitations that make them unsuited for many scientific applications, i.e.:

- Low sensitivity in the NIR range between 750 – 1100nm
- Slow signal response leading to image lag
- Cross talk, especially for larger pixels and longer wavelengths
- Not suited for direct detection of high energy radiation like x-rays or minimum ionizing particles (MIP)

Cross talk issues are overcome in commercial BSI imagers by depositing micro lenses on the backside. But because these lenses are made of organic materials, they shield shorter wavelength light, making the resulting device insensitive in the UV range.

The root cause for the listed limitations is the fact that CMOS ICs are made using low resistivity silicon where no deep charge collection regions can be established around a PN junction or photogate. The photosensitive silicon region in conventional CMOS BSI imagers is therefore only a thin membrane with a thickness of a few

microns. To overcome these limitations, high resistivity float zone silicon is used to realize scientific imagers like fully depleted BSI CCDs [2], hybrid FPAs [3] or 3D IC chip stacks [4]. In order to match and exceed the performance of these scientific devices at significantly lower manufacturing cost, we used the same material for monolithic integration in a 0.18um CMOS process [5]. In this paper the technology and design of a fully depleted backside illuminated scientific CMOS imager is described.

2. Technology Overview

A cross section illustrating the fundamental device structure of our high rho BSI pixel is shown in Figure 1. Just like in a low resistivity CMOS imager, active readout circuitry and the charge collection region PD are located within a thin layer on the front side. However, an electric field extends from PD to the backside through the thick, fully depleted silicon membrane and all charge carriers generated by photon impinging anywhere on the backside are collected, corresponding to an effective fill factor of 100%.

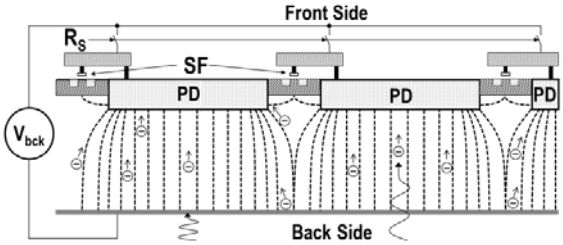

Figure 1 *Simplified pixel cross section of the presented fully depleted backside illuminated CMOS image sensor. A backside bias V_{bck} must be applied to achieve full depletion. R_s – Reset transistor, SF – Source Follower, PD – photodiode.*

The maximum possible depletion layer thickness is a function of silicon resistivity and applied backside bias (Figure 2) and defines the quantum efficiency especially for wavelengths in the NIR domain (Figure 3). Although a depletion depth of 400 micron can be reached with a backside bias of 100V, we chose the maximum thickness for our device to be 200 micron to limit dark current and cooling requirements, respectively (Figure 4). The reverse bias voltage required for full depletion is significantly below the breakdown voltage for silicon. It is therefore possible to over bias the described photo detector and accelerate signal charge into the front side collection node. Shorter vertical drift times of photo generated charge carriers will reduce lateral diffusion and thereby lead to improved MTF performance in a PIN type pixel array as expressed by the charge spread value in Figure 5.

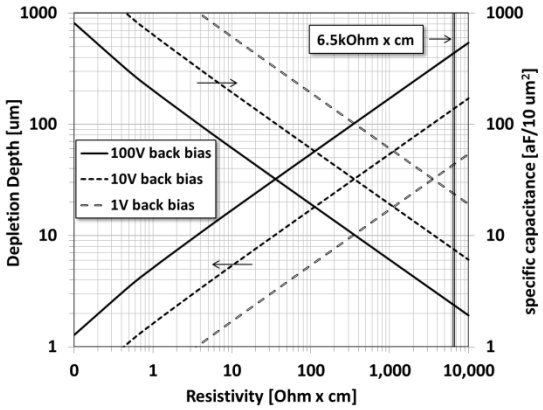

Figure 2 *Depletion layer width of PIN photodiode as a function of silicon resistivity. Right axis shows corresponding specific capacitance. The presented imager was integrated on 6.5kOhm x cm Si. Note that the PD capacitance at this resistivity and pixel size of 15μm is so small that practically all signal charge is integrated on the discrete capacitor C_{int}.*

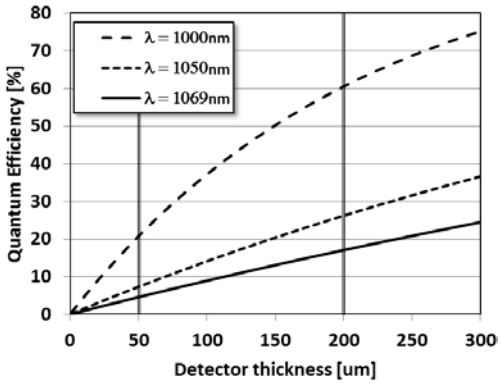

Figure 3 *Maximum achievable quantum efficiency as a function of detector thickness for 3 NIR wavelengths: λ=1000nm, 1050nm and 1069nm. Vertical lines indicate thicknesses of designed devices.*

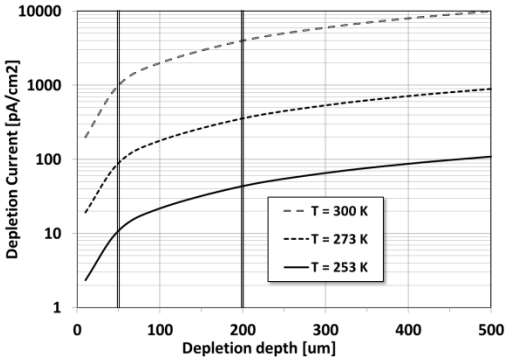

Figure 4 *Predicted depletion current (the dark current limit for a fully depleted BSI imager) as a function of depletion depth for temperatures T=253K, 273K and 300K. The two vertical lines indicate the thicknesses to which the designed device is thinned. At room temperature the dark current for a 50μm (200μm) thick detector is 1nA/cm^2 (4nA/cm^2).*

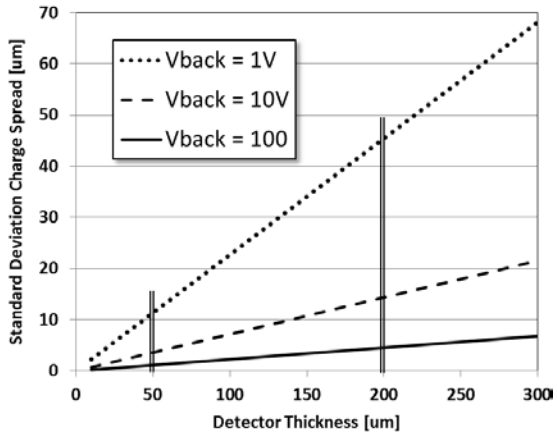

Figure 5 *Charge spread as a function of detector thickness for back bias voltages of 1V, 10V and 100V. The described imager is thinned to 50 and 200 μm thickness. The charge spread is a measure for the smallest possible pixel with Nyquist limited MTF performance. At 200μm detector thickness and 100V back bias the charge spread is only 4.5μm.*

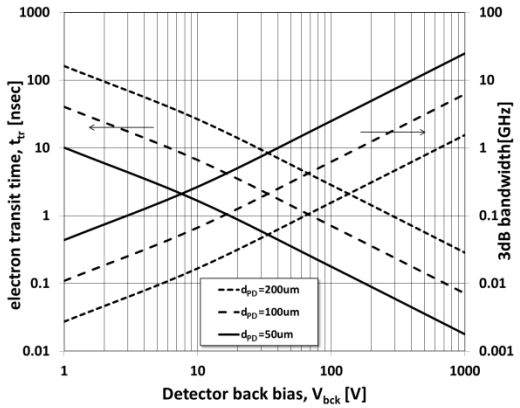

Figure 6 *Electron transit time and corresponding 3dB bandwidth for fully depleted photodiodes as a function of backside bias voltage V_{bck} and imager thickness d_{PD}. For a 100um thick detector with 100V back bias the transit time is 0.7 nsec corresponding to a 3dB bandwidth of 625MHz.*

The electron transit times for thick, fully depleted Si photo detectors is shown in Figure 6. For a 100 micron thick detector with 70V back bias, the electron transit time is only 1nsec, making a corresponding pixel array well suited for imaging applications with nano second time constants.

3. Pixel Design

The pixel schematic is shown in Figure 7. It is based on a floating diffusion readout followed by an analog memory block to store reset and (signal + reset) value. 4 storage capacitors were integrated in each pixel so that an integration time window can be placed anywhere within a frame readout window with no constraints from signal or reset value settling aspects. The circuit supports row individual programmable full well capacity, snapshot shutter functionality with integration times as short as 100nsec and low noise Correlated Double Sampling (CDS) readout. The corresponding pixel timing is explained in Figure 8. Readout of each row consists of memory node reset followed by transferring reset and signal values from C_1 and C_2 into the column amplifier, where they are subtracted from each other to create an offset free low noise output signal.

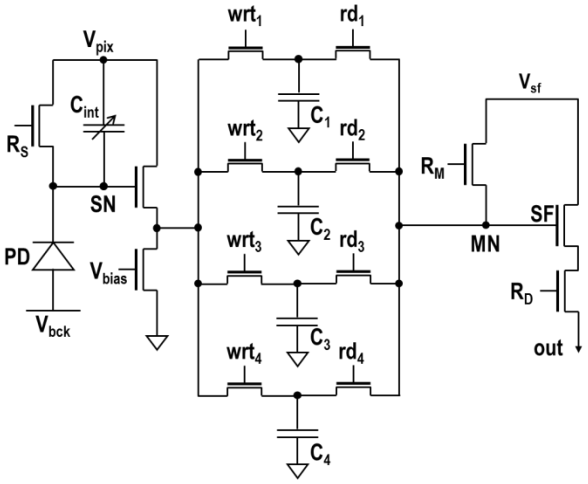

Figure 7 *Pixel schematic for PIN photodiode readout supporting programmable full well capacity, snapshot shutter functionality, Correlated Double Sampling (CDS) and integration times as short as 100nsec (with corresponding adjustment of V_{bias}).*

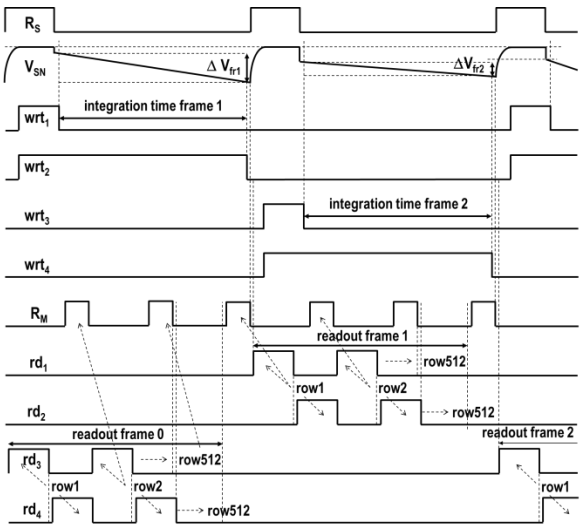

Figure 8 *Timing diagram for signal integration and readout of the pixel described in Figure 4. Reset values from odd (even) numbered frames are written to C_1 (C_3) memory when wrt_1 (wrt_3) is high. (signal+reset) values from odd (even) numbered frames are written to C_2 (C_4) memory when wrt_2 (wrt_4) is high. Readout of reset values is controlled by rd_1 (rd_3), readout of (signal+reset) values by rd_2 (rd_4) for odd (even) numbered frames. The difference between reset and (signal+reset) value is calculated in the column amplifier, resulting in an output signal with no kTC noise.*

4. Imager Design

The sensor requires 4 external digital clock signals, i.e. “frame”, “line”, “exp” and “clk” to control readout, integration time window, regions of interest and frame rate. All other signals for row and column addressing as well as clocking of the fully offset compensated readout chain are generated on-chip. Bias conditions and operating modes are programmed via serial interface.

In a fully depleted photodiode sensor array, pixels can be binned in the detector itself by selectively suppressing the reset. This causes photodiodes without reset to become de-biased and all photo generated charge carriers to be collected by pixels with reset. For readout, binning rows “bin_{row}<i>” are defined as illustrated in Figure 9. There are as many pixels in a binning row as in a regular row but the ratio of regular rows to binning rows per frame is equal to the number of binned pixels. Therefore the frame rate increases proportional to the number of binned pixels.

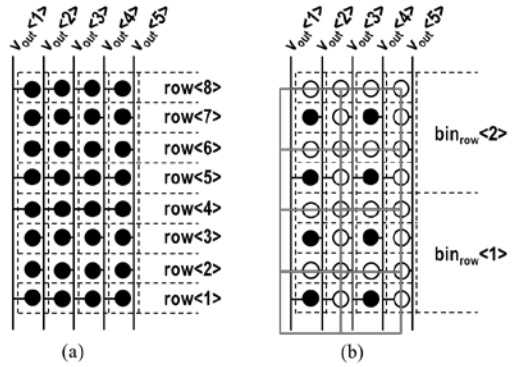

Figure 9 *Pixel array identifying rows and vertical output bus lines v_{out} in full resolution (a) and 2x2 binning mode (b). Black circles represent signal integrating pixels, white ones non-integrating pixels. Grey squares in (b) indicate the effective charge collection region in 2x2 binning.*

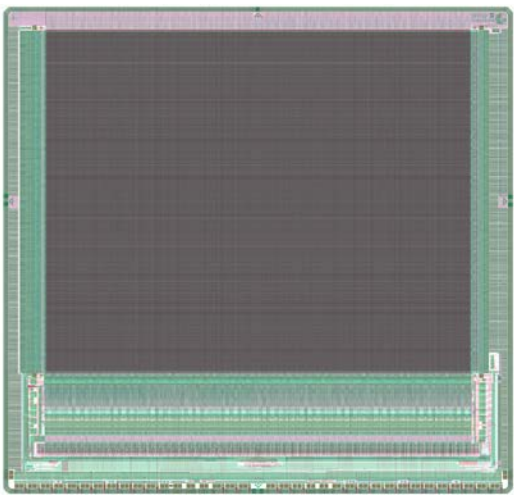

Figure 10 *Layout screenshot of the designed BSI image sensor. The IC has a size of 12 x 12mm^2. All I/O pads are arranged along the bottom edge of the chip.*

5. Summary

The development of a monolithic fully depleted backside illuminated CMOS imager for scientific applications was presented. A layout screenshot of the sensor that is presently in fabrication is shown in Figure 10. Design parameters are summarized in Figure 11.

Parameter	Value
Array Format	640x512
Pixel Size	15um
Die Size	12 x 12 mm^2
Frame rate	30Hz, 60Hz, 240Hz, 1000Hz
Master Clock	5 MHz, 5MHz, 20MHz, 41 MHz
Number outputs	1,2,4,8
Shutter type	global shutter
Integration modes	ITR, IWR, HDR, NDR
Exposure time	100nsec to 30 msec
Charge capacity	500ke, 60ke, 10ke
Minimum Noise	< 10e$^-$
QE at 1050nm	> 25% for 200nm thick Si
Binning	2x2, 1x2, 2x1
Output type	analog
Power	60 mW @ 60Hz frame rate
Supply Voltages	1.8V/3.3V
Serial interface	3 wire

Figure 11 *Predicted Specifications for the presented fully depleted backside illuminated imager on high resistivity silicon.*

6. References

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