On The Pixel Level Estimation of Pinning Voltage, Pinned Photodiode Capacitance and Transfer Gate Channel Potential

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***Abstract*—The pinning voltage extraction method proposed by Tan *et al.* is analyzed to clarify its benefits and limitations. It is demonstrated that this simple measurement can bring much more useful information than the pinning voltage, such as the pinned photodiode capacitance and the transfer gate channel potential. Objective criteria to compare the pinning voltage on different devices are also discussed.**

I. Introduction

THE pinning voltage ($V_{pinning}$) is one of the most important parameters that define the structure of a Pinned Photodiode (PPD). As for the determination of channel potential in CCDs [1], it is well established that isolated test structures (such as the one simulated in [2]) can be used to estimate this parameter. Such structures are not always available or representative of the PPD shape and environment in the sensor of interest. A method to evaluate $V_{pinning}$ and other fundamental parameters (such as the PPD capacitance and Transfer Gate (TG) channel potential) directly at the pixel level (at the sensor output) would be an important benefit for CMOS Image Sensor (CIS) process development, PPD design optimization, modeling and characterization. This is especially true for radiation related applications (space, nuclear, medical…) since it has been recently shown that ionizing radiation can change the pinning voltage of PPD CIS [3] and since users have generally not access to pinning voltage test structures during irradiation test campaign.

In this work, we propose to analyze the benefits and limitations of the $V_{pinning}$ extraction method recently proposed by Tan *et al.* [4]. We demonstrate that, in addition to the pinning voltage estimation, this characteristic can be used to evaluate the pinned photodiode capacitance, and in some cases, to extract the channel potential evolution with TG voltage. After the detailed description and analysis of the characterization method, its benefits are illustrated by comparing the responses achieved after design variations and technological variations.

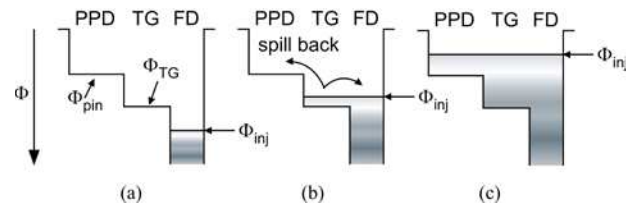

Fig. 1: Simplified electrostatic potential (Φ) diagram of the PPD, TG and FD for three injection bias conditions: (a) when $\Phi_{inj} > \Phi_{TG}$: no injection, (b) when $\Phi_{pin} < \Phi_{inj} < \Phi_{TG}$: partial injection due to possible charge spill back (c) when $\Phi_{inj} < \Phi_{pin}$: direct injection of charges into the PPD.

II. Studied Device Details

Except the ones used for the last figure, all the studied sensors are 256×256-4T-PPD-pixel-arrays manufactured with a widely used commercially available 0.18 µm CIS foundry. All the measurements have been performed in the dark at room temperature. Each data point of the presented plots represents an average value resulting from a spatial average over the 256×256 pixels and from a temporal average over 100 frames. The injection pulse has been chosen long enough (≈50 µs) to ensure that the injection voltage was properly applied on the Floating Diffusion (FD).

III. PPD Parameter Extraction

A. $V_{pinning}$ Extraction Plot Principle

The previously proposed $V_{pinning}$ extraction technique [4] is based on the injection principle illustrated in Fig. 1. It has been implemented here with the setup and the timing diagram shown in Fig. 2 and Fig. 3. Depending on the injection voltage V_{inj}, charges are injected into the PPD (Fig. 1c) or not (Fig. 1a). This is illustrated on the $V_{pinning}$ extraction plot in Fig. 4. When the injection potential is higher than the TG channel potential, there is no signal at the sensor output (no charge $Q_{out} = V_{out}/CVF$, CVF being the output conversion gain) whereas the output signal rises rapidly with decreasing V_{inj} when the injection potential is below $V_{pinning}$. Between these two regimes, a plateau appears on the characteristic. This plateau has not be reported in [4] and is attributed to charge

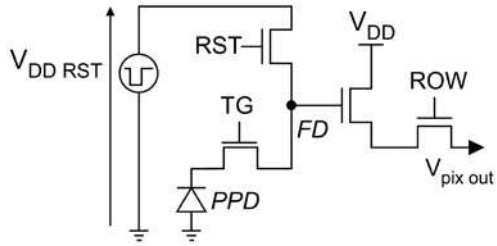

Fig. 2 : Test setup illustration. A pulse is generated on the V_{DDRST} supply line to inject charges in the PPD through the RST MOSFET and the TG. Only one pixel is represented for clarity purpose, but the V_{DDRST} line is connected to all the pixels of the tested image sensor.

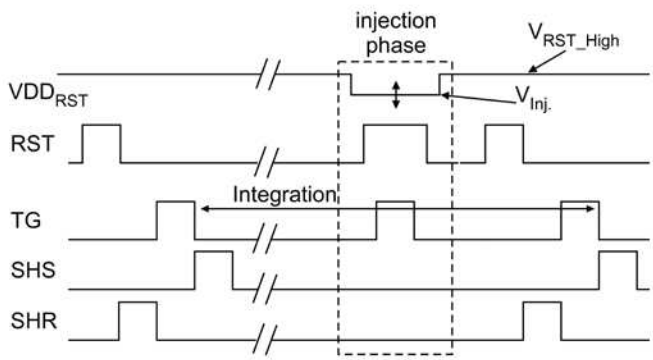

Fig. 3 : Simplified timing diagram. The charges are injected into the PPD at the end of the integration phase (injection phase) by lowering V_{DDRST} to Vinj and pulsing TG. In order to transmit properly the V_{DDRST} voltage pulse to the capacitive V_{DDRST} bus, a long V_{DDRST} pulse is used during the injection phase (≈50 µs).

spill back [5] from the TG to the PPD as illustrated in Fig. 1b. Several reasons may explain why it has not been reported before. First, the spill back charge usually represents only a small fraction of the full well charge, and one needs to focus on this region to observe this plateau. Another possible reason is the existence of a potential barrier in the device tested in [4] that prevents spill back and thus that would inhibits this regime. It could also be due to the use of V_{inj} values that are not high enough to reach the regime of case (a) in Fig. 4. In this case, the transition from (a) to (b) would not be visible and thus, the plateau would not be observable.

B. *Influence of TG Voltage and Channel Potential Estimation*

The first non-ideality considered in this study is the possible effect of the TG voltages on the extracted pinning voltage value. Fig. 5, Fig. 6 and Fig. 7 show that the TG ON and TG OFF voltages (respectively V_{HITG} and V_{LOTG}) have almost no effect on the injection region where $V_{pinning}$ is evaluated. However, as expected, V_{HITG} has a direct influence on the V_{inj} value at which the spill back phenomenon occurs (Fig. 6). This particular V_{inj} value corresponds to the TG channel potential, and it can be used to draw the TG channel potential evolution with TG gate voltage (as shown in the inset of Fig.6). This is very convenient to characterize the transfer gate or to monitor his health when exposed to stress sources (e.g. radiation).

Fig. 7 confirms that when V_{LOTG} is reduced, the amount of charge that can be stored in the PPD increases, until reaching the accumulation regime (for V_{LOTG} around -0.5V here).

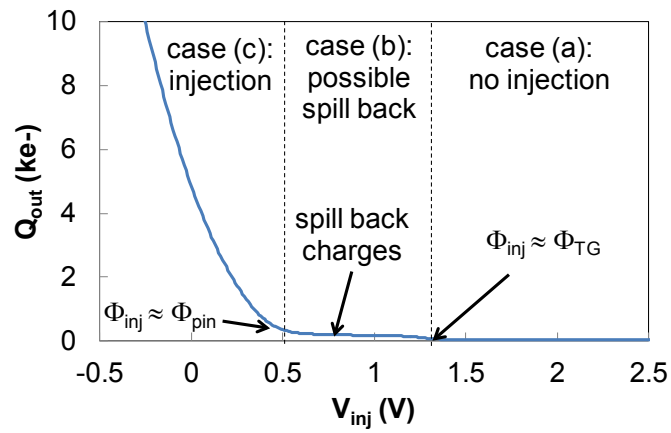

Fig. 4: $V_{pinning}$ extraction plot: PPD charge (Q_{out}), measured on the FD (average value on the whole pixel array), as a function of the injection voltage V_{inj}. The three regime discussed in Fig.1 are presented (regimes (a), (b) and (c)). Sensor details: 256x256 4.5 µm pitch pixel array, PPD CIS 0.18µm technology, 4T-PPD pixel, CVF ≈ 80µV/e-.

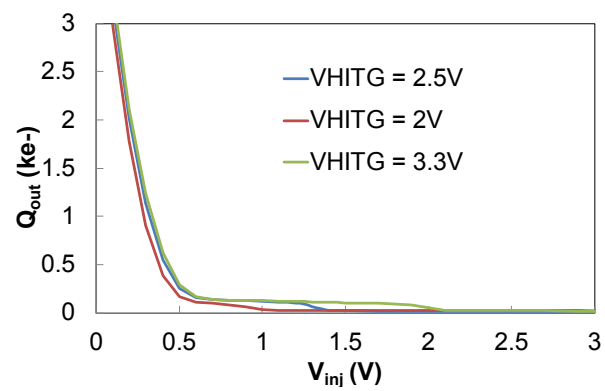

Fig. 5: V_{HITG} effect on the $V_{pinning}$ extraction plot. Despite a wide range of V_{HITG}, only a very weak effect on the "injection region" where $V_{pinning}$ is evaluated can be observed, whereas the V_{inj} voltage at which $\Phi_{inj} = \Phi_{TG}$ is significantly shifted with V_{HITG}. Same sensor as Fig. 4.

C. *PPD Capacitance Determination*

The PPD capacitance can also be directly extracted from the $V_{pinning}$ extraction plot (see Fig. 8), simply by computing the first order derivative ($C_{PPD} = dQ_{out}/dV_{inj}$ in the injection regime: case (c) in Fig. 4). Fig. 8 shows that the C_{PPD} value is only valid between the "smooth transition region" (for $\Phi_{inj} \approx \Phi_{pin}$) and the regime in which the readout chain approaches its saturation. This technique allows to observe the evolution of the PPD capacitance with the filling level of PPD.

D. *Limitations Associated to $V_{pinning}$ Evaluation*

The pinning voltage should correspond to the V_{inj} value at which the injected charge starts to increase (called the knee voltage in [4]). There are several limitations associated to this approach. First, the transition from the "spill back regime" (case (b) in Fig. 1 and Fig. 4) to the injection regime (case (a)) is pretty smooth (most-likely because of thermo-ionic emission) and one needs to define a clear criterion to measure $V_{pinning}$. One possible way is to take the X-intercept of the asymptote at V_{inj} = 0V. This objective criterion can be used to compare the pinning voltage of different pixels, but it may underestimate the real pinning voltage value because of the increase of PPD capacitance with increasing filling level (i.e.

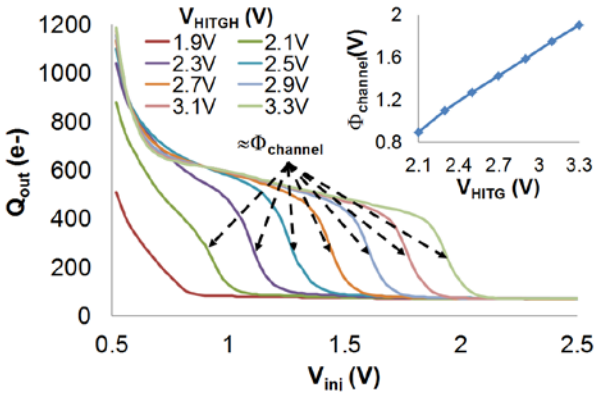

Fig. 6: V_{HITG} effect on the "spill back regime" (case (b) in Fig. 1). The inset shows the extraction of the TG channel potential (estimated at Q_{out} = 300 e-) as a function of the TG gate voltage V_{HITG}. Same sensor as Fig. 4.

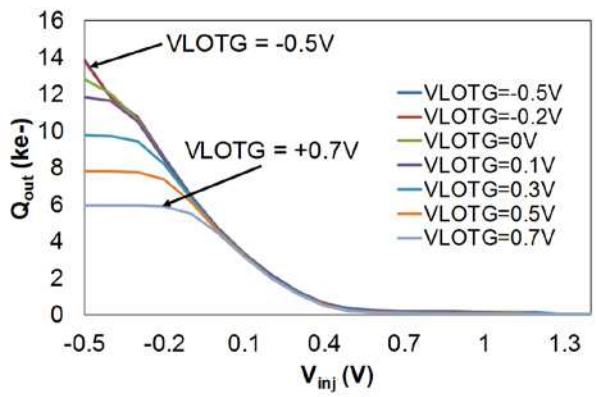

Fig. 7: V_{LOTG} effect on the $V_{pinning}$ extraction characteristics. V_{LOTG} only changes the maximum amount of charge that can be stored into the PPD. When V_{LOTG} is low enough (< -0.1 V), the TG is accumulated, its surface potential is pinned to 0V and there is no more effect of the TG voltage on the FWC. Same sensor as Fig. 4..

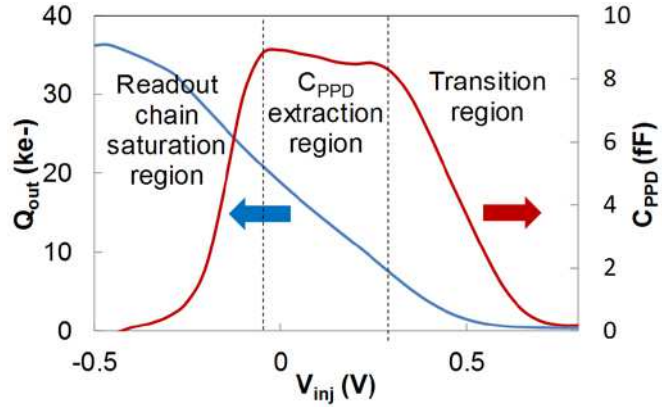

Fig. 8: $V_{pinning}$ extraction characteristics and extracted PPD capacitance as a function of the injection voltage on a 7µm pitch 4T pixel sensor (0.18 µm CIS foundry). The saturation charge achieved for V_{inj} = -0.5V corresponds to the saturation voltage of the readout chain. The extracted PPD capacitance is the first order derivative of the $Q_{out} = f(V_{inj})$ curve. Due to the saturation of the readout chain and the transition region non-ideality, the capacitance extraction is only valid between V_{inj} = -0.1 and +0.3V.

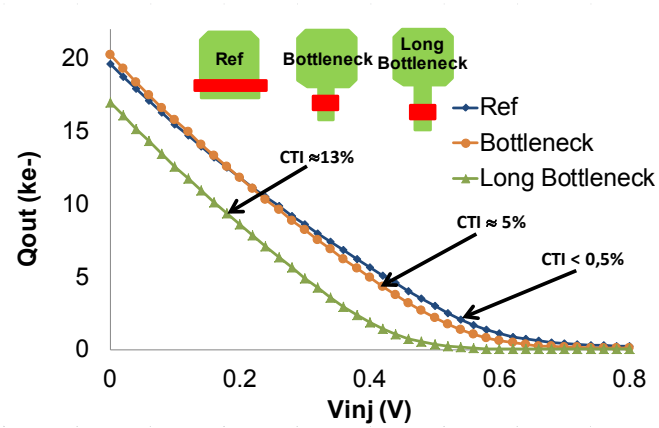

Fig. 9: $V_{pinning}$ extraction plot measured on three different pixel designs with the same pinning voltage and different lag performances (i.e. CTI values).

decreasing V_{inj} value). Despite this limitation, this criterion appears to be accurate at least for relative comparisons.

The existence of a potential barrier could also possibly have an influence on the extracted pinning voltage value. Fig.9 presents the pinning voltage characteristics measured on three different pixels of the same test sensor, with the same PPD (same size, same pinning voltage) but with different TG designs. The reference design exhibits no image lag and it is assumed that there is no significant potential barrier in this pixel. In the other two, the PPD and the TG have been narrowed to create a bottleneck and to generate an important potential barrier leading to important charge transfer inefficiency (CTI): up to 13%. It should be emphasized that the CTI is measured here with only one TG pulse per frame, artificially leading to higher CTI values than the one usually reported on commercial sensors with the use of more than one TG pulse per frame [3].

It can clearly be seen in Fig. 9 that this inefficiency shifts the characteristics toward lower voltage values leading to an underestimation of the pinning voltage. This underestimation is roughly equal to the CTI value, and thus, one can conclude that as far as CTI is below a few percent (which is generally the case in optimized pixels), potential barriers have only negligible effects on the extracted $V_{pinning}$ value.

E. Application to Design and Process Variations

As an illustration, this method is applied to pixels presenting design variations (PPD area) in Fig. 10. There is a clear change of slope, indicating a change of PPD capacitance (obviously due to the change of area), but it is very difficult to decide whether the pinning voltage is different or not based on the "knee voltage criterion" used in [4]. Fig. 11 shows the extracted capacitances (on the validity range discussed previously). These capacitances slightly rise with decreasing injection voltage (as expected for a PN junction) and the Fig. 11 inset shows that the area capacitance can be determined from these measurements (~1.2fF/µm²). The apparent decrease of capacitance for decreasing V_{inj} on the last points of the 9.5µm² and 7.5 µm² photodiodes is due to the influence of the readout chain saturation.

Once the capacitances have been determined, it is possible to normalize Fig. 10 by the capacitance at V_{inj} = 0V (or at 0.25 V for the 9.5µm² diode, since this pixel is saturated for V_{inj} = 0V) to compensate for the change of slope. The results, shown in Fig. 12, confirm that the design variations studied here have

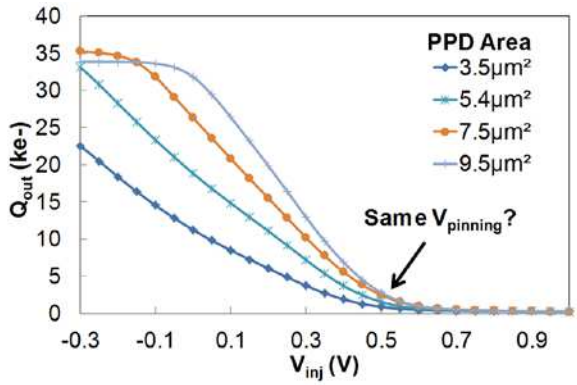

Fig. 10: Design effect on the $V_{pinning}$ extraction characteristics. It is difficult to make a relative comparison of the pinning voltages because of the different slopes (i.e. capacitances). The PPD perimeter of the tested pixels is fixed and equal to 14µm. Pixel pitch =7µm. CIS 0.18 µm process. V_{LOTG} = -0.5V. The observed saturations are due to the readout chain saturation

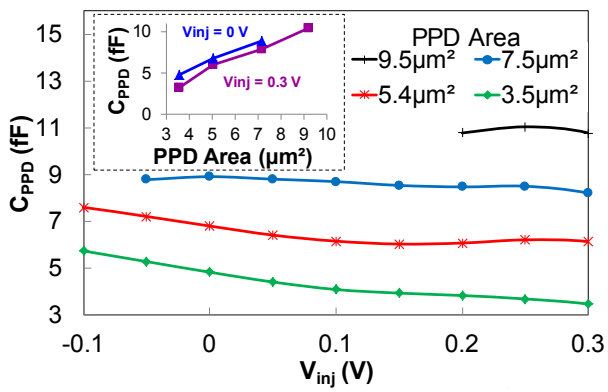

Fig. 11: Capacitance extracted from Fig.9 as a function of Vinj for several PPD areas. The expected linear area dependence is shown in the inset at two V_{inj} voltages. In both cases, the extracted area capacitance is about 1.2fF/µm². For the 9.5µm² and 7.5µm² areas, the data points below 0.2V and -0.05V respectively are not shown because they are located in the readout chain saturation region.

no effect on the pinning voltage (no geometric effect [6] here). Hence, normalizing by the capacitance value appears to be an efficient way to perform relative graphical comparisons of $V_{pinning}$ values (when the capacitance differs from one pixel type to another). Finally, the last plot shows that the effect of N_{PPD} doping concentration on the pinning voltage can be easily evaluated with this technique. The expected results are observed: the pinning voltage increases when the implantation dose increases. It is also interesting to notice that the E = 50%, Dose = 300% plot exhibit a much more intense spill back regime than the other three.

IV. Conclusion

We have shown that despite some limitations due to the difficulty to select an objective criterion and to the existence of a potential barrier, the pinning voltage extraction voltage proposed by Tan *et al.* appears to be a very powerful tool. First, we have not observed any experimental evidence of a bias on the absolute value of the extracted $V_{pinning}$. In any case, once an objective criterion is used to determine $V_{pinning}$, or once the characteristics has been normalized by the PPD capacitance, this method appears to be really accurate for

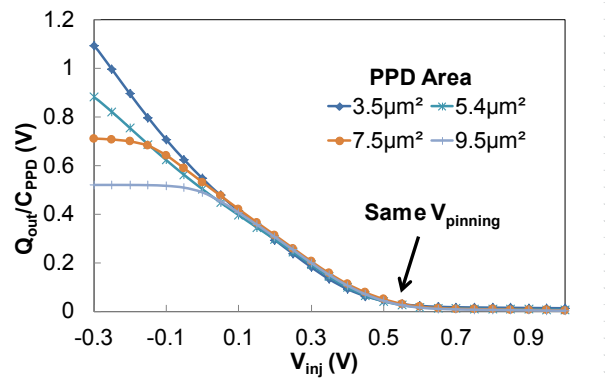

Fig. 12: $V_{pinning}$ extraction characteristics of Fig. 9 normalized by the capacitance of Fig. 11 at V_{inj} = 0.3 V. The relative comparison of $V_{pinning}$ voltage is now possible and we can see that there is no area effect here.

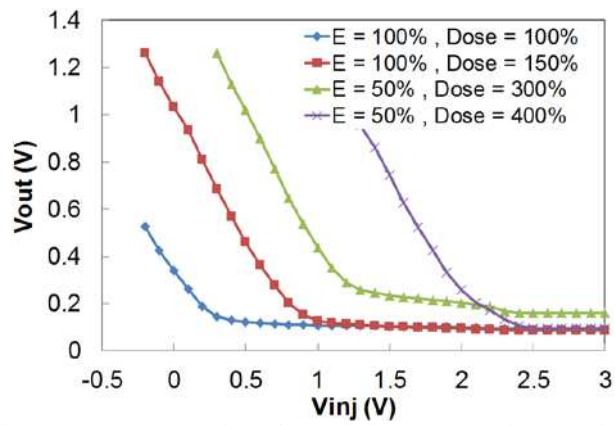

Fig. 13: $V_{pinning}$ extraction characteristics for several N_{PPD} doping concentration. CIS technology under development.

relative comparison (e.g. design/process variations).

It has been shown that a spill-back regime appears on this characteristic and that he can be used to analyze the structure of the PPD. We have also demonstrated that much more than the pinning voltage can be extracted from this plot. The PPD capacitance value (as a function of the filling rate of the PPD) can be retrieved from the slope of the curve, whereas the TG channel potential at a given TG voltage can be determined by detecting the beginning of the spill back regime. This last result can be used to monitor the TG threshold voltage.

This study opens the door to detailed pixel level analyses of stress induced PPD/TG degradations (electrical, optical, hot carrier, radiation induced…) and many other studies where monitoring the parameters discussed here are of primary importance (PPD/TG modeling, process development…).

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