A Dual Exposure Method for Wide Dynamic Range Operation of CMOS Image Sensors

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Abstract: Although image sensor applications have seen considerable progress, industry requirements are also becoming more demanding as image technology in CMOS image sensors (CIS) is becoming more complex. The use of CMOS image sensors is recently starting to expand into DSLR cameras, medical sensors, and defense and space applications, which require a wide dynamic range of operation. While several decades of research have yielded advances in this area [1]-[3], further improvements are still needed. These include better resolution and higher speed for such new sensor markets as the automotive industry and security. This paper presents results of developing advanced wide dynamic range pixels using dual exposure image capturing.

Dual Exposure method: Various approaches to extend the dynamic range of CIS has been proposed. As shown in Fig. 1, the key concept of them is the use of nonlinear response by retarding the saturation of pixel using logarithmic behavior or knees introduction of well capacity adjusting during integration, otherwise multiple capture approaches. However, most of them are focusing on extending the dynamic range under high illumination. In order to enhance the dynamic range in high illumination as keeping on the availability of low noise, high sensitivity with 4T pinned photodiode Active pixel Sensor(APS), we approached dual exposure scheme during one integration period. The scheme of 4T pinned photodiode APS is shown in Fig 2. This Dual exposure image is captured by a hybrid pixel readout, which is a combination of 3T pixel and 4T pixel signal readout schemes. In this dual exposure image approach, a long exposure(LE)and short exposure(SE) response at each pixel are readout in a same horizontal term. SE is overflow signal accumulated in the FD region. So it is zero until PD is overflowed. SE behaves a linear response at lower signal and a log response at higher signal because of reset gate(RX) overflow characteristics. In this scheme a synthesized signal can be simply calculated as a sum of LE signal and SE signal at the one horizontal term, and it needs only one line memories. This scheme is shown in Fig. 3

Results and Discussions: Our WDR pixels were fabricated using 0.11μm CIS technology with 1poly 3Metals and a 2fF MIM capacitor option. 12bit column parallel ADC is also integrated in this prototype CIS. To realize fast conversion time using a relatively slow clock, 2 upper-bit successive approximation register(SAR) ADC is combined with 10.5 lower-bit single-slope ADC having redundancy. Frame rate of 45fps at 1280X960 and 60fps at 720p with twice ADC operation per horizontal period are realized at 135MHz of clock frequency. Typical ADC input range is 1.4V for pixel evaluation. Total noise of ADC is less than 1LSB. This pixel configuration generates two images at the same time. One is a conventional 4T pixel image captured during a long exposure time and the other is a 3T pixel image captured by reading out the overflowing charge during a short exposure time. The respective images are shown in Fig. 6(a) and (b). The synthesized WDR image can be created by combining 3T and 4T pixel readout images as in Fig. 6(c). And the dynamic range evaluation of conventional mode and proposed WDR mode was performed like in Fig 4. The result of WDR mode is 110dB and the other values is summarized in Table 1. The pixel characteristics of 4T pinned photodiode in our proposal were evaluated with photon transfer curve and Quantum efficiency, as shown in Fig 5.

Conclusion: This paper introduces a dual exposure image capture pixel scheme that does not require additional exposure time, which is suitable for high resolution and high speed wide dynamic range sensor applications. According to the result, this scheme can enhance the dynamic range in high illumination without the expense of low noise and sensitivity of 4T pinned photodiode.

References

[1] M. Mase, et al., IEEE ISSCC Dig. Tech. Papers, p.352, 2005. [2] M. Sasaki, et al., IEEE J Sensors, p7:151, 2007. [3] Y. Oike, et al., IEEE Trans. Electron Devices, 44 (10), p.1689, 1997. [4] J. Solhusvik, et al., International Image Sensor Workshop, 2009.

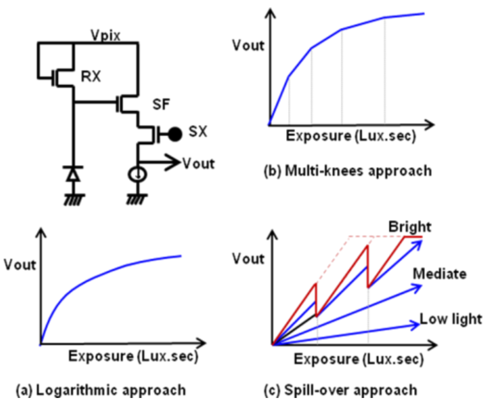


Fig.1. Representative schemes of Wide Dynamic Range

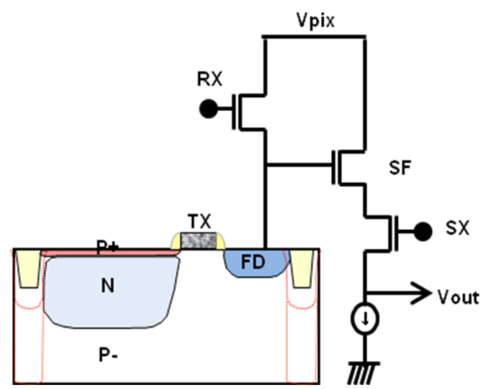


Fig. 2. The schematic of 4T pinned photodiode APS

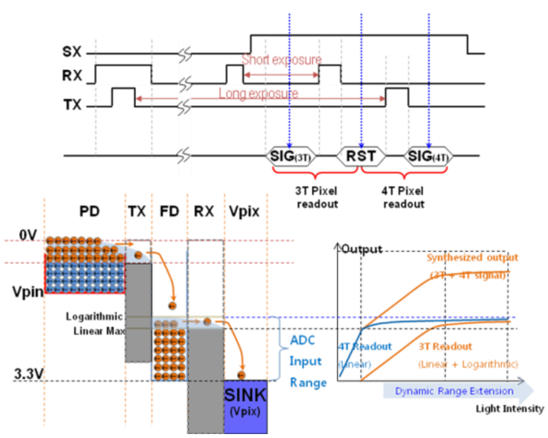
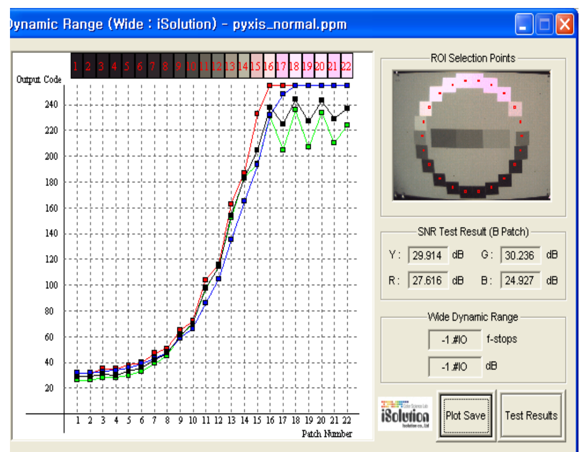


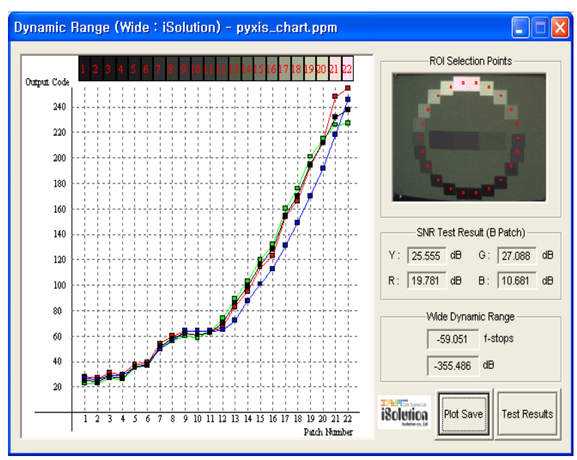
Fig.3. Timing and potential diagram of dual exposure



(a)

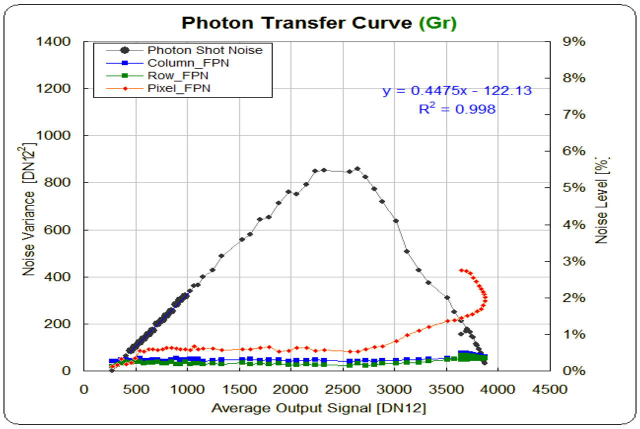
Parameter	Typical value
Optical Format	1/3 inch
Pixel Size	3.69um X 3.69um
Fabrication	0.11um 1Poly 3Metal
Shutter Type	Electronic Rolling Shutter
Array Size	1280(H) X 960(V)
Frame Rate	45fps@Full / 60fps@720p
ADC	12bit Column ADC on chip
Supply Voltage	1.5V(Digital) / 3.3V(Analog)
Sensitivity	4.21 V/lux.sec (G)
Dynamic Range	110dB
Temporal Noise	2.6e−
Average Crosstalk	16.6%
Quantum Efficiency	60% (Green)

Table. 1. The pixel characterization summary for the dual exposure image capture scheme



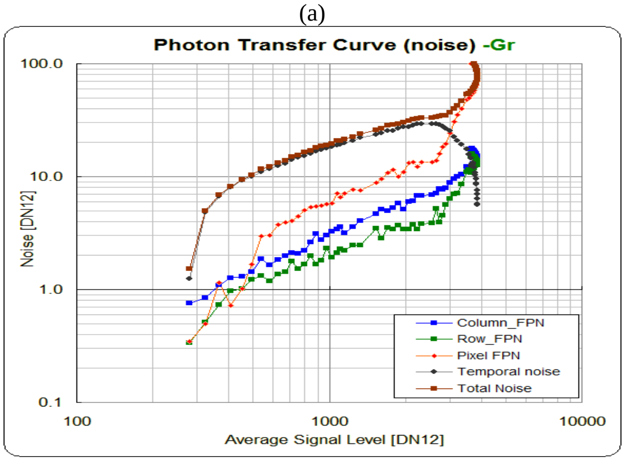
(b)

Fig 4. Dynamic Range measurement results using the specific transparent chart. (a) Conventional mode and (b) proposed dual exposure mode.

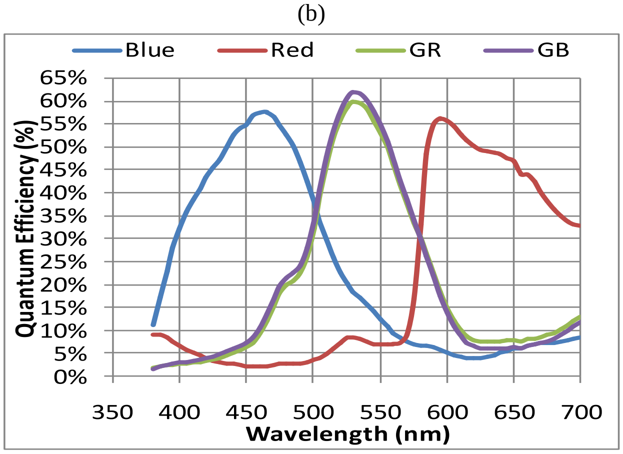


[note] DN12 : digital number of 12bit

(a)



(b)

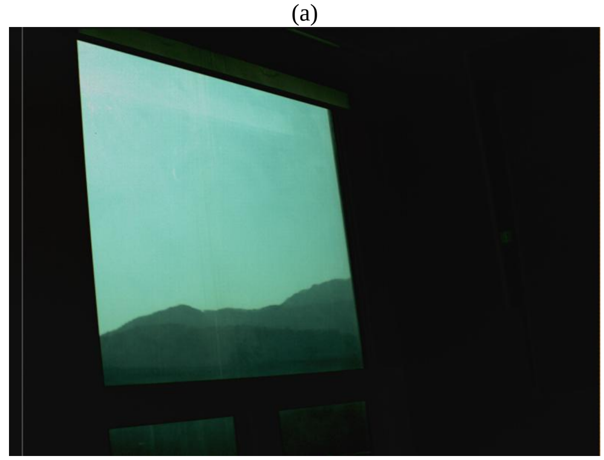


[note] GR: green pixel next to Red / GB: green pixel next to Blue

(c)

Fig. 5. (a) Photon transfer curve in linear scale (b) Photon transfer curve in Log scale, where the shot noise is dominant in l and (c) quantum efficiency of pixels with each color pattern.

(a)



(b)

(c)

Fig. 6. (a) 4T pixel readout image during long exposure time, and (b) 3T pixel readout image during short exposure time without extra exposure time overhead and (c) the synthesized image by combining the 4T readout image(a) and the 3T readout image(b).