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Single Slope ADC with On-chip Accelerated Continuous-time Differential Ramp Generator for Low Noise Column-Parallel CMOS Image Sensor

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Abstract
This paper presents a 12-bit single slope ADC architecture that uses an on-chip ramp generator for low noise column-parallel CMOS image sensor. An on-chip continuous-time ramp generator is used instead of a discrete-time implementation. This is to reduce the glitch noise caused by a high speed clocking of a discrete-time ramp. Differential topology is adopted to improve the power supply rejection (PSR) performance of the ramp generator. High speed ADC conversion is obtained with accelerated ramp signals by exploiting photon shot noise characteristics of image signals [1,2]. The ADC is designed to be highly scaleable and the architecture is used for a family of image sensors fabricated in TSMC 0.18um 3.3V/1.8V CMOS process. Measurements show a row noise of 13uV at gain 24x and 50uV at gain 3x. The total readout noise is 108uV at gain 24x and 171uV at gain 3x.

I. Introduction

In recent years, video has become pervasive and CMOS image sensors has become more and more popular in such applications as medical instruments, security cameras, mobile phones and automotive industry due to its low power consumption, high speed imaging and easy system integration with on-chip circuits. This has popularized the use of column-parallel ADC architectures that tend to improve frame rate, reduce power consumption and lower readout noise at high pixel resolutions. SS ADC has been widely applied in CMOS column-parallel image sensors because they provide relatively high resolution with minimal area and low power consumption.

The “ramp generator” is a critical building block for SS ADC’s. To operate properly, the ramp generator should provide stable reference to the ADCs. In order to reduce the readout noise, the ramping signal should be as low noise as possible and have good common mode rejection to filter power and ground modulation. In this paper, we present a 12-bit SS ADC architecture that uses an on-chip ramp generator designed specially with considerations of minimizing these noise sources.

II. SS ADC

Figure 1 shows the differential column sample-and-hold, preamp and comparator using a topology described in [3]. The input stage allows differential kTC noise cancellation for increased PSR. A front-end auto-zero phase allows the use of a high-gain preamp to reduce column fixed-pattern noise. When pixel signal and reset levels after PGA are being sampled, the preamp is put into auto-zero phase and the ramp generator is held in reset phase. After signal sampling finishes, the common mode feedback circuit of the ramp generator is enabled and the charge is transferred and stored at the input of preamp by the crowbar signal. Once the common mode of the ramping signals settle after the kick back from crowbar action, a global gray counter will start to count and at the same time, the ramp generator starts to ramp. When the column comparator output change status, a pulse will be sent to the column SRAM to write the gray counter value into the respective SRAM unit.

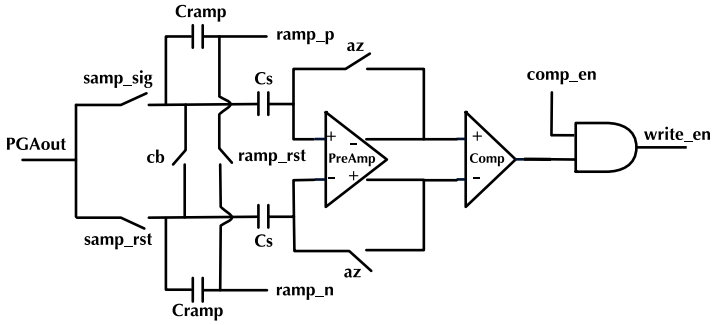

Figure 1. Column SS ADC diagram

II. Ramp Generator

One drawback of SS ADC is its slow conversion speed when bit resolution is high. In principle, SS ADC needs a conversion time of 2N-1 clock cycles, where N is the resolution. For example, to complete a 12-bit data conversion, it takes 4,095 clock cycles. Consequently, the row operation time must be longer than 4,095 clock cycles; therefore the frame rate will be low if the pixel array has many rows.

Since shot noise increases with increasing signal and dominates among various noise sources in the large input signal region, if we increase quantization step while keep quantization noise less than half of shot noise [1], the imaging quality won't be affected. This means that we can complete an effective higher-resolution conversion with less steps and hence the frame rate can be increased, which requires the ramping signals for the SS ADC to be accelerated.

Figure 2 shows the diagram of the accelerated continuous-time differential ramp generator. The accelerated ramp generator is used to increase the 12-bit ADC conversion rate. Differential design is adopted to improve power supply rejection (PSR). In order to obtain the binary increasing slope of the ramping signals, Iint is seeded by a 2-bit current DAC. Each DAC bit doubles the integrating current. The ADC conversion process can be started with ramp_off pulse first to guarantee the output of column comparator is in correct status. Then control signals ix1a, ix1b, ix2 and ix4 will turn on one by one until the ADC conversion cycle completes. A super current source generating the currents is designed to reduce mismatch, increase output impedance and eliminate glitches. In order to create a knee as ideal as possible when the slope is changed and to reduce the knee's sensitivity to PVT corners, a local feedback circuit is added around the current sources. The high gain OTA is a folded cascode amplifier and is powered with 3.3V supply, the common mode output is 1.65V, and the output swing of the differential ramping signals can reach 2.2V.

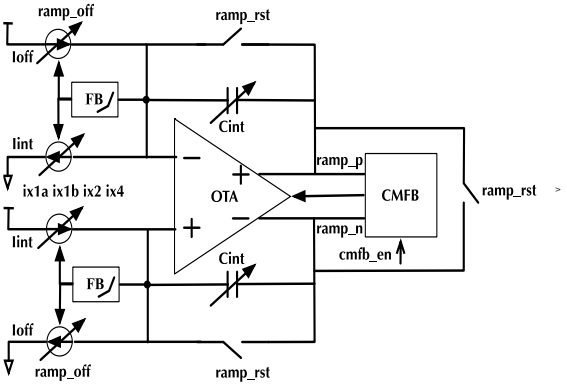

Figure 2. Ramp generator diagram

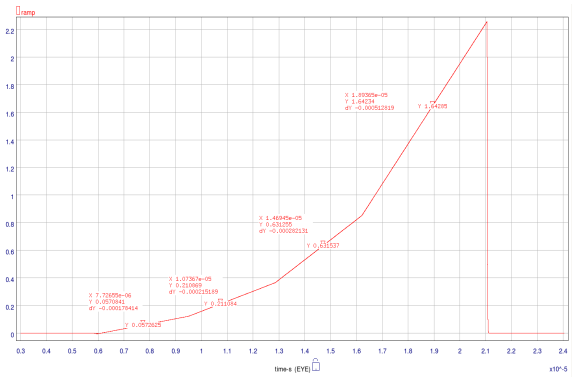

Figure 3. Transient noise simulation results

Because the integrator capacitor and loading capacitor of the ramp generator are big, the noise of the generated ramping signal is low by nature. Figure 3 shows the transient noise simulation results for 50 iterations. The peak-to-peak noise at the first section is 178uV, while this noise is increased to 512uV at the last section because more noise sources are active when more branches of current are turned on.

III. Super Current Source

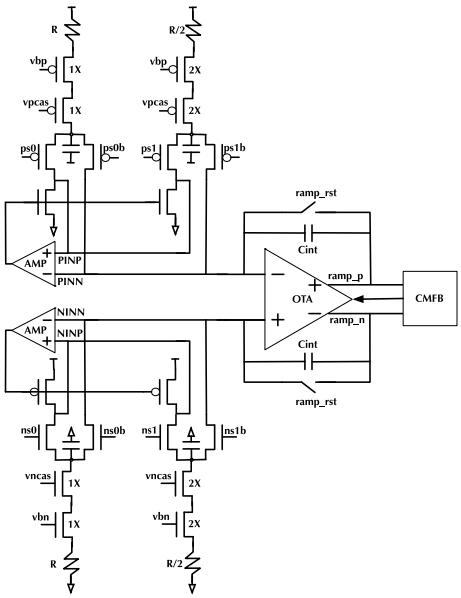

Figure 4. Super current source diagram

Figure 4 shows the implementation of the low mismatch, high output impedance and glitch free current source used to generate the ramping signals. The quality of the ramping signals is dominated by the performance of the current sources used to generate Iint and Ioff. In order to meet the 0.1% mismatch requirement between the slopes of the ramp signals across PVT corners, a cascode current source with source degeneration resistor is adopted in the design. The accelerated ramp signals have multi knees. A knee is created when we add one more branch of currents. Clock feed through, charge injection and other transient effects will deviate the knee from ideal position, especially when the circuit is operated under different PVT corners. In order to make the knee as ideal as possible, two strategies have been taken in the design. First, all the control signals' (ramp_off, ix1a, ix1b, ix2 and ix4) swing is limited and the switching slew rate is controlled to reduce clock feed through effect. Only a few hundred millivolt swing on the control signals is needed to completely switch the tail current of a differential pair (the two switches); Second, a local feedback circuit is used to reduce the performance sensitivity to PVT variations. This local feedback amplifier ensures NINN=NINP and PINP=PINN to enhance the matching of the current source. The current sources steer the current either to power/ground or to the integrating capacitor depends on the status of the control signals. The capacitors connected at the sources of the switches have two purposes, one is to filter out glitches when a control bit changes status, and two is to create a zero together with the on resistor of the switch to stabilize the feedback loop.

IV. Prototype Imager

Figure 5 shows the block diagram of the column readout architecture incorporated in the prototype imager. Top and bottom readout topology was used in the design. It consists of PGA,

sunspot correction, sample and hold capacitors, binning switches, SS ADC and SRAM in each column. A global ramp generator and gray counter provide ramp signal and counting bus for the SS ADC's. Once the comparator in the column flips, the current bus value will be captured into the dual bank SRAM for readout. A family of 5 image sensors with different pixel size, array size and clock speed have been fabricated in the TSMC 0.18um 3.3V/1.8V CMOS process using the same design architecture.

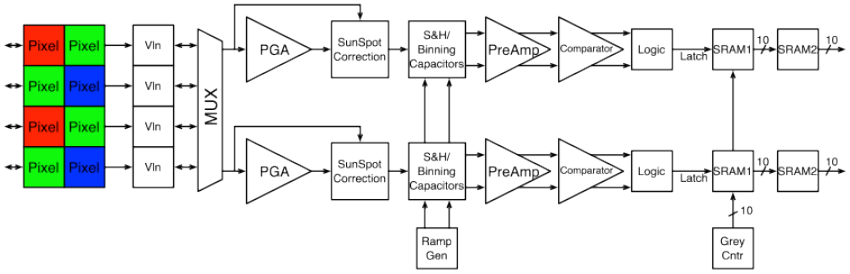

Figure 5. Column readout architecture

V. Conclusion

A prototype low noise, low power, column-parallel CMOS image sensor incorporating SS ADC was presented. The measured DNL performance is shown in figure 6. The glitches in the DNL curve correspond when the knee happens and it is an active area of work for future designs. The DNL was calculated to take into account the variation of LSB size along the ramping signals. Noise performance of the imager was carefully measured without any correction for different gain settings and the results are shown in table 1.

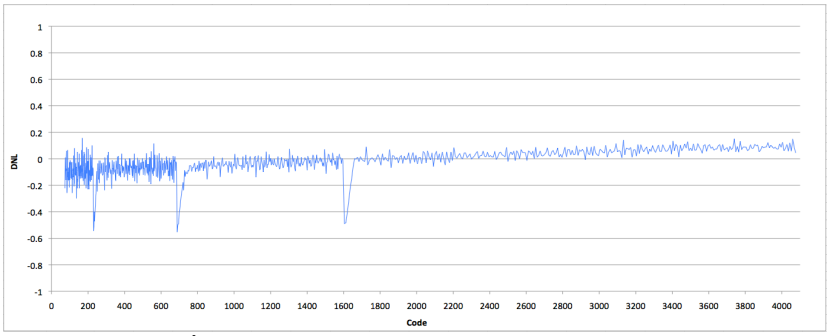

Figure 6. SS ADC DNL measurement

Table 1 Noise measurement results

	Gain			Unit
	1x	3x	24x	
Total Noise	532.12	192.03	143.92	µV
Readout Noise	497.86	171.37	107.94	µV
Row Noise	193.52	50.23	13.37	µV
Column FPN	156.9	42.12	33.88	µV

References:

[1] Toshinori Otaka, et al., "12-Bit Column-Parallel ADC with Accelerated Ramp", IISW, 2005.
[2] M.F.Snoeij, et al., "A Low-Power Column-Parallel 12-bit ADC for CMOS Imagers", IISW, 2005.
[3] Daniel Van Blerkom, Lin Ping Ang, "Column parallel readout with a differential sloped A/D converter", US Patent No.7.471.231.82, 2008.