A low power counting method in ramp ADCs used in CMOS Image sensors

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Abstract
We present a new counting method that can be used in a column-level ramp ADC. Comparing to the conventional ADC architecture, the proposed method can significantly reduce the power consumption by reducing the number of count with two clocks at different frequencies. The implementation of this method makes it possible to use such ADC structure in a large resolution sensor with relatively small digital power consumption.

1. Introduction

Column-level ADC has been widely used in modern CMOS image sensor design to achieve high data rate. For its simplicity, ramp or single-slope ADC architecture is one of the popular options in the column-level ADC design. Recent publication [1] had showed a column ADC designed in a very small pixel pitch, down to 5.5um in 180nm CIS technology. However, comparing to some other ADC structure, the conversion speed of ramp ADC is rather slow because of it in general requires at least 2^n count in a n-bit conversion.

Figure 1 shows a typical ADC architecture. A ramp signal is provided as the input of the column comparator, the output of the comparator is connected to a counter enable block which generates the counting cycles. Figure 2 shows an example ADC quantization algorithm that was used in [1]. Differently, as described in [3], the counters can also counting first downwards and then upwards.

In both options, the total number of clock counts directly relates to the difference between the reset level and signal level. However, whether or not changes the counting direction, to realize high conversion speed, it is essential the counting clock is running at very high frequencies, even up to a few GHz [2,3]. In this case, it consumes quite a lot of current in the digital counters and introduces a lot of spikes in the substrate, resulting in supply noises. In addition, the total ADC power consumption, the supply and ground level vary when the scene is complete dark or bright because the count may counts for different length. This is a particularly a big problem in a very high resolution sensor implementing column ramp ADC since the ADC power consumption is dominant the total chip power. In extreme cases, the high power current flows from the ADC supply may pull down the supply level significantly due to parasitic resistance of the chip and package, thus causes the chip to fail.

This paper presents a new digital counting method which can dramatically reduce the number

of counts in the column and therefore the power consumption by using two clocks with different frequencies.

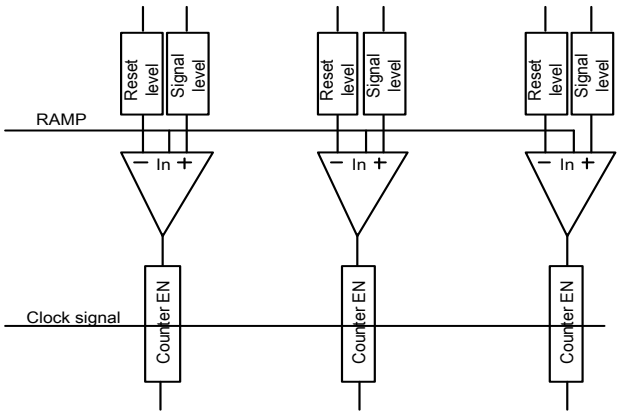

Figure 1 Typical ramp ADC architecture

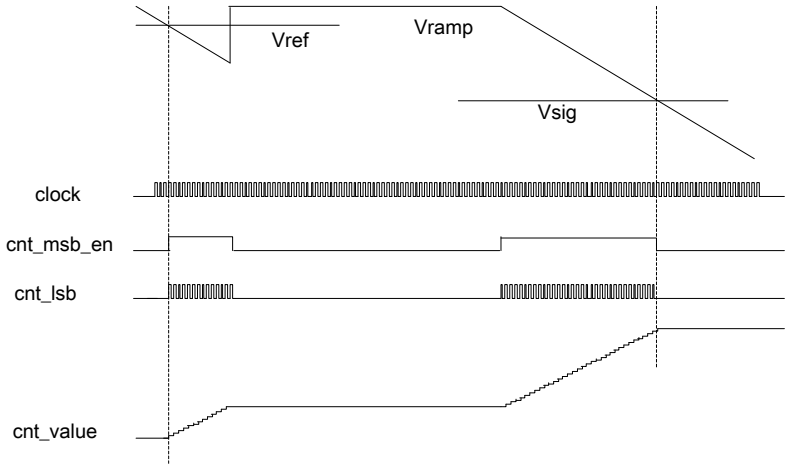

Figure 2 ADC quantization process in [1]

2. Implementation

The proposed counting algorithm is illustrated Figure 3, the ramp converts pixel reset voltage starts from t0 and end at t3, the ramp converting pixel signal voltage starts from t5 and end at t9. The comparator flips at t1 when converting the reset voltage and flips at t7 when converting the signal voltage. The frequency of clock high is 2^{n_lsb} times the frequency of clock low, with n_lsb the number of bits we want in the LSB counter. t2 and t8 are the first falling edge after the comparator flip, t4 and t9 are the first falling edge after the end of the ramp converting the reset voltage and the beginning of the ramp converting the signal voltage respectively. The MSB counter starts up counting from t2 and end at t4, then it starts up counting again from t6 and end at t8. The LSB counter starts up counting from t1 and end at t2, then it starts down counting from t7 and end at t8.

With this algorithm, the maximum number of counts in each column is reduced to $2^{n\_lsb}+2^{n\_msb}$

instead of $2^{(n\_lsb+n\_msb)}$ as in the conventional method. Given an example, in a 12bit conversion, the maximum number of count is 4096, while in this method; it reduces to $2^6+2^6=128$ counts. This dramatically reduces the total current consumption in the digital counters. Besides, as the total number of counts is not proportional to the signal level in each column, the digital power supply level and ground level variation at dark level and saturation level is the same in principle.

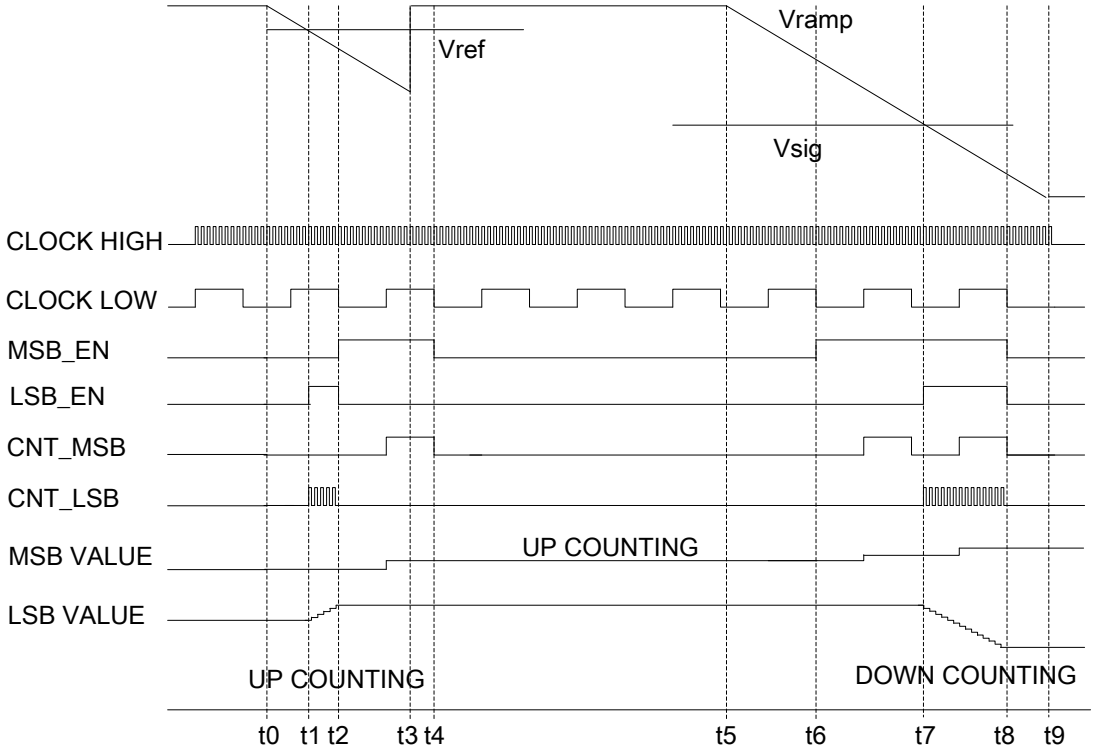

Figure 3 Proposed counting algorithm with two different clocks

In order to verify this algorithm, a test chip was made to implement an 8-bit ramp ADC, with 4 bit MSB counting with low clock frequency and 4 bit LSB counting with high clock frequency. For simplicity, a voltage level Vpix is input to the ADC instead of real pixel output voltage. As shown in Figure 4 , Vpix and ramp voltage are input to a comparator, the comparator output is input to some logic circuits to generate the counting cycles CNT_MSB and CNT_LSB which are then input to the MSB and LSB counters. As the LSB counter needs to count in both directions, one addition bit is used for overflow protection. In the end of the conversion, the final data on the two counters are processed to form an 8- bit digital data word and serially read out. The test chip is still under test at the moment.

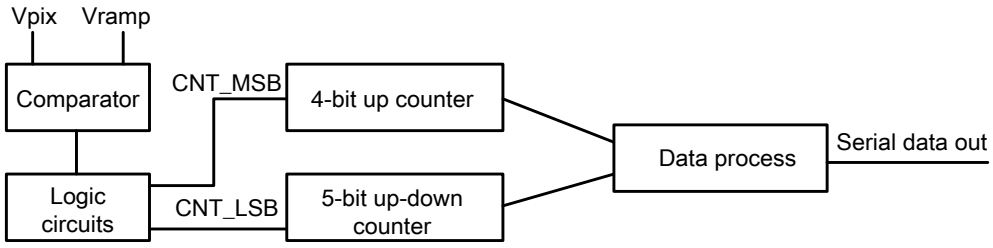

Figure 4 Block diagram of the test chip

3. Conclusion

A new counting algorithm is presented to reduce the digital power consumption in ramp ADCs through two clocks with different frequencies. This algorithm generates two counter cycles that are used for MSB counting and LSB counting respectively. MSB counter cycle is generated based on the low frequency clock and the comparator output, while LSB counter cycle is generated based on the high frequency clock, the comparator output and the edge of the low frequency clock. Power consumption is reduced through the dramatically reduction of the number of clock counts in the column.

4. Reference

[1]: X. Wang, et al, “A 2.2M CMOS Image Sensor for High Speed Machine Vision Applications”, proc. SPIE vol. , 7536, January 2010.

[2]: J.Bogaerts, et al., “ High speed 36Gbps 12Mpixel global shutter CMOS image sensor with CDS”, IISW 2011.

[3]: T. Toyama et al., “A 17.7Mpixel 120frames/s CMOS Image Sensor with 34Gb/s Readout”, ISSCC2011, paper 23.11.