A Passive Integrator to Achieve Low Power, Low Noise Signal Amplification

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Abstract **This paper presents an integrator architecture to achieve signal amplification and noise averaging without the use of an active element. By using a diode that can fully deplete within an operating voltage, a signal voltage is sequentially sampled in the charge domain and transferred on an integration capacitor. Such structure can achieve lower power, lower noise and potentially less silicon area compared to traditional integration amplifiers. A test chip (T.C.) has been designed using the passive integrator as a column gain block in an image sensor. The T.C. has been manufactured in a standard 0.18 image sensor process. The silicon results confirm the theoretical analysis and provide interesting insights for future applications in image sensors and micro-electronics in general.**

1. Introduction

Integration amplifiers are widely used in microelectronic applications. In this paper, the focus is on it's use in image sensors. It can be used as a major block for an ADC or as a stand-alone analog block to gain up signals and average out the noise.

Such integrators need at least one active element to achieve the required feedback to drive the integration capacitor's virtual ground so that charge integration can occur.

However, in most cases, a differential amplifier is used to achieve linear integration. In that case, amplifiers with multiple active devices (mos transistors) are required. This increases the total noise and power consumption. In an image sensor such gain structure can be required in each column, increasing the total power consumption of the image sensor significantly.

An example of a simple traditional integration amplifier structure is shown in figure 1. The timing to operate it is presented in figure 2.

The passive integrator architecture described in this paper is a completely different approach to achieve signal integration enabling lower noise, lower power consumption and possibly less silicon area compared to the traditional integrating amplifier architectures.

2. A passive integrator: principle of operation

Figure 3 presents a circuit diagram of the passive integrator in it's most basic form. A possible timing to operate it is shown in figure 4. The principle of operation described below can be understood from the timing and the fluid analogy diagram in figure 5.

Prior to sampling, the diode is pre-charged to a low voltage, the diode is than sufficiently full of electrons (see figure 5: 1/4: A). At approximately the same time, the integration capacitor Cint is reset to a high voltage (Vdd_reset). This introduces ktc noise on Cint in the voltage domain according to Eq. [1].

$$Vn_{reset} = \sqrt{\frac{K \cdot T}{C\,\mathrm{int}}} \qquad [1]$$

Thereafter, the input voltage is sampled on the diode, draining away some of the charge until the voltage of the diode equals the applied input voltage. As a result, a certain charge residue remains in the diode according to Eq. [2] (see figure 5: 2/5: B).

$$Qdiode_{sample} = Cdiode \cdot (VPIN - Vin) \qquad [2]$$

With VPIN: depletion voltage of the diode in [V]

This sampling phase introduces ktc noise on the diode in the voltage domain according to Eq. [3].

$$Vn_{sample} = \sqrt{\frac{K \cdot T}{Cdiode}} \qquad [3]$$

After the sampling phase, the integration phase starts: the remaining charge in the diode is transferred to the integration capacitor Cint (which was reset during or prior the first sampling phase). Due to the fact that the diode is able to fully deplete of charge (this is an absolute critical factor), all charge is transferred, achieving a nearly zero noise integration (3/6: C). This sequence can occur for a number of N cycles. Eq. [4] then expresses the output voltage Vout after N integration cycles.

$$Vout(N) = Vdd\_reset - N \cdot \frac{Cdiode}{C\,\mathrm{int}} \cdot (VPIN - Vin) \qquad [4]$$

The output noise after N integration cycles is expressed in Eq. [5].

$$Vn\_out(N) = \sqrt{\left(\frac{K \cdot T}{C\,\mathrm{int}}\right) + N \cdot \left(\frac{K \cdot T}{Cdiode}\right)} \qquad [5]$$

Figure 6 presents the theoretical output noise comparison between the passive integrator and an active integrator with similar capacitor sizes in function of the number of integration cycles.

It must be noted that in practical circumstances, the input voltage Vin better doesn't get too close to the diode's depletion voltage VPIN. Because, in that case, the diode capacitance will start to reduce which results in a non linear output response (see the diode representation in Figure 9 and the silicon results described in the next chapter).

3. Silicon results confirm theoretical analysis

Figure 7 and 8 present the output voltage in function of # integration steps N and the input referred noise respectively. As can be seen, for an increase in N, the input voltage needs to be closer to VPIN to enable a useful output voltage (for input voltages that are too low in absolute value, the output will be clipped for larger N). Whereas for large input voltages (close to VPIN), a non linear response is observed. Due to the latter, a certain minimum range for the input voltage Vin from VPIN is required to stay in the linear amplification range.

This introduces an offset which is integrated, limiting the number of effective integration cycles. This offset integration can be significantly reduced by using a compensation circuit that consists of a sequential level shift on the integration capacitor after each integration cycle. In Figure 9, a possible circuit to do this is shown.

In this circuit, the back plate of the integration capacitor Cint is connected to a circuit that can apply a step by step incremental voltage after each integration cycle. As such, the integrated offset can be partially compensated which will increase the amount of effective integration cycles. Figure 10 shows the theoretical improvement of such approach.

4. Summary

A method and architecture is proposed to enable signal integration without the use of an active element. Silicon results confirm the theoretical analysis and provide insights in the possibilities for such architecture in future applications in image sensors and potentially to other applications in micro-electronics as well

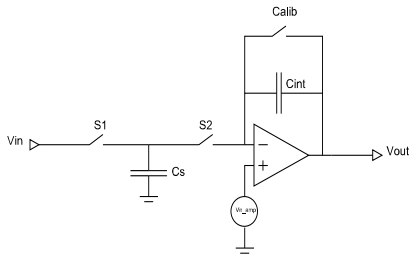

Figure 1: A basic traditional integration amplifier.

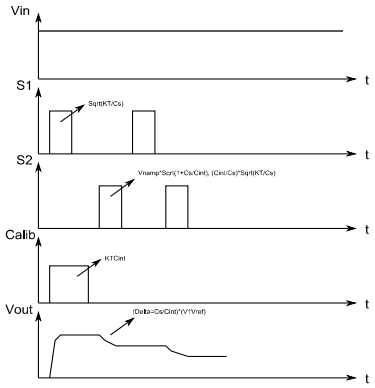

Figure 2: A possible timing to operate a traditional integration amplifier (shown in figure 1).

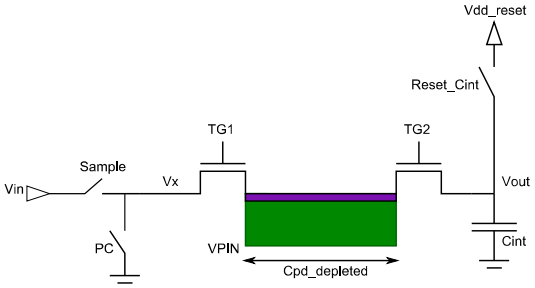

Figure 3: A passive integrator in it's most basic form.

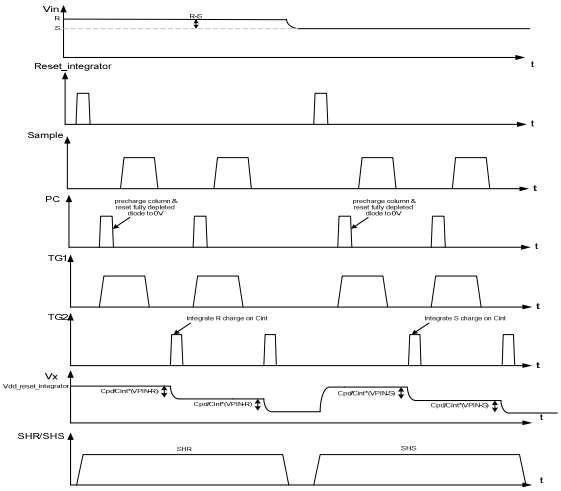

Figure 4: Timing to operate the passive integrator of figure 3.

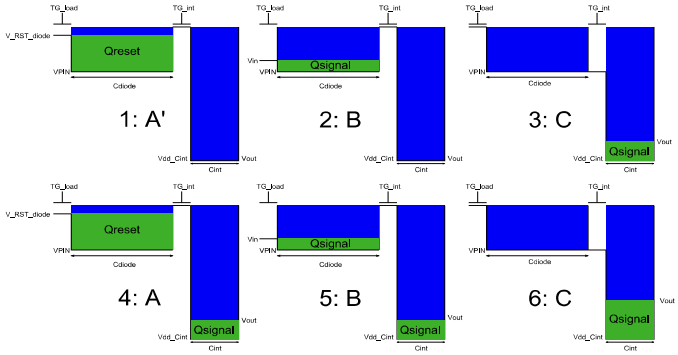

Figure 5: Fluid analogy

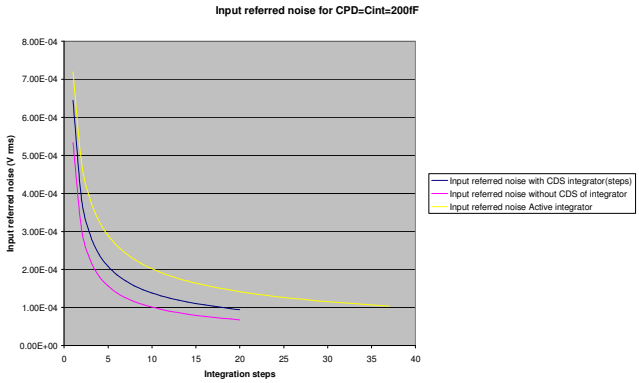

Figure 6: Noise performance comparison in function of # integration steps (model).

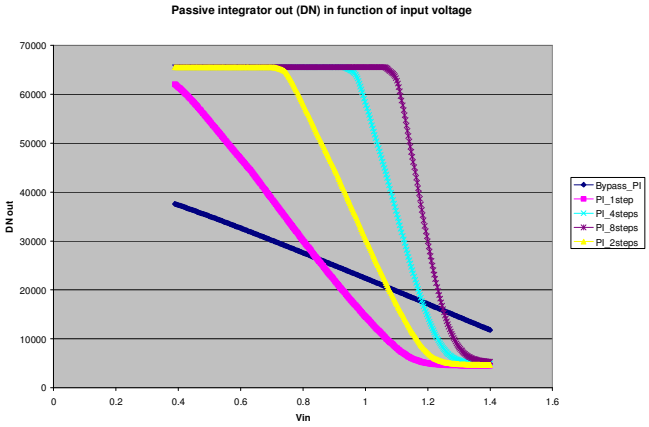

Figure 7: Measured Input-Output relationship for different # integration steps.

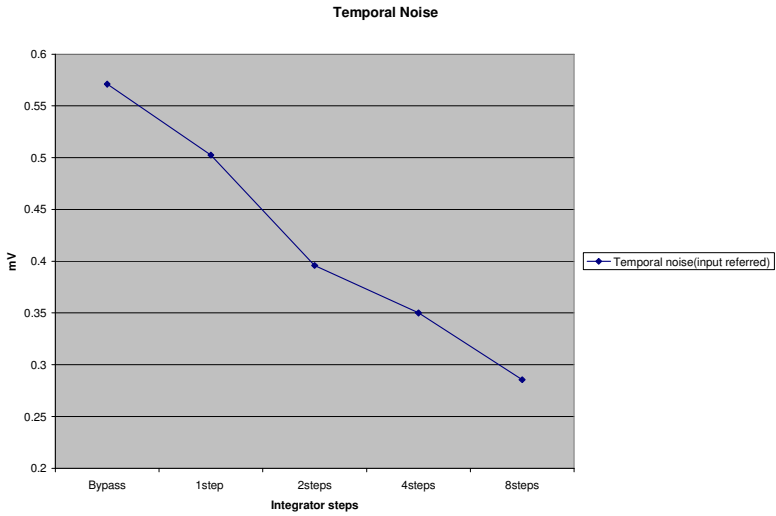

Figure 8: Measured input referred noise.

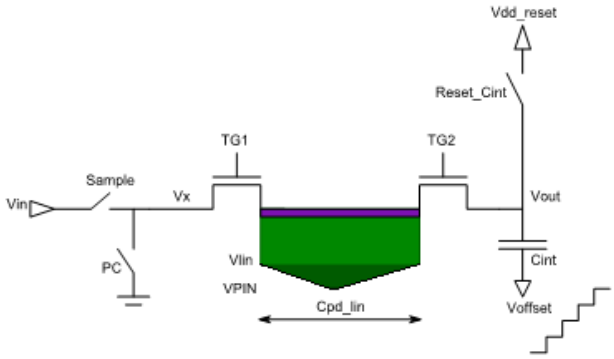

Figure 9: Passive integrator with (partial) offset cancellation and (more) realistic diode representation.

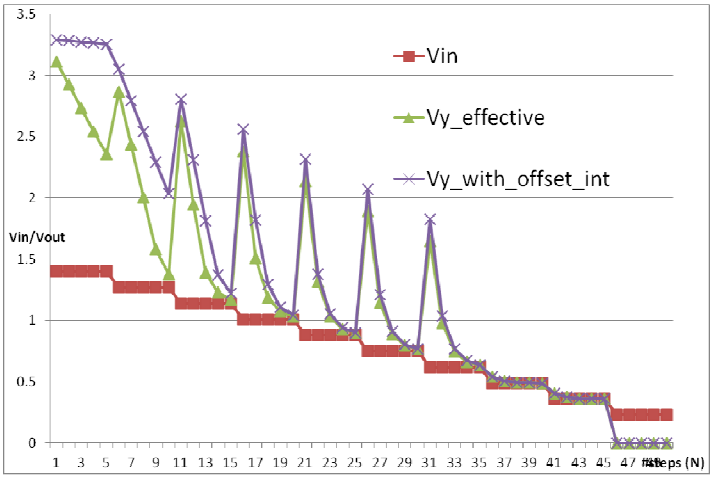

Figure 10: Passive integrator input-output with and without offset cancellation (Model).