New monolithic CMOS sensors on a fully isolated substrate

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Introduction

As predicated by the title of reference 1, today all commercial digital cameras use almost exclusively CMOS sensors. The success of monolithic CMOS image sensors as a viable lower cost replacement for CCDs in consumer products triggered a widespread interest in the potential use of these devices for scientific applications [1,2,4], and some experiments have already started using them [3]. The main advantage of this approach is the integration of the sensor on the same substrate as the readout electronics which results in higher yield, reliability and lower cost.

Most current CMOS devices use a structure similar to the one shown in figure 1a. Since the nwell is used as a collecting electrode, PMOS transistors cannot be used around the sensing area. This restricts the front-end circuit to few NMOS transistors laid out in the pwell, severely limiting the readout performance and resulting in a less than 100% fill factor. Designs that could achieve 100% fill factor have been proposed in [6] and [7]. In [6] this has been achieved by using a specially developed 0.18µ process where the nwell, where PMOS transistors reside, is isolated from the substrate by a deep p-well unique to this technology. In reference [7] a 0.35µ high-voltage CMOS process, along with special circuit techniques, has been proposed.

It is worth mentioning that charge collection in these devices except in [7] is primarily a diffusion process. As a result, monolithic particle detectors are generally inferior to their hybrid counterparts when it comes to charge collection efficiency, timing performance, and tolerance to radiation damage. In hybrid systems the sensor and readout electronics are separately produced and optimized components, interconnected by packaging.

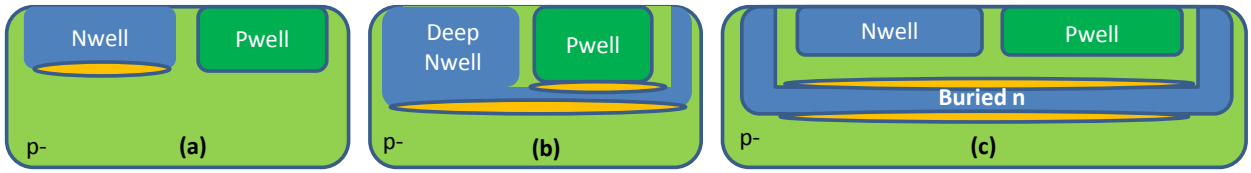

Figure 1 Very simplified illustration of: (a): standard CMOS (substrate could be epitaxial). (b): deep nwell structure. (c): CMOS with buried n isolation. Orange ovals denote the main p-n junctions.

When the deep-nwell structure became available in commercial CMOS processes, it was proposed that they could be used to improve these sensors [5,8]. As shown in figure 1b, some of the NMOS transistors could be integrated above the sensing junction. Also, one could bias the substrate to negative voltages (if all NMOS transistors in the chip are integrated in deep n-wells as in [8]). Biasing the substrate could result in improving the detection efficiency [8, 11]. Timing improvement is also expected because the fraction of charge collected by drift would increase. However, the deep nwell sensor does not result naturally in a 100% fill factor. The usage of all devices would require special process steps and/or circuit techniques as in [6, 7]. Using deep-nwell devices could also result in lower circuit density.

Production of the "ideal" monolithic radiation detector, where the sensing function places no restrictions on the electronic circuits and the fill factor is 100%, has so far proven elusive. One promising approach has been to use Silicon on Insulator (SOI) technology with a modified process to use the normally inactive substrate as sensor [10]. SOI, however, is not a mainstream technology for consumer electronics, and special processing is required to produce SOI sensors.

In this paper we describe a new monolithic sensor on a fully isolated substrate in a 0.13μ CMOS commercial process where low voltage, high performance transistors can be used over the sensing area without significant restrictions or special circuit techniques.

Monolithic sensors on a fully isolated substrate:

Recently a new isolation process has been introduced in a popular commercial technology (0.13u CMOS). A cartoon of this process is shown in figure 1c. The nwell, where the PMOSs are laid out and the pwell, where the NMOSs are laid out, are implanted above a third buried nwell (dubbed here BN). Because the devices are laid out using the regular design rules, modest area penalty is incurred. The substrate can be completely isolated from the wells where the active devices are located. One can use the substrate-BN junction as a sensing element. Since both transistor types are isolated, they can be used for the readout function and 100% fill factor can be achieved. The substrate can be biased to increase detection efficiency and improve timing performance without affecting the readout devices. This type of monolithic sensors has not been proposed before, to our knowledge, and could potentially prove to be a major step towards ubiquitous low cost, low mass monolithic particle detectors and x-ray detectors. Another way to use this structure is to bias BN and use the local p substrate inside of it as the collecting electrode, connected through a thin p+ implant at the surface. This structure could prove very suitable for applications that require thin collection layer like electron microscopy, since the local p substrate could then be fully depleted (as opposed to traditional active pixels) resulting in enhanced spatial resolution. But in this case 100% fill factor would not be possible.

Performance competitive with hybrid systems could be achieved if the resistivity of the substrate were comparable to that of detector grade silicon. Using high resistivity substrates for CMOS chips is the subject of current R&D at CERN [9].

Monolithic sensors using the BN process are a natural candidate for a high performance monolithic detector system, as all the devices are truly isolated from the substrate.

Prototype chip

To investigate this principle we have designed an 18X64 prototype chip. The main active area is composed of 16X64 "large" pixels (22μ by 225 μ) and each pixel contains about 715 devices. These pixels design targets High Energy Physics applications. Because of the need to store hit data, such as timestamp and analog information, until needed by the readout system, quite complex in-pixel functionality is required [12]. The leftmost and rightmost columns consist of 1X64 small reference pixels (10μ X10μ). No transistors were laid out over these sensors. They are read-out by the same front-end circuit as the larger pixels. These small pixels are closer to typical MAPS designs. In a real chip, rudimentary front-end circuit would be implemented. The area would accommodate about 8 to 10 P-type and N-type transistors. The front-end circuit diagram is shown in figure 2. The cell consists of a charge sensitive preamplifier with programmable gain (feedback capacitance) DC coupled to a comparator. The comparator threshold is set by a chip-wide bias added to a local tuning bias to reduce threshold dispersion. The tuning current is set by a 5-bit DAC. The cell also contains configuration, control and readout blocs. These were designed not only to readout the chip but also to investigate possible cross-talk issues as all circuits are directly on top of the corresponding sensor.

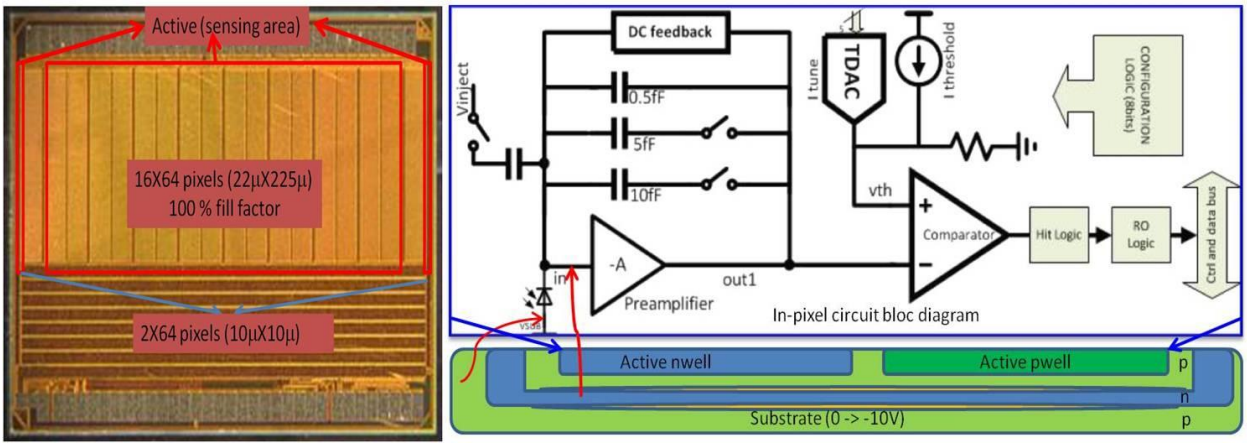

Figure 2 Prototype chip photo and the in-pixel circuit diagram illustrating the main sensor connections. (Not to scale).

Preliminary results

The chip was found to function as expected. At nominal bias condition (15µA/pixel at 1.5V supply voltage and -10V substrate bias) the achieved input referred noise is about 200e-,rms for the large pixels and about 25e-,rms for the small ones. Threshold dispersion without tuning has been measured to be about 530 and 120e-,rms for large and small pixels respectively. Individual pixel tuning should reduce the mismatch to less than 25e- . The chip was also tested with substrate bias (VSUB) ranging from 0 to -10V. Figure 3a shows the ENC as function of VSUB. Figure 3b shows the effect of VSUB on the preamplifier response. Both results indicate a non negligible reduction in input capacitance as one decreases the substrate bias from 0 to -10.

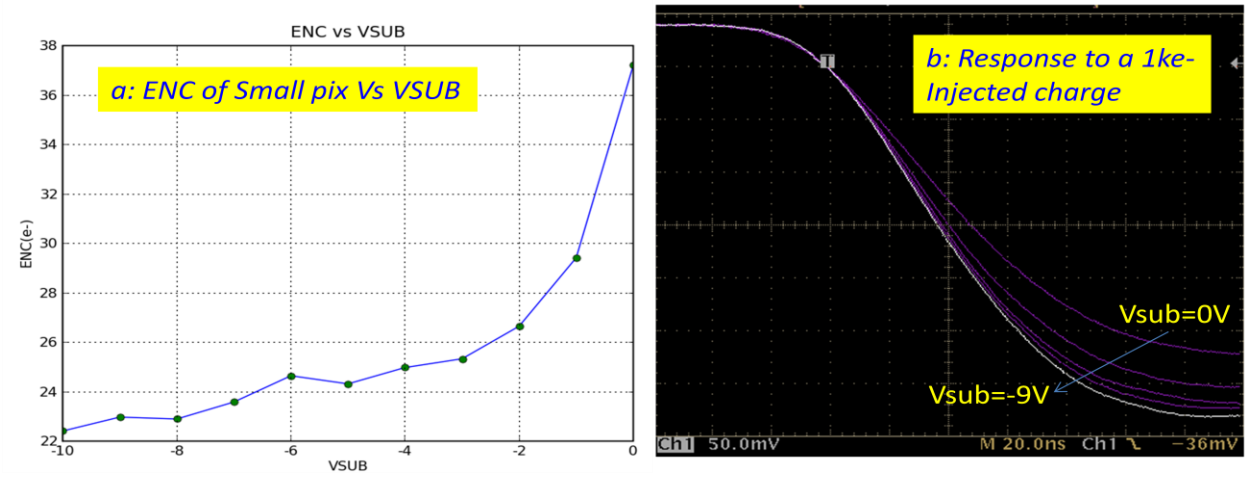

Figure 3 a: ENC vs Vsub. b: Preamp response to a 1ke- injected charge as function of Vsub

The chip was exposed to both monoenergetic electrons (form a Sr90 source) and photons (from an Fe55 source) and all pixels were found to be responsive. A typical small pixel Fe55 source spectrum is shown in figure 4. In the case of Fe55, the effects of biasing the substrate are visible. At -10V the two main characteristics peaks of this source are clearly visible and separated. At 0V, not only the amplitude, at the preamp output, of the main peak has decreased but we see also that the 2 peaks have merged as a result of increased noise. The bias condition may also have altered the way charge is collected. For the Sr90 case even though the difference is not as pronounced, we see the broadening of the spectrum at 0V as result of increased noise.

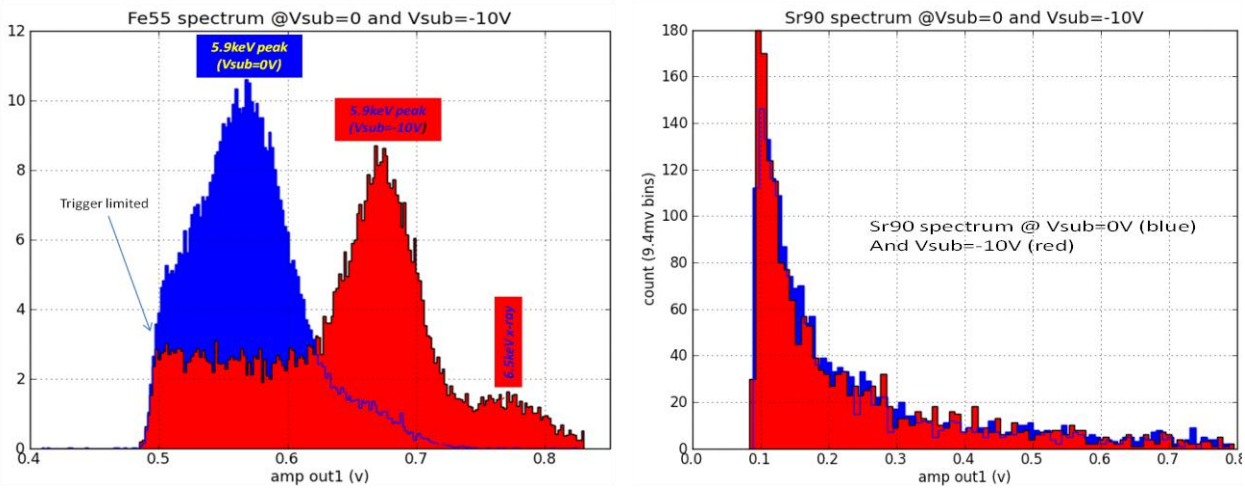

Figure 4 Spectrum of Fe55 (X-ray) and Sr90 (e-), obtained from a 10μX10μ single pixel.

Conclusion

We have exploited a new CMOS substrate isolation implant to implement a monolithic radiation detector. Because the substrate is completely junction-isolated from the active wells, it can be biased at larger negative voltages than would be possible in a standard process. This not only permits true 100% fill factor but also improves the sensor performance. Preliminary results from our prototype are encouraging and complete evaluation and analysis of the sensors is ongoing.

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