

New model of Dark fixed pattern noise generation in CMOS imager pixel with negative transfer-gate bias operation

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ABSTRACT

In this paper, we analyze the mechanism of Dark fixed pattern noise generation in CMOS imager pixel with negative transfer-gate bias operation by both measurement data and simulation. Our results show the noise generation is caused by recombination between electrons from photo-diode and holes trapped at interface state when negative bias is applied to transfer transistor.

I. INTRODUCTION

Negative gate bias on transfer gate has been widely used in CMOS imagers to reduce dark current because the accumulation of holes at the interface between gate insulator and Si substrate reduces the generation rate of dark current [1-3]. Recently, we suggested Negative Bias Temperature (NBT) stress for transfer gate causes Dark Fixed-Pattern-Noise (FPN) [4]. Fig.1 shows an example of dark FPN, which was observed in a test sensor. Some circles show black defect pixels. We reported this degradation has negative bias and temperature dependency. Dark FPN is caused by dark electron loss at transfer gate channel. This phenomenon is important issue for the aging effect of CMOS image sensor.

This paper reports the Dark FPN generation mechanism based on experimental results of increase interface state density at gate insulator and Si substrate, and on TCAD simulation with re-combination model between electrons and holes at the interface.

II. EXPERIMENT

Fig.2 shows the proposed test pattern of simple pixel array with a gated-diode structure, which was used to evaluate the change of interface state density before and after negative bias stress. The fixed bias is applied to the floating diffusion (FD) and SUB is connected to ground. Bias from -1.5 to 1V is applied to the transfer gate (TG). The current of SUB in weak inversion around gate bias of -0.5V depends on the interface state density, because gated-diode current in weak inversion relies on the Shockley-Read-Hall (SHR) theory of the recombination-generation process [5]. Fig.3 shows the I-V characteristics after 48 hours under stress of (a)-1V, (b)-2V. This result shows the increase of state density due to strong negative bias stress and indicates that the increase of interface state causes Dark FPN.

In NMOS case, the transistor characteristics are same even under the condition of state density increase which is different from PMOS case, as shown in Fig.4. That is the reason why NBTI degradation of NMOS has not been focused until now.

III. DIFFERENCE OF NMOS AND PMOS

Fig.5 shows the differences of effect by NBT Stress in NMOS and PMOS, respectively. The interface state density near valence band increases with negative bias stress and holes are trapped at the trap sites. In PMOS, of which operation bias is negative, the trapped holes remain in gate insulator and at the interface between gate insulator and Si

substrate. However, in NMOS, because operation bias is positive, the trapped holes recombine electron of conduction band. So, the decreases of trapped holes cause the recovery of NBT Stress degradation.

IV. SIMULATION OF RECOMBINATION MODEL

In order to confirm the recombination phenomena, the dynamic behaviour of trapping were obtained using Transient Noise Simulation (TNS) [6]. In this simulation, the τ_c and τ_e of each trap are calculated by means of the WKB theory for tunnelling probability and SRH statistics for transit probability (Fig.6). Fig.7 shows the simulation conditions. Gate length of 0.25 μ m, T_{ox} of 7nm and the interface state density of $1e17cm^{-3}$ and $1e18cm^{-3}$ are used. Fig.8 shows the simulation results. These results clearly represent the electrons of conduction band recombine the trapped holes. Fig.9 shows the effect of hole traps at operation bias in NMOS and PMOS. In NMOS, finally, almost all of the trapped holes recombine the electrons of conduction band. This result obviously shows the reason why the transistor characteristics are same even under the condition of state density increase. Fig. 10 shows the IV-t sampling characteristics of the degraded NMOS by applying NBT Stress. We measure I_d at $V_g = 3V$, $V_d = 3V$, $V_{sub} = 0V$ after V_g stressed at $V = -4V$ for 30 min to inject holes into trap sites. I_d decreases with time due to increase of V_{th} . This result indicates the decrease trapped hole by recombination and the simulation result supports the measurement data. Fig. 11 shows our model of Dark FPN generation. Negative bias operation for transfer gate causes an increase of the state density and the electrons from photodiode recombine with the trapped holes.

V. CONCLUSION

We analyze the mechanism of Dark fixed pattern noise generation in CMOS imager and propose new model based on re-combination between the electrons from photodiode and the holes trapped during NBT Stress. We show the model can explain Dark fixed pattern noise observation.

Reference

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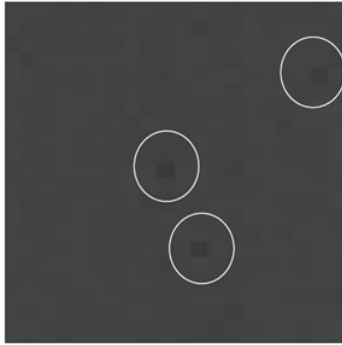


Fig.1 Enlarged dark image taken after NBT stress. Circles show black defect pixels [4].

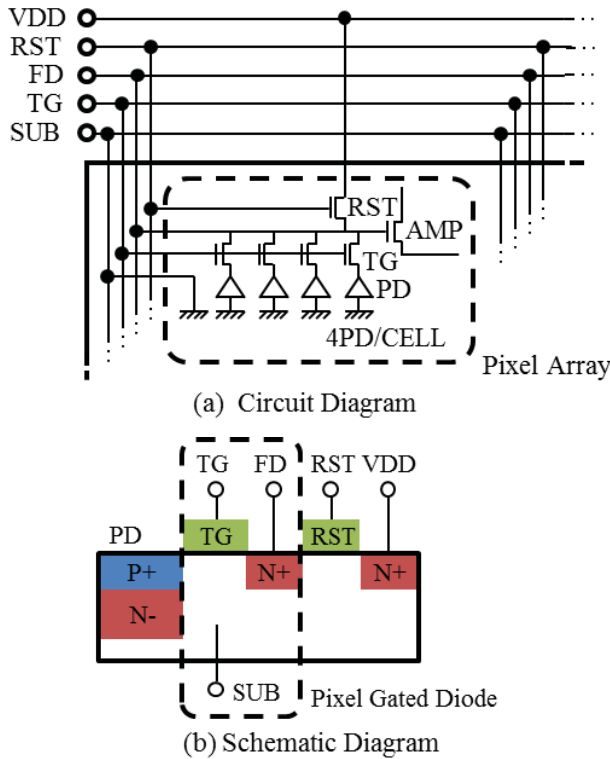


Fig.2 Proposed test structure for evaluation of the change of the interface state density before and after negative bias stress.

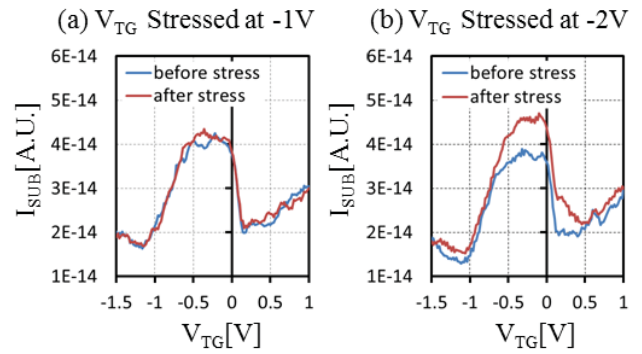


Fig.3 Evolution of Gated Diode (DCIV) Peak for V_{TG} Stressed at 70C. Comparison of (a) and (b) means the increase of interface trap density has bias dependence.

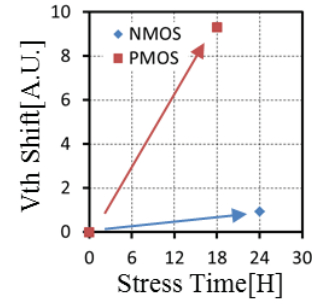


Fig.4 NBTI degradation for V_G Stressed at $-4V@70C$. PMOS has strong correlation between the interface trap density and V_{th} shift but NMOS has small.

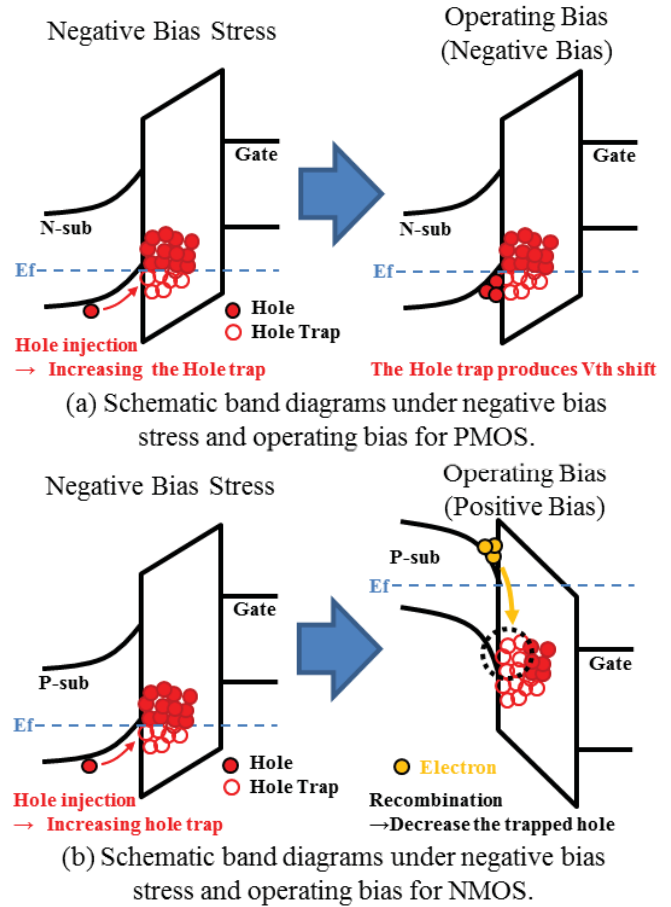
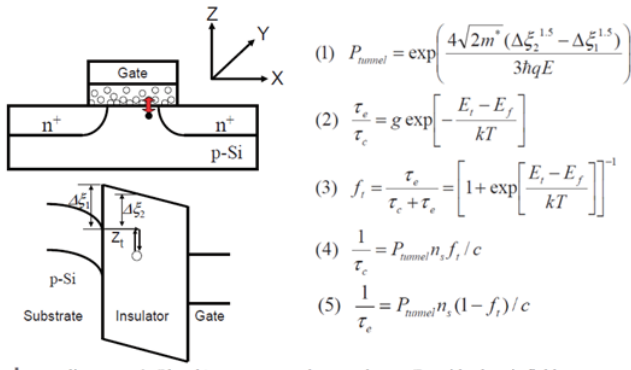


Fig.5 The trapped holes remain under PMOS operation. On the other hand, the holes recombine the electron in conduction band under NMOS operation.



m^* : tunneling mass, h : Planck's constant, q : electron charge, E : oxide electric field, g : degeneracy factor; g is assumed to 1, T : temperature, E_t : energy level of trap, E_f : quasi Fermi energy, n_s : carrier density, c : capture coefficient; c is assumed to $10^{-8} \text{ cm}^3/\text{sec}$

Fig.6 The τ_c and τ_e used in recombination model are calculated by means of the WKB theory for tunneling probability and SRH statistics for transit probability. The formula to calculate in our simulation are shown in this figure. [6].

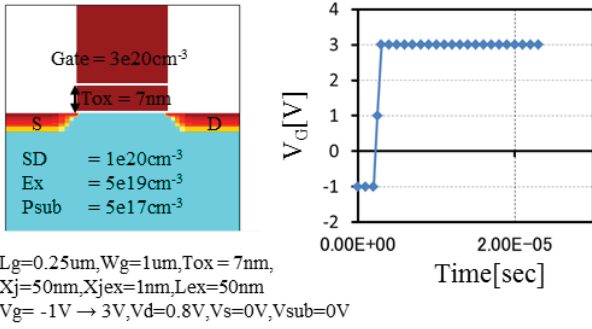


Fig.7 TCAD Simulation Condition. “Low” bias pulse was applied for 3us, before applying “High” bias pulse for 20us.

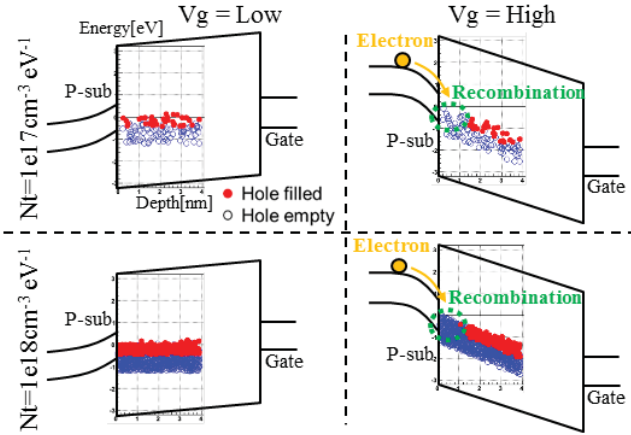


Fig.8 Transient Noise Simulation (TNS) represents the electron in conduction band recombine the trapped holes by a negative pre-pulse. The increase of trap density causes the increase of the electron-hole recombination.

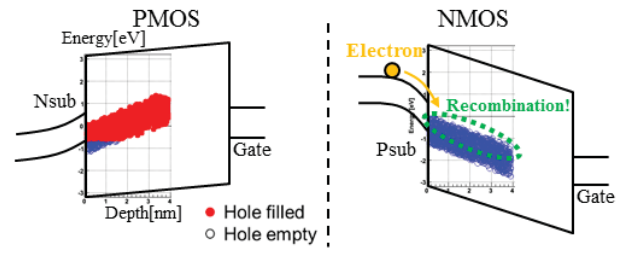
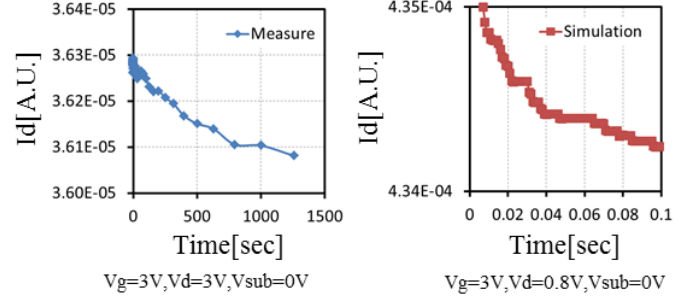
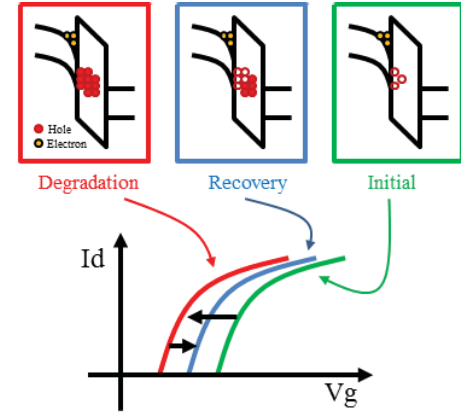


Fig.9 The increase of trap density causes the strong degradation in PMOS but the small degradation in NMOS, because the electrons in conduction band recombine the trapped holes. After applying a positive bias for a long time, in case of NMOS, almost all of the trapped holes disappears.



(a) I_d - t sampling characteristics of NMOS under fixed V_d , V_s , V_g and V_b after applied negative pre-pulse. The blue one is a measurement data of NMOS stressed at NBT and the red one is a simulation data using the electron-hole recombination model.



(b) The V_{th} shift of NBT stressed NMOS during I_d sampling measurement.

Fig.10 The decrease of I_d is caused by the V_{th} shift, which indicates the recombination between electrons and trapped holes occurs.

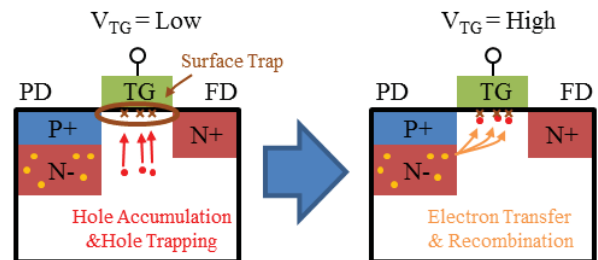


Fig.11 Dark FPN Generation Model. The generated electrons in photodiode decrease due to the recombination with trapped holes. This electron decrease causes Dark FPN.

