Novel Device with Ultra Low Noise for Smaller CMOS Image Sensor Pixel

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Abstract

Minimize pixel noise is a very important topic to enhance signal to noise (S/N) ratio of CMOS image sensor (CIS), especially for smaller pixel. In this work, we have developed a novel device with self-aligned junction isolation (SAJI) and operated by buried channel. With optimized process and junction profile, this novel device can demonstrate better narrow width effect (NWE), lower flicker (1/f) noise and larger photodiode (PD) sensing area than STI device by surface channel.

Introduction

As pixel size is further scaled to achieve higher resolution CIS, how to maintain the required S/N ratio is getting more challenged. Backside illumination (BSI) sensor technology had been the mainstream to boost the optical performance [1, 2]. Another important factor to enhance S/N ratio is to reduce noise level. However, an undesirable 1/f noise could dominate the noise and degrade CIS quality as pixel transistor (Tr) shrunk with pixel size scaling [3]. According to previous investigation [4], Tr gate oxide traps and shallow trench isolation (STI) are two major sources which would induce 1/f noise.

In this study, we analyzed the junction profile of the buried channel (BC) Tr then found out the optimized device to prevent from gate oxide traps. On the other hand, adopting junction isolation (JI) to replace traditional STI can reduce dark leakage and 1/f noise as well but narrow width effect (NWE) is the challenge of Tr with JI [4]. We analyzed and optimized the junction profile to significantly improve NWE and 1/f noise at the same time. Then we created a new device with self-aligned junction isolation (SAJI) to further shrink Tr dimension and reduce NWE. Combining with optimized SAJI and BC, this novel device successfully demonstrated ultra low 1/f noise and larger PD sensing area which can be employed in smaller CIS pixel.

Device Design

Fig. 1(a) shows the schematic diagram of a traditional STI device operated by surface channel (SC). STI process damage and gate oxide traps are also illustrated in the figure. In order to reduce the impact from STI sidewall damage, STI surrounded by a field implant had been usually adopted to reduce dark current and noise. But a required spacing between PD and STI is still necessary for lower dark current and white pixel. And even with STI field implant, the damage can't be 100% isolated.

For gate oxide trap reduction, optimizing gate oxide quality is necessary but it's difficult to achieve trap-free. Thinner gate oxide thickness and larger Tr width and length could reduce 1/f noise, but lower gate oxide integrity and be unfavorable to pixel shrinkage are side effects respectively. Changing from surface channel to buried channel device is another effective choice to get away from gate oxide traps as shown in Fig. 1(b). BC device evaluation will be discussed in next section.

Using an anti-type implant as junction isolation instead of STI is shown in Fig. 1(c). However, NWE and poly end-cap control are major challenges to employ JI for CIS [4]. Higher isolation implant (ISO-Imp) dosage can provide better device isolation for sure but it will consume PD sensing area as well. ISO-Imp and relative device junction adjustment are critical to deliver a good Tr for smaller CIS pixel.

A self-aligned junction isolation (SAJI) device was created as shown in Fig. 1(d). With this novel structure, we don't need to worry about poly end-cap control anymore and PD sensing area can be further enlarged

due to ISO-Imp region shrinkage. Combining with SAJI and BC, device should be able to deliver extremely low noise and dark leakage.

Results and Discussions

Junction optimization is an important work to deliver a good BC device. Deeper channel could provide lower 1/f noise due to much away from gate oxide traps. But Tr off-current (I_{off}) would be increased and Tr threshold voltage (V_t) would be decreased, as shown in Fig. 2. Theoretically, Tr with P+ Poly could provide truly buried channel because of energy bank gap difference, compared to using N+ poly. However, V_t of P+ poly Tr is higher than that of N+ poly under same Tr I_{off}. Fig. 3 compares N+ and P+ doped poly BC device with same channel implant profile. Nevertheless, higher V_t will reduce CIS operation range thus lead to smaller dynamic range. Consequently, define the desired V_t and I_{off} target for a BC device is the 1st decision that we need to make. Thus we can focus on channel junction optimization by N+ or P+ doped poly.

Following, we start to evaluate the NWE and 1/f noise of the device. Fig. 4 demonstrates the normalized Tr NWE of STI, junction isolation (JI) and self-aligned junction isolation (SAJI) devices operated by surface channel (SC). The X-axis shows Tr delta channel width and Y-axis shows Tr delta V_t. The NWE could be significantly improved when we modified the device junction profile from A to B to C. The NWE of profile C is already better than that of device with STI. On the other hand, with same profile B, SAJI device can further improve NWE than JI device. And we assume that combining SAJI with best profile C, the NWE should be further minimized.

We also evaluated the NWE for BC devices and the results are shown in Fig. 5. They indicate the same trend that both modifying device junction profile and adopting SAJI structure can indeed improve NWE. And SAJI device demonstrates better performance than JI device.

Finally, we analyzed the 1/f noise performance and found something interesting. Fig. 6 compares the Tr drain current noise of SC to BC devices and STI to JI devices. Changing from SC to BC indeed shows a little improvement. But using JI instead of STI can dramatically reduce the 1/f noise around 1-order. This result demonstrates that damage from STI process would impact 1/f noise more than traps from gate oxide. Therefore, employ junction isolation instead of STI could effectively eliminate 1/f noise.

We also evaluated the 1/f noise of different junction profiles (A, B, C) and JI, SAJI devices, as shown in Fig. 7 & Fig. 8. The result shows that 1/f noise keeps the same level for these varieties.

Conclusion

In this work, we studied the device performance of buried channel transistor with different junction profiles to reduce 1/f noise from gate oxide traps. And we improved the transistor narrow width effect by optimizing the junction profile of junction isolation devices. We also designed a novel device with self-aligned junction isolation to further minimize NWE and transistor dimension which benefits smaller pixels. As a result, NWE can be better than that of traditional STI device by optimizing process condition. Furthermore, we demonstrated that STI process damage degrades the 1/f noise more than gate oxide traps. And combining with optimized junction isolation and buried channel devices, 1/f noise has been significantly reduced.

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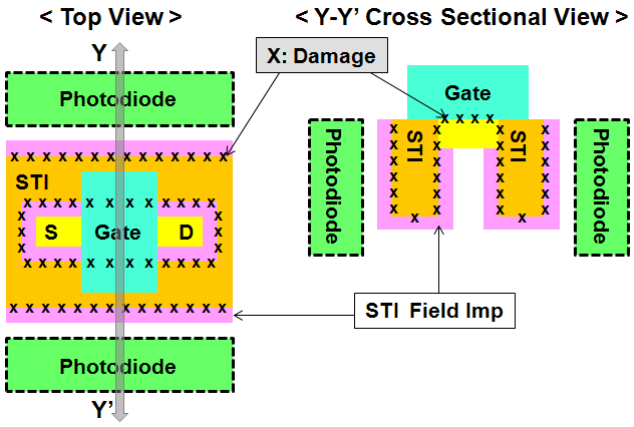

Fig. 1(a): Schematic diagrams of STI device with surface channel.

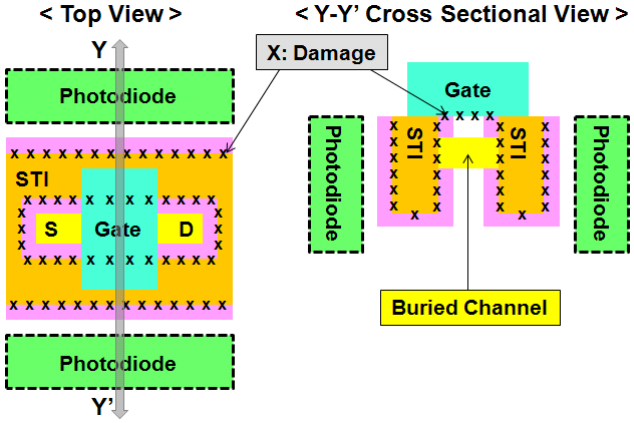

Fig. 1(b): Schematic diagrams of STI device with buried channel.

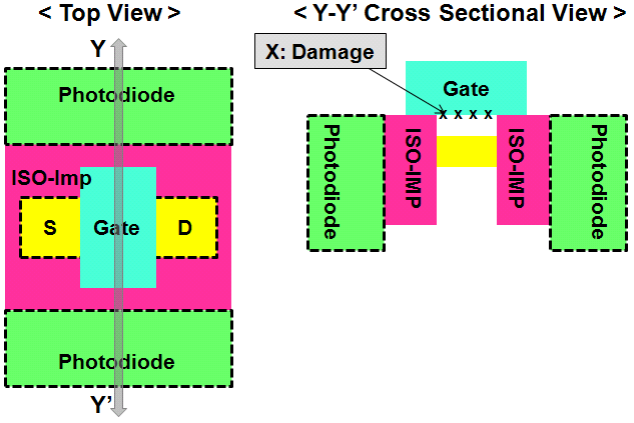

Fig. 1(c): Schematic diagrams of JI device with buried channel.

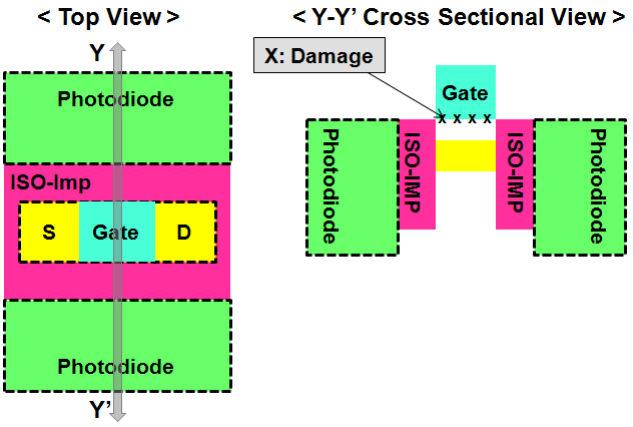

Fig. 1(d): Schematic diagrams of SAJI device with buried channel.

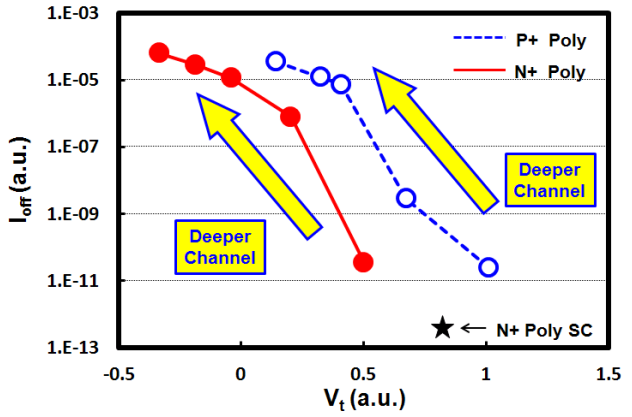

Fig. 2: Tr I_{off} versus V_t of P+ and N+ poly BC device when channel depth varies.

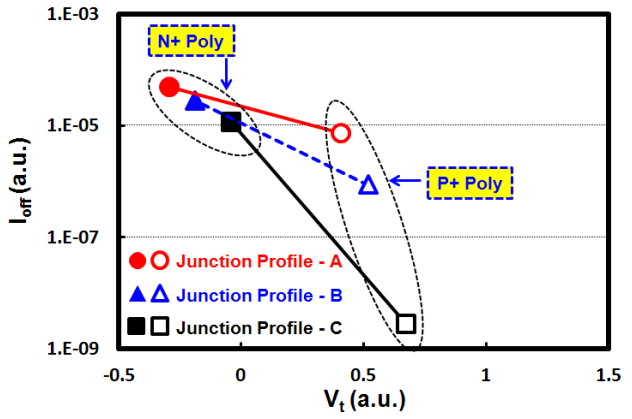

Fig. 3: Tr I_{off} versus V_t of P+ and N+ poly BC device with same junction profile.

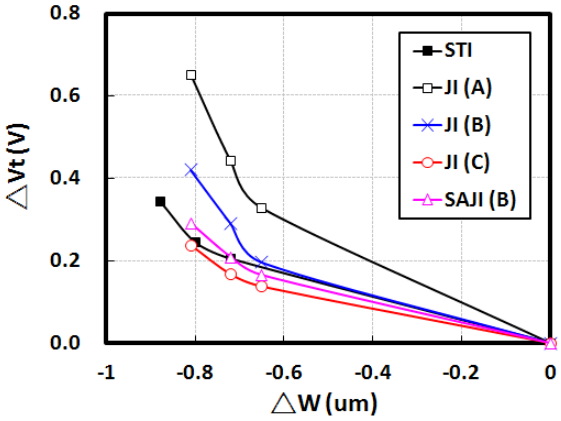

Fig. 4: Normalized NWE of STI, JI, SAJI SC devices with various junction profiles (A, B, C).

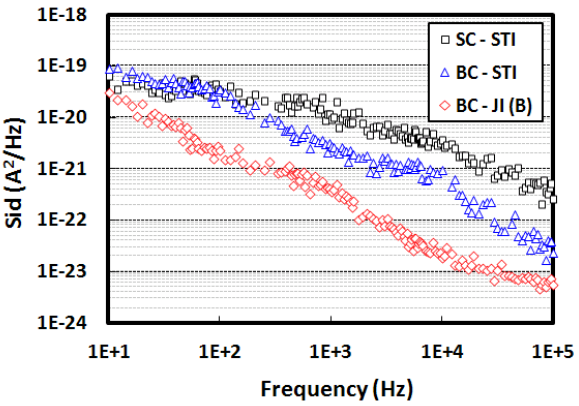

Fig. 6: Tr drain current noise spectra comparison for SC, BC & JI devices.

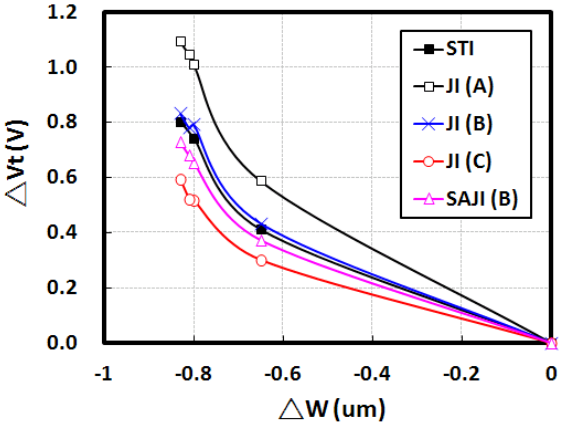

Fig. 5: Normalized NWE of STI, JI, SAJI BC devices with various junction profiles (A, B, C).

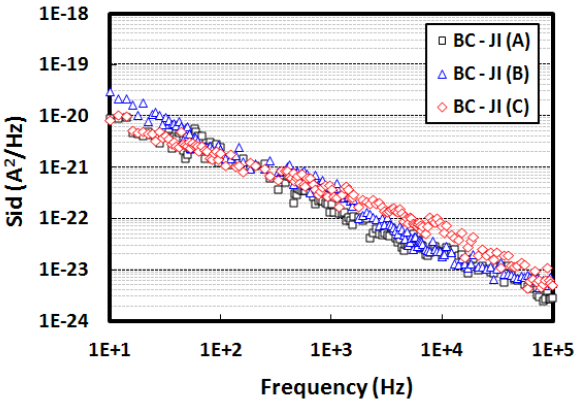

Fig. 7: Tr drain current noise spectra of BC JI devices with various junction profiles (A, B, C).

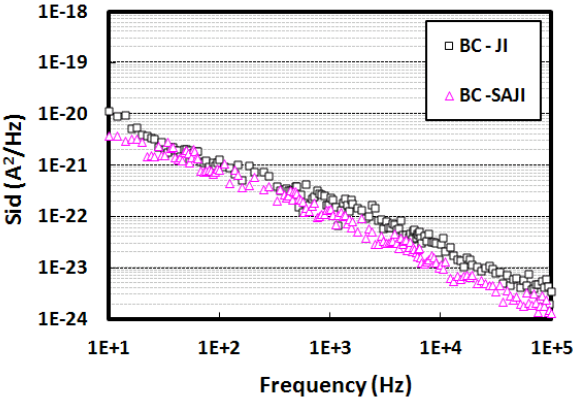

Fig. 8: Tr drain current noise spectra of BC JI & SAJI devices with same junction profile.