MEM-FLIM, a CCD imager for Fluorescence Lifetime Imaging Microscopy

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Abstract

MEM-FLIM, a CCD imager for use in advanced Fluorescence Lifetime Imaging Microscopy (FLIM) applications is presented. A demodulation frequency of 80MHz is achieved with 4V clock swing with an optimized pixel design. An optional electron-multiplication CCD register using a single-poly electrode structure is included in the imager.

Introduction

A FLIM system requires an imager that can 'gate' the incoming light synchronized with a pulsed light source in the frequency range of 20MHz to 80MHz, with a typical resolution of 500x500 pixels, an image area of ~1cmx1cm, and a readout speed of 30 fps. The required sensitivity range is from 450 to 700nm. We chose for a CCD-based approach [1] because of the high achievable fill factor with pixel sizes around 25x25μm^2, achievable resolution of up to 512x512 pixels and the feasibility of high fringing fields to achieve the high demodulation speed, but with the known challenge of high power consumption. For the typical low light levels in FLIM, an optional electron-multiplication readout (EM-CCD) was developed. Examples of current state- of-the-art FLIM imagers based on CMOS or SPADs technologies can be found in [2], [3], [4]. The development was done in two phases: (1) Development of two prototypes CCD imagers with different pixel concepts; and in parallel the development of an EM-CCD design and technology; (2) Development of the final MEM-FLIM imager incorporating the results of the first phase.

Development of two FLIM-CCD prototypes

As prototypes, two small CCD imagers were developed and combined in a multi-project-wafer approach. The first prototype, Fig. 1, uses a 'horizontal toggling' pixel concept: two toggle gates, to the left and right of the photo-gate, are pulsed in anti-phase and the generated electrons are collected via the integrating gates in the interline registers. The second prototype, Fig. 2, uses a 'vertical toggling' concept: two toggle gates are positioned above and below the photo-gate and the generated electrons are collected under two collection gates; followed by a 3-phase readout. Due to chip-size constraints for the multi-project wafer, this prototype has only a full-frame structure (i.e. not a FT-CCD structure). Both sensors have a light-shield (not shown) on the whole pixel except on the photo-gate. The CCDs were made in the 'standard' CCD technology of Teledyne DALSA [5],[6]. The details are captured in Table 1. The motivation for investigating the 'horizontal toggling' concept was that the illumination does not need to be stopped during readout (integrating gates are set to low voltage, and electronic shutter condition is present under photo-gate also set to low voltage), and that the high-frequency toggling gates are separate from the 'interline gates' which makes the camera electronics optimization easier. Figs. 3 shows the phase response at 20MHz for both types. Details of the evaluation of the vertical toggling CCD w.r.t. actual lifetime measurements can be found in [7]. As a result of the critical settings of the interline register and the low fill factor in the horizontal toggling prototypes, the vertical toggling concept was chosen for the final implementation.

Development of EM-CCD structure

An EM-CCD with 1072 stages was introduced into an existing 1kx1k FT-CCD imager with 12μm pixel pitch, see Fig. 4. To minimize the degradation of the EM-CCD [8], a new technology was developed consisting of a single-poly design for the EM-CCD gates with oxide-only (i.e. no nitride) dielectric. The spacing between the EM-CCD gates of 0.20μm is reliably achieved with 0.50μm litho capability. A SEM photograph of two details of the structure is shown in Fig. 5. The image area uses the conventional two thin layers of 'membrane' poly-silicon with optically optimized oxide-nitride gate dielectric. The concept of the EM register operation is shown in Fig. 6. DC voltages are applied to gates DC1 and DC2. The generated electrons are immediately removed from DC2 to D1', resulting in a constant electrical field – and gain – under the transition from DC1 to DC2. The voltage difference between DC1 and DC2 determines the EM gain. The results of electron-multiplication measurements for two samples are shown in Fig. 7. The gain linearity is good over the full range, the saturation is occurring at the output stage only, not in the EM register, Fig.8. Reproduced images are shown in Fig.9. Preliminary lifetime experiments showed no EM-CCD degradation.

Development of the final MEM-FLIM CCD imager

The final imager has an FT-CCD architecture 512x512 'FLIM-pixels' of 24x24μm^2 and a storage area 1024(V)x512(H) cells of 12(V)x24(H)μm^2. This results in the largest possible chip size without stitching, with an image diagonal of 17mm matching well with existing microscopy optics. Readout is either through a conventional CCD readout register or through an EM-CCD register like in Fig.5. The target spec (and the obtained results) are

summarized in Table 4. The challenges in the development were the fill factor, the fringing fields in the CCD pixel during toggling, the on-chip power consumption of the CCD gates during toggling, and the interconnect to the gates. To limit the capacitance per pin, the image section was split into four vertical sections with separate gate connections for the high-frequency gates. All HF interconnects, on the chip and in the package, were made as identical as possible to achieve identical performance of all four image sections when demodulating.

To maximize the fill factor, the photo-gate needs to be as large as possible. However, a long photo-gate will result in a low fringing field even at high voltage swings of the neighboring toggle gates. This challenge was solved by splitting the photo-gate into three parts: a central part, not clocked, and two 'side-wings' clocked at reduced voltage swing, Fig. 10. For a symmetrical interconnect scheme with a high fill factor, a third metal layer was introduced to connect the 'wings'. The first metal (Wm) is used to connect to low-frequency electrodes. Fig. 11 shows the simulated electrical field in transport direction under the full length of the photo-gate, for a single photo-gate with toggle gates with a 8V clock swing, and for a toggle gate with two 'wings', with 2V clock swing, and 4V clock swing on the toggle gates. The significantly reduced voltage swing results in a power consumption reduction by a factor 3 with an increase of the minimal electrical field of a factor 8, from 100 to 800V/cm.

Evaluation Results

All measurements were done with 2V clock swing on the photo-gate wings and 4V clock swing on the toggle gates, all with 50% duty cycle. Fig. 12 shows the collected signal under the opposite integrating gates at 20MHz toggling frequency using a red pulsed laser with 33% duty cycle, as a function of phase shift between illumination and toggle gates. The demodulation efficiency is defined here as (max-min)/max. Fig. 13 shows the demodulation efficiencies obtained as a function of frequency. The illumination duty cycle was 33%. The efficiency is almost constant up to 60MHz and then starts to degrade, but it should be noted that part of the degradation is also due to the decreased modulation depth of the available laser. Demodulation efficiencies larger than 60% are considered useful for practical FLIM applications. The difference in demodulation efficiency per image section, at 20MHz, is <1.5 % without any special camera tuning, but it increases at higher frequencies.

The measured capacitances of the photo-gate wings and toggle gates are 1.7nF and 2.3nF per image section. The temperature of the sensor (in an un-cooled ceramic PGA package) increased by 20^{o}C only at 80MHz toggling, showing acceptable on-chip power consumption. Fig. 15 shows an assembled device.

Summary and Conclusions

We presented a FLIM imager with 512x512 pixels of 24x24μm^2 with a 50% fill factor and capable of operating at 80MHz demodulation frequency. An optional EM-CCD readout using a single-poly electrode structure is included.

References

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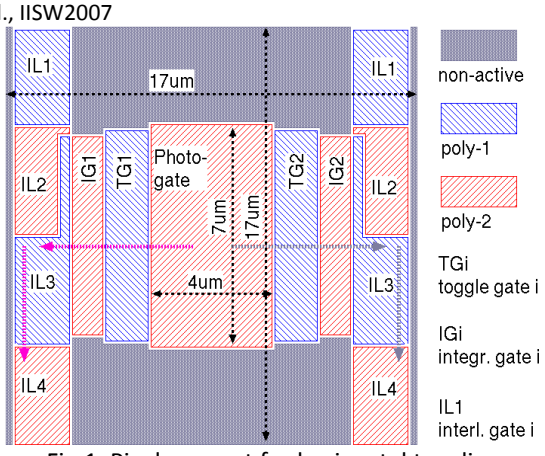

Fig.1. Pixel concept for horizontal toggling

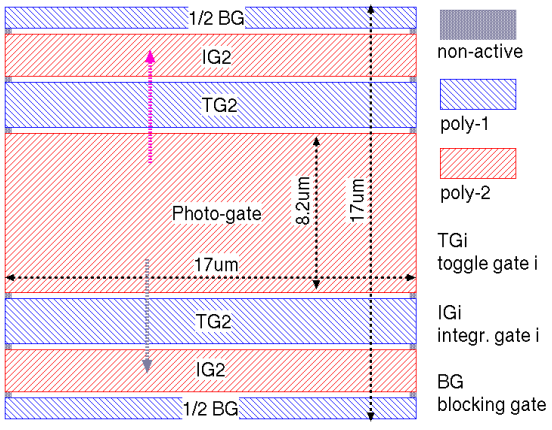

Fig.2. Pixel concept for vertical toggling

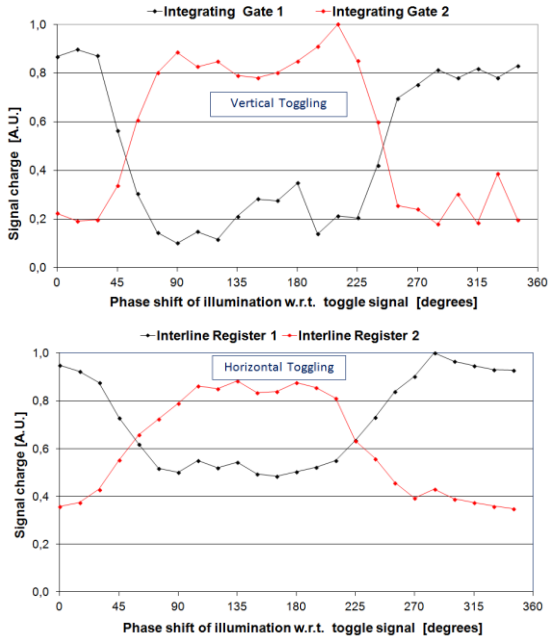

Fig.3. Collected signal under opposite integrating gates/interline registers as a function of phase shift of illumination (duty cycle 25%) for vertical (top) and horizontal toggling prototype (bottom). The high offset in the horizontal toggling prototype is due to direct collection in the register (light-shield too narrow).

	H toggle	V toggle
Pixel size (μm x μm)	17 x 17	17 x 17
Number of gates per pixel	9	6
No. of clocked phases during integration	6	5
Fill factor [%]	10%	40%
Number of poly's	2	2
Number of metals	2	2
PhG voltage (V)	6.4	5
TG voltage swing (V)	0-12	0-5
IG voltage during toggling (V)	10.2	8
BG voltage during toggling (V)	5.7	0

Table 1. Overview of MEMFLIM prototype imagers

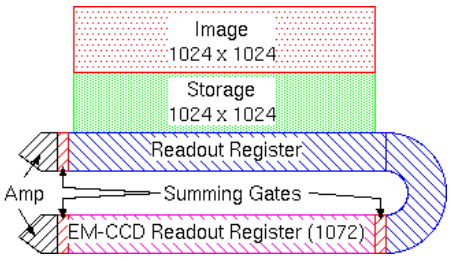

Fig.4. EM-CCD register integrated in 1kx1k FT-CCD

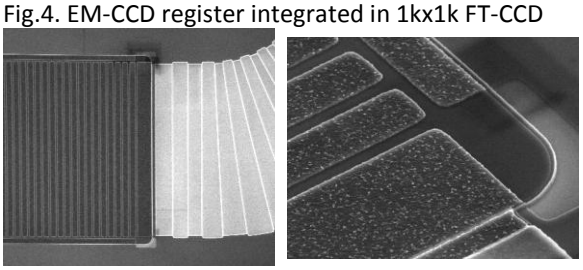

Fig.5. SEM photos of details of EM-CCD register

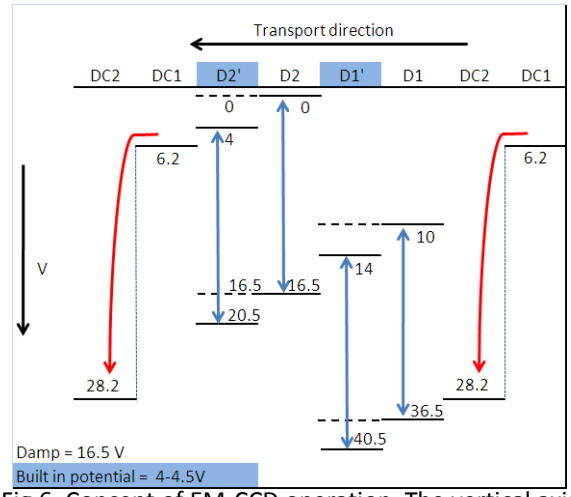

Fig.6. Concept of EM-CCD operation. The vertical axis shows the applied gate potentials.

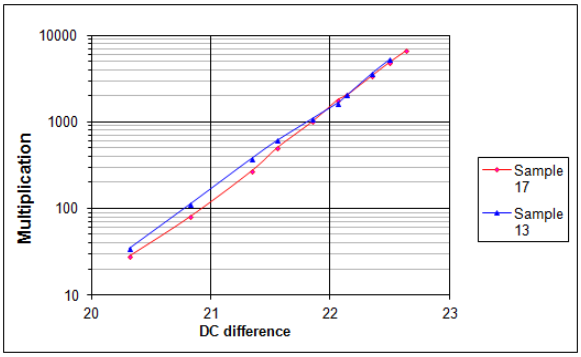

Fig.7. EM gain over 1074 stages as function of bias between DC1 & DC2 gates; 25MHz EM transport frequency, 25°C

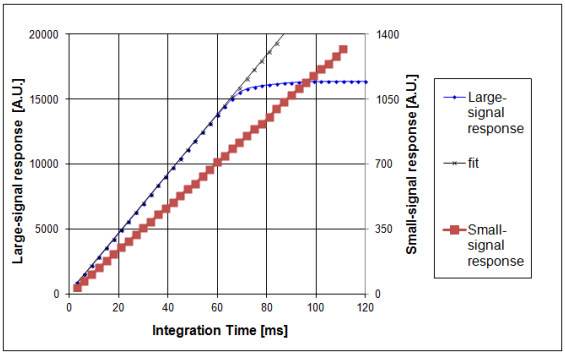

Fig.8. Linearity of multiplication, small and large signals

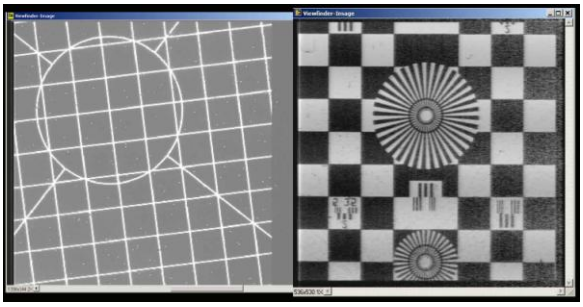

Fig.9. Left: Full-resolution image through EM-CCD without gain; Right: 2x2 binned image through EM-CCD register, gain ~500, 30fps. Both images at 25MHz register frequency.

Readout speed	25MHz
Amplifier sensitivity	17.5µV/e^-
Amplifier noise (25MHz, after CDS)	26 e^-
EM-CCD gain stages	1072
EM-CCD gain over all stages	1 to 5000 x
Linearity EM over 1074 stages	Better than 97%

Table 2. Summary of EM-CCD imager performance

Parameter		Target	Achieved
Toggling frequency (MHz)		20 to 80	20 to 80
Fill factor (%)		50	50
Number of phases per pixel		8	8
Number of HF phases per pixel		4	4
Clock swing PG 'wings' (V)		2	2
Clock swing TG's (V)		4	4
Capacitance of HF phases (per phase, for all 4 sections) (nF)	PhG	6.4	9.2
	TG	6.4	6.8
Max. frame rate at full res. (fps)		30	30
Max. frame rate 2 x 1 binned (fps)		50	50
EM-CCD gain		1 to 5000	t.b.d.
Max. EM-CCD frequency (MHz)		25	t.b.d.

Table 3. Target and achieved performance spec of final MEM-FLIM imager

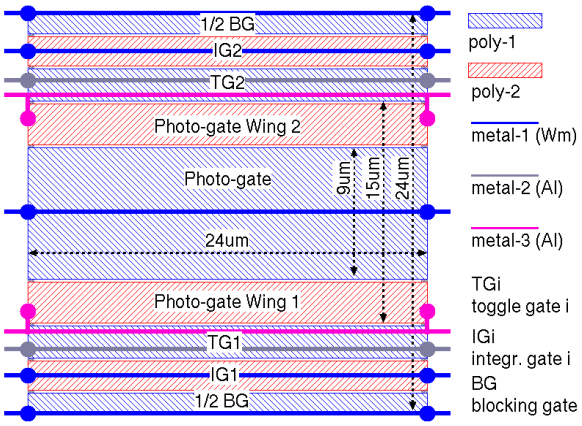

Fig.10.Pixel electrode and interconnect structure of final imager

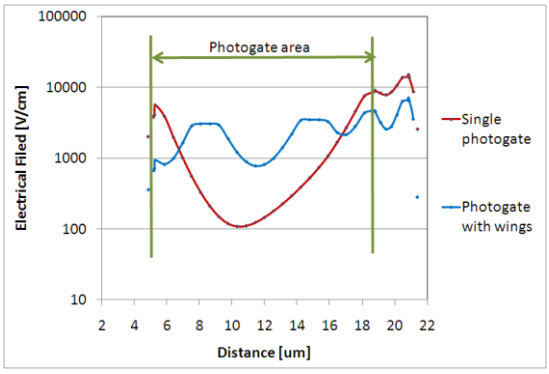

Fig.11. Simulation results for maximizing electrical field in pixel of final imager

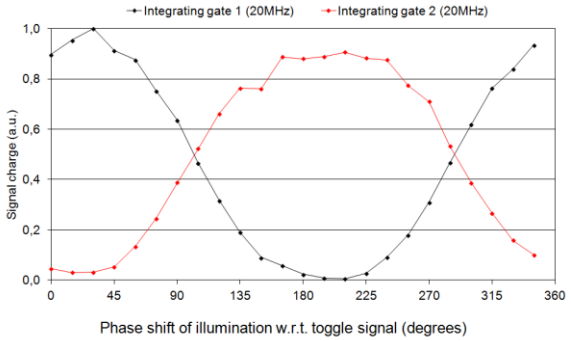

Fig.12. Collected signal under opposite integrating gates as a function of phase shift of illumination (duty cycle 33%).

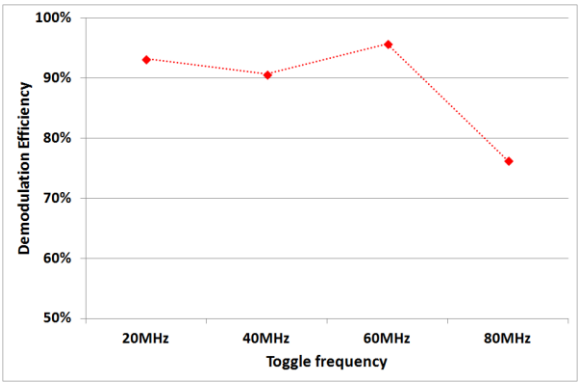

Fig.13. Demodulation efficiency vs. frequency for red laser illumination

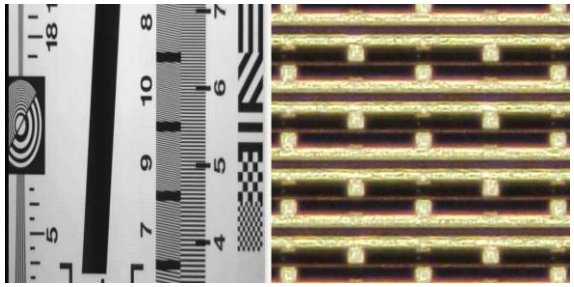

Fig.14. Detail of first image of final imager at 80MHz toggling, non-modulated illumination; and photo of detail of image section before final light screen deposition

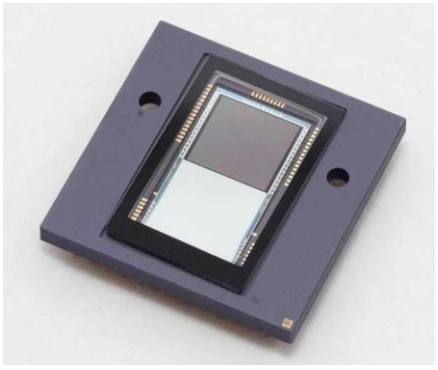

Fig.15. Photograph of assembled device

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