

Dark Current Reduction in Image Sensors Through Metals Gettering : A Critical Review of Disruptive Techniques

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Abstract

Dark current reduction in image sensing devices is one of the challenging tasks, as the metal contamination requirements become stringent ($<1E5$ atoms/cm²) for future technology nodes. With the advent of backside illumination (BSI), the stacked image sensors demand for efficient gettering mechanisms for better device performance and yield (DPY). It is the purpose of the present paper to introduce the most advanced disruptive gettering schemes, based on Varian's highly differentiated Process Temperature Control systems. The application space for the cryogenic and heated carbon implants with specific reference to the front and backside illuminated image sensing devices, will be discussed.

1. Introduction

As consumers demand more for high performance image processing than clicking a mere picture or video, from their mobile communication devices, such as smartphones and tablets, the need to incorporate more functionality into the image sensing devices arises more than ever before, for the future technology nodes. A stacked image sensor, a characteristic of the backside illuminated (BSI) CMOS Image Sensors (CIS), is one such device enabling high performance image processing in a more compact 3-D chip [1,2]. With the current pixel technology at around 1 μ m node, digital cameras with >10 megapixel resolution are commercially available in the market today. Processing of such large image related information with speed and accuracy, can only be accomplished with the help of an on-board digital signal processor (DSP) and some cache memory. Note that the DSP and memory might be manufactured with 65 nm or even more advanced technology nodes. A stacked structure thus mainly consists of two equal and most important components; (i) an image sensor and (ii) a signal processor. Stacking up of two such functions has been successfully demonstrated with the help of Through Silicon-Via (TSV) interconnecting technology [3]. However, TSVs are filled with copper paste and cured at 200~300°C, to establish the electrical connectivity between the sensor and the signal processor. It is well known that copper diffuses rather fast in silicon even at low temperature anneals [4]. It is well proven that the presence of such metal impurity in the photodiode region of an image sensor will be detrimental to the device performance.

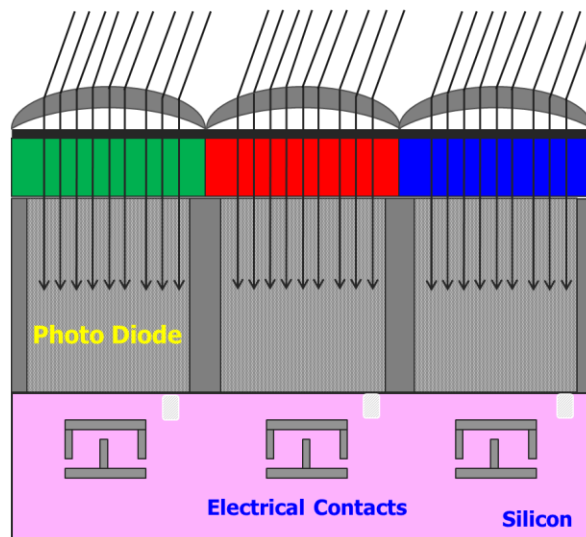


Figure 1. The schematic of a backside illuminated (BSI) Image sensor.

It has been theoretically estimated that the presence of a single metal impurity atom in such a CIS pixel severely degrades its performance, leading up to the device failure [5]. The mechanism is such that the presence of a metal impurity gives rise to deep level defects in the bandgap of silicon (Si), as shown in Fig.2. Depending on its capture cross-section to the electrical charge stored in the photodiode, these defect levels act as generation and recombination centers, resulting in dark currents, comparable to the original signal strength in the sensor [6-9]. It is noteworthy to mention other processing steps, such as implant, anneal, epitaxy, etch, in addition to BSI specific, wafer thinning, polishing, stress relieving, were also considered as a major source

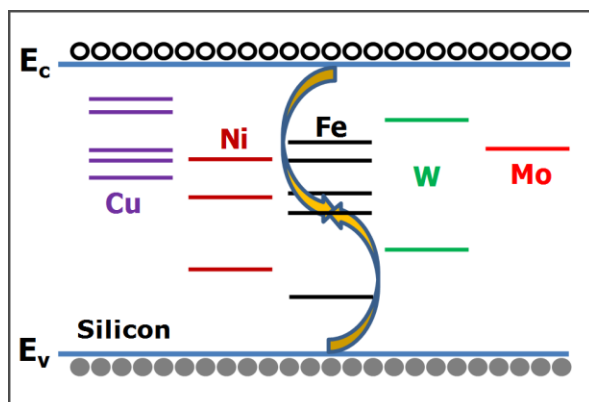


Figure 2. The relative positions of the metal induced deep level defects in silicon.

of metal contamination. There are existing mechanisms to getter these metal impurities. Magic denuded zone (MDZ) is one such approach [10]. Given its empirical nature, it is quite challenging to achieve a reliable gettering. Moreover, its adaptation to BSI technology is questionable. Hence, there is a need for a simple and efficient gettering of these metal contaminants in image sensing devices. This is especially true for the stacked sensors. It is the purpose of this paper to present advanced gettering schemes, based on Varian's highly proprietary and differentiated, disruptive techniques, namely, Process Temperature Control systems II (cryogenic) & III (heated).

The salient features of our single wafer, high energy ion implanter, specially equipped with metals reduction kit, will also be presented. The dynamics of the gettering will be discussed with the help of cross-sectional TEM images. The evidence for the trapping of the metal contaminants at the gettering sites will be presented, with the help of SIMS profiles.

2. Experimental

All the implants in this work were carried out on our single wafer, medium current ion implanter, VIISa 900XPT. Its salient features include precise angle control, maximum productivity (500WPH), extremely low metal/particle contamination and seamless process transferability with Varian's other implanters. The unique architecture style of our medium current and high energy ion implanters (VIISa HE-XP and VIISa 3000XP) provides the ability to cover the

entire dose-energy requirements of the CIS manufacturers, in terms of gettering and other doping requirements. It may be remembered that an ion implant at room temperature creates significant damage to the crystal lattice. As part of our strategic initiative to provide solutions to the implant related damage (Damage Engineering), Varian has developed cryogenic and heated implant capabilities. While a cryogenic implant is proven to be very effective in eliminating end-of-range related defects, heated implant dynamically anneals out point related defects during the implant itself. Both capabilities address distinct application spaces, thus improving device performance by lowering the leakage currents. In specific, the application space of these products with reference to the frontside and backside illuminated image sensing products, will be discussed in this paper, from the gettering standpoint.

3. Results and Discussion

The gettering schemes discussed in this paper are mainly based on carbon implants. However, these can be easily transferred to other species, namely, oxygen, hydrogen, and nitrogen, giving enough choice for the CIS manufacturers. Each one of these candidates has its own merits and demerits. While oxygen implants tend to severely degrade the mechanical strength and thus warping the Si substrate, boron and phosphorus tend to alter the polarity of the substrate leading to latching effects with the device layer. Further, the bond strength between these species and the metal impurities is so weak that the subsequent thermal cycles set these contaminants free to further diffuse in to the device layer. On the other hand, it is well known that the implantation of carbon into silicon results in the formation of Si-C complexes, which indeed play a critical role in the nucleation of oxygen precipitates. It is well documented in the literature that an oxygen precipitate is the necessary and sufficient condition to getter any kind of metallic impurity [9-11]. Given its highest electron affinity for any given metal, oxygen thus getters these contaminants by forming complexes like, ZnO, FeO, CuO, NiO, MoO₂ and W₂O₃. It may be noted that in an isolated report, Koyama suggested that carbon doesn't necessarily participate in the nucleation process [12].

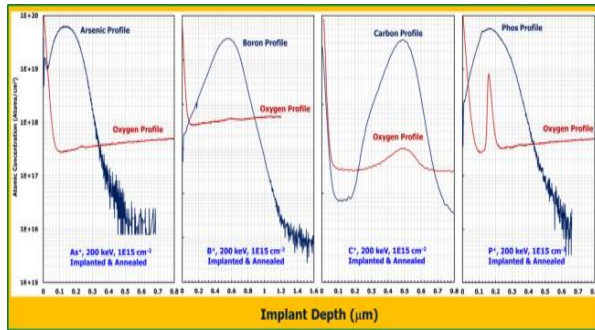


Figure 3. The nucleation of oxygen in As⁺, B⁺, C⁺ and P⁺ implanted Si (@RT), as demonstrated with SIMS profiles.

To further substantiate our claim that carbon is the key for effective gettering, we have implanted As⁺, B⁺, P⁺, & C⁺ species of same energy into silicon with a dose of $1\text{E}15\text{ cm}^{-2}$. The samples were then subjected to anneal at 1000°C in nitrogen ambient. The precipitation of oxygen is very exclusive to the carbon implant, as shown in the SIMS profiles [Fig.3]. Further, the precipitation of Cu, Fe, Ni and Ti metal impurities at the gettering layer was much higher in the C+ implanted, than the rest. The sharp oxygen spike in the phos implanted sample was found to be ineffective in gettering the metal impurities. Thus it is proven to be that carbon is the key for effective gettering. When coupled with the disruptive techniques (cold/hot carbon), it will meet the stringent contamination requirements of the current and future technology nodes, whose device performance severely degrades even with the presence of a single metal impurity atom in the photodiode.

An interesting observation can be made from the cross-sectional TEM (XTEM) images taken on as-implanted wafers at room and cold temperatures, as shown in Fig. 4(a) and (d) respectively. Cold carbon implant shows an abrupt and thick amorphized region, which is completely absent from the room temperature implant. The formation of such layer is attributed to the damage accumulation of the point defects and their complexes, as successive cascades are created by the incident ions [13-15]. Self-annihilation of these point defects is severely suppressed by the cold temperature at which these gettering implants were carried out. Such a stable and well defined amorphous layer is critical to precisely position the gettering layer at a predetermined depth.

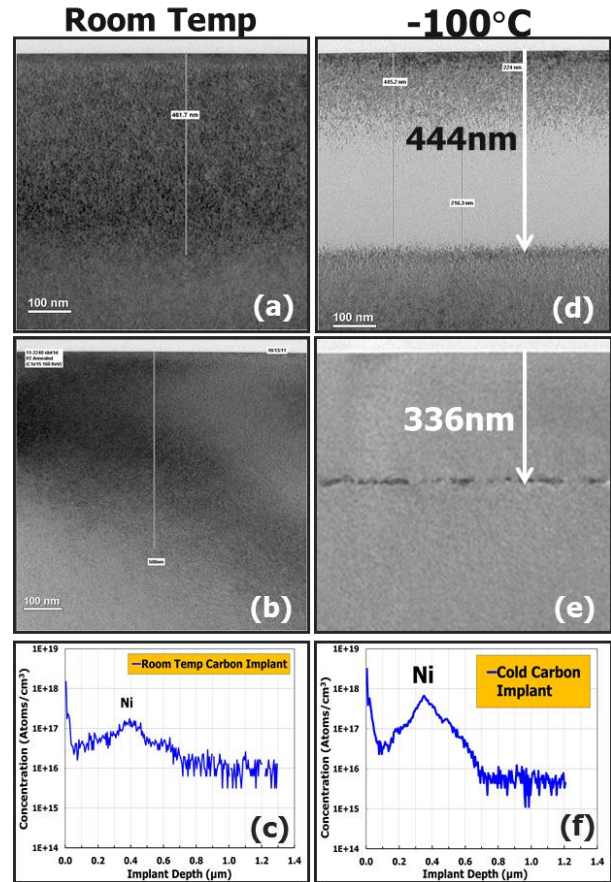


Figure 4. Cross-sectional TEM images of RT and cold carbon implanted Si. SIMS profiles of gettered metal impurities.

When these are subjected to an anneal, in order to quench the impurities, one can clearly observe the formation a deep buried C⁺ gettering layer, as shown in Fig.4(e). Note that, it should be located in close proximity to the device layer to prevent the metal impurities from getting into the device region. Its position from the Si surface can be easily adjusted by changing the C⁺ ion energy. The gettering of nickel in cold carbon implanted wafer was much more efficient than the room temperature implanted, as seen from the SIMS profiles (Fig. 4c & 4f). The same argument holds good for any other metal impurity. Such a breakthrough could only be achieved with our disruptive approach; a cryogenic carbon implant. It thus supersedes all the existing mechanisms including magic denuded zones.

Since the manufacturing techniques for front (FSI) and backside illuminated (BSI) CIS products are somewhat different, the origin of metal contamination could be different too. The FSI

sensors are usually built on top of the bulk substrate. Hence, the main source of contamination for this type of products could be the bulk substrate itself. With 650 μm thickness, it acts as a reservoir of metal impurities, which originate from both internal and external sources. Therefore the formation of a deep buried gettering layer, yet in close proximity to the device, will be a strategic solution for frontside illuminated products.

In the case of BSI products, the bulk substrate will be recessed down to 10 microns and then bonded to an image processor through copper filled TSVs. In this case, TSVs could be main source of contamination [16]. However, the mechanical strength of such an extremely thin device layer is somewhat questionable, due to the the grinding and the subsequent stress relieving techniques. Hence any process related damage, like photodiode and its isolation implants, may have some adverse impact on the device performance. It is extremely important to dynamically anneal out such defects. Heated carbon implant capability, our second disruptive approach, will address such problems by dynamically annealing out the implant related damage during the implant itself, by heating the wafer to a desired temperature.

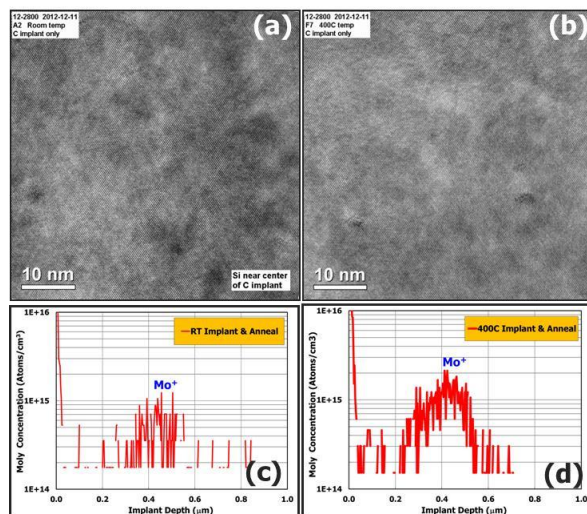


Figure 5. Cross-sectional TEM images and Sims profiles in carbon implanted wafers at room temperature [(a) & (c)] and at 400°C [(b) & (d)].

As shown in Fig.5, it is quite evident from the cross-sectional TEM image that the heated carbon implant (Fig.5b) shows less atomic defects, as

against the room temperature implanted one. Accordingly, it getters better than RT implanted, as seen from the Moly SIMS profiles (5c & d).

In conclusion, novel gettering schemes based on cryogenic and heated carbon implants were presented as device performance and yield enhancement knobs for the next generation image sensors. The seamless transferability of these disruptive techniques offers the choice among the FSI and BSI CIS manufacturers to optimize the process accordingly.

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