Architecture and Development of Next Generation Small BSI Pixels

H. Tian, H. Komori, G. Agranov, J. Bai, J. Hynecek, C. Baron, H-W. Lee, X. Zhao, W. Gazeley, D. Tekleab, S. Nagaraja, W. Gao, P. Adepu, V. Rajasekaran, A. Rayankula, N. Li, U. Boettiger, M. Mooney, B. Vaartstra

Aptina Imaging, 3080 North First Street, San Jose, CA 95134, htian@aptina.com

Abstract

This paper presents recent results from the development of our next generation small back side illuminated (BSI) pixels. According to the trend of pixel scaling [1], next generation small pixels will be at about 1.1um to 0.9um in size, achieving higher performance, and offering more advanced features than current pixels. Presented are the basic optical and electrical characteristics of the next generation 1.1um and 0.9um pixels. Pixel design concept and implementation including process and circuitry are discussed. The paper also presents a novel multiple-conversion-gain architecture for small pixels

1. BSI technology development

BSI technology allows aggressive reduction of pixel size and more symmetrical pixel design. Small BSI pixels have gained popularity in mobile and digital still camera (DSC) applications. Today 1.4um BSI pixels and 1.1um BSI pixels are widely used in production, while designers of image sensors are actively working on the next generation of 1.1µm and 0.9um pixels. Pixel size reduction and pixel performance enhancement remain the most powerful driving force for new technologies and innovations in pixel development.

Aptina continues to improve its BSI pixel technology. Figure 1 compares the pixel circuit schematic of the 1st generation 1.1um pixel and one of the 2nd generation pixels. As we can reduce the transistor numbers in the 2nd generation pixel, it offers much larger photo-diode area and less shallow trench isolation (STI) area. This leads to large charge storage capacity and better quantum efficiency (QE). The photo-diode depth is also significantly increased which enables ~30% thicker BSI silicon. As a result both red QE and signal-to-noise ratio (SNR) are significantly better. Pixel implants are optimized to minimize the dark current and to reduce hot pixel count. A novel color filter (CFA) process is developed to maximize the QE and minimize the crosstalk. The optical stack on top of Silicon is carefully optimized, and new material for optical anti-reflection coating is adopted to minimize reflective loss from optical stack.

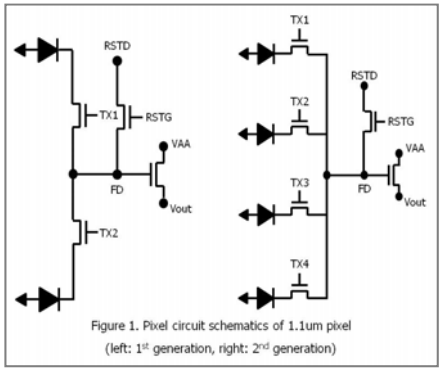

Figure 1. Pixel circuit schematics of 1.1um pixel (left: 1st generation, right: 2nd generation)

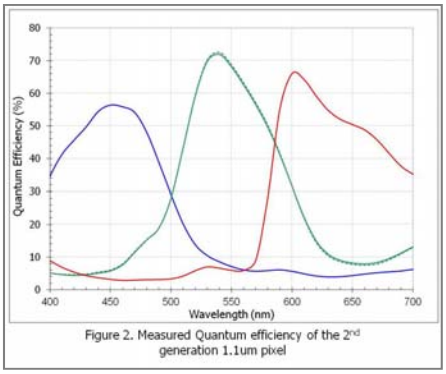

Figure 2. Measured Quantum efficiency of the 2nd generation 1.1um pixel

The resulting 2nd generation of 1.1um pixel achieves SNR10 of 125lux. This is about 25lux better than for the 1st generation 1.1um pixel performance. Figure 2 shows the measured quantum efficiency. Compared to the 1st generation 1.1um pixel, peak QE is increased while crosstalk is significantly reduced across the spectrum. Full well capacity of the 2nd generation 1.1um pixel is about 35% higher, while dark current is reduced. Table 1 summarizes the key parameter improvement of the 1.1um pixels.

Table 1. Performance of 1.1um Pixels

	Unit	1st generation	2nd generation
Peak QE	%	65	72
SNR10	lux	150	125
Full well capacity	e-	3700	5000
Dark current @ 60C	e-/s	20	9
Dynamic range	dB	66	69

2. 0.9um pixel development

The expectation for sub-micron pixels is to perform as well as, if not better than, current generation 1.1um pixels. Without new technology, the reduction of pixel size naturally leads to pixel performance degradation. Figure 3 illustrates that two key parameters, SNR and well capacity, degrade rather rapidly with shrinking pixel size if no other performance improvements are made. New technologies are required to fight this degradation trend, in order to successfully develop the sub-micron pixels.

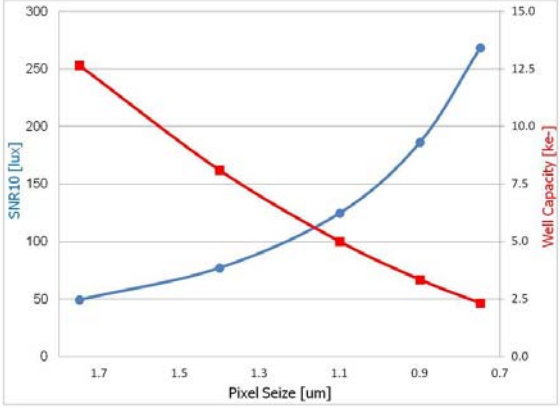

Figure 3. Scaling trend for major pixel performance

Quantum efficiency (QE) and spectral crosstalk are typically among the most important factors limiting SNR performance. As pixel size shrinks from 1.1um down to 0.9um, crosstalk shoots up dramatically in a conventional CFA system [2]. This is attributed to the diffraction effect: the incident light through a specific color filter is no longer confined within its associated photodiode. At Aptina a novel CFA process (Figure 4) has been developed to significantly reduce the crosstalk. The grid material is designed to provide additional focusing power when interacting with color filter. Other improvements of the pixel optical stack include further optimization of anti-reflective coating, fine tuning the optical stack height, and refining microlens design. We also applied tighter design rules to maintain the photodiode fill factor, and enhanced the silicon process to increase pixel quantum efficiency and reduce the electrical isolation region between pixels. Figure 5 presents simulated spectral QE characteristics for a 0.9um pixel, using 3D and FDTD models. With this new CFA process and photodiode enhancement, the expected 0.9um pixel spectral response approaches a similar level of the 1.1um pixel. This brings a 0.9um pixel performance close to the ideal scaling curve shown in Figure 3. To further improve SNR10 performance to reach the customer

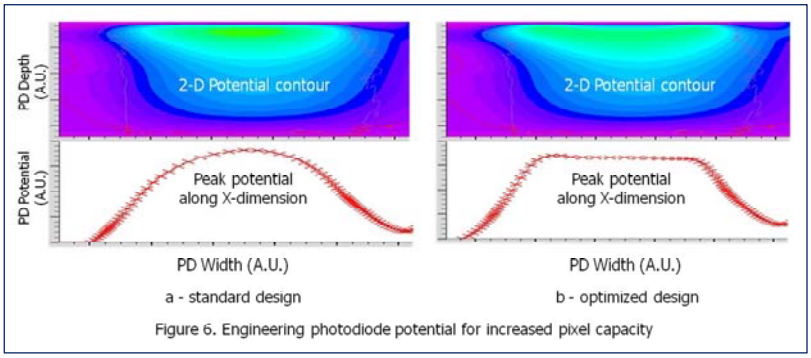

Figure 6. Engineering photodiode potential for increased pixel capacity

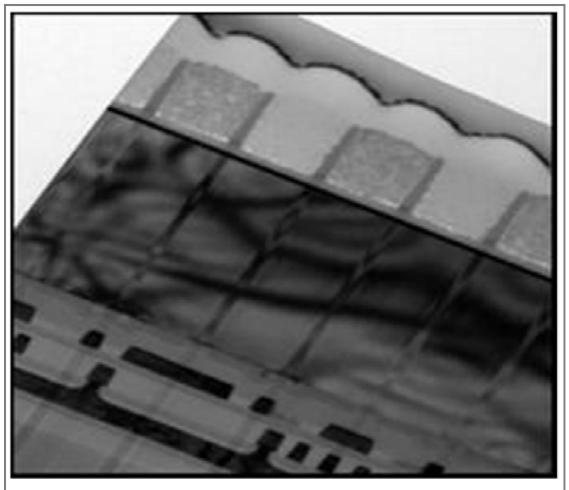
Figure 4. New CFA structure

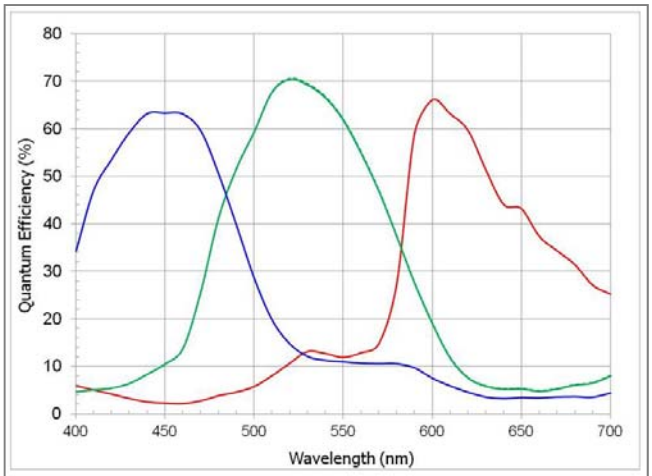

Figure 5. Simulated spectral response of 0.9um pixel

acceptance threshold, Aptina has also developed our Clarity+™ technology. It introduces panchromatic pixels into 50% of the sensor array, and thus reduces the light level required for SNR10 to about half of what's achieved without this technology.

One of the big challenges for 0.9um pixel development is pixel capacity. For a 0.9um pixel to reach the same well capacity as a 1.1um pixel, the charge storage capability of the photodiode needs to be maximized. This paper describes several approaches to increase pinned photodiode capacity. While tightening design rules and migrating to a more aggressive process node is an obvious trend in small pixel development, big improvement in pixel capacity can come from charge transfer gate (TX) design and engineering of photodiode (PD) with well optimized potential profile. As shown in Figure 6, the optimized design achieves a much wider peak potential region along photodiode width. This leads to higher electric field near the photodiode surface and thus higher full well capacity. Transfer gate in a BSI pixel serves as the transferring device during readout and provides anti-blooming path for the pixel. In a traditional pixel TX is made to be sufficiently long, in order to avoid punch-through, while achieving lag-free transfer and low dark current. Aptina developed a device to significantly shorten the TX length, while providing a better controlled anti-blooming path. The device is lag-free, and has built in potential to suppress the dark current and hot pixels associated with TX channel. The process integration of the new TX device is optimized to provide good misalignment tolerance and hence excellent manufacturability. As a result of these combined techniques, pixel capacity of 0.9um pixels can be brought to the level of current generation of 1.1um pixel. Figure 7 presents the image taken from 0.6Mpix pixel array with 0.9um pixel.

Figure 7. Image from 930 x 690 pixel array with 0.9um pixel

3. Multiple-conversion-gain pixel

As pixel size shrinks, it's critical to introduce more compelling features for better camera user experience. This paper presents a new pixel architecture, namely a multi-conversion-gain pixel which can greatly benefit the next generation of small pixels. It enables some highly desirable features for the small pixels such as extended dynamic

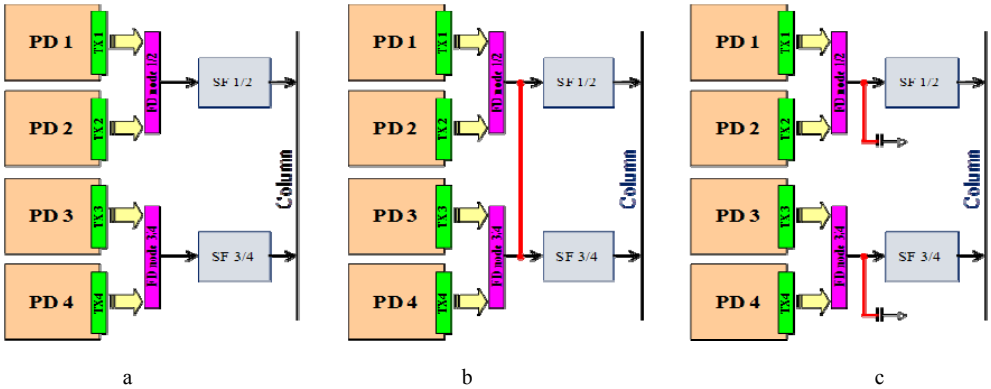

Figure 8. Structural view of pixel architecture

a - high conversion gain mode;
b - low conversion gain mode allowing pixel binning and high full well;
c – intermediate conversion gain mode

range, pixel level binning, adjustable conversion gain of the floating diffusion, and low readout noise. Figure 8 presents the structural view of this pixel architecture. Two floating diffusion nodes of neighboring pairs of pixels in traditional 1x2 common element pixel architecture (CEPA) can be combined into 1x4 CEPA by using additional switches between those pairs of pixels. When working in 1x2 CEPA mode (Fig 8a), high conversion gain and correspondingly low readout noise floor can be realized, leading to high performance at low light. When switched to 1x4 CEPA mode (Fig 8b), the pixel realizes high charge handling capacity and the ability to bin charge on the FD. The readout noise does not increase as much as the conversion gain reduction would suggest, thanks to the use of a distributed Source Follower (SF). This pixel structure allows several conversion gain choices for the FD simply by changing the mode of pixel operation (Fig 8c).

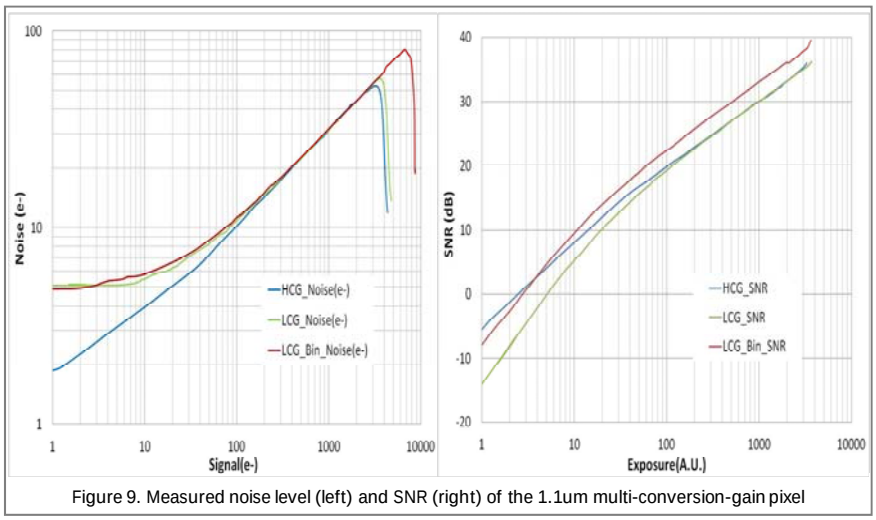

Figure 9. Measured noise level (left) and SNR (right) of the 1.1um multi-conversion-gain pixel

Symmetry is very important in the implementation of multi-conversion-gain pixel. Circuitry and pixel layout are carefully designed on 1.1um pixel. The measured 1x2 mode conversion gain is well above 200uV/e-, leading to excellent low light noise performance. At 1x4 mode the conversion is brought down to about 60uV/e-, sufficient to handle large charge capacity from multiple photo-diode. This is particularly useful for pixel binning, which improves SNR. Figure 9 shows the measured noise level and SNR performance of the various conversion gain modes. The HCG mode achieved very low noise floor of 1.6e, while LCG binning mode significantly boosted SNR by simultaneously accumulating and reading out charge from two photodiodes of the same color.

4. Conclusion

The paper summarizes recent results of photoelectrical characterization for our next generation of 1.1um pixel and 0.9um pixel. We consider quantum efficiency, crosstalk, full well capacity, dark current, readout noise, and major image quality. Through continuous technology innovation and development, these next generation pixels realized excellent performance. A multiple-conversion-gain pixel architecture and measured 1.1um pixel data with this architecture are also presented. The pixel achieved very low noise floor, while enabling pixel binning feature.

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