Blooming and Antiblooming in 1.1µm-Pixel CIS

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ABSTRACT

Blooming occurs when excess photo carriers in over-saturated pixels spill into adjacent pixels [1-2]. Conventional techniques developed for CCD imagers, such as charge-pumped antiblooming or vertical overflow drain (VOD), are difficult to be implemented in CIS, especially for BSI technology with very thin substrate. A separate lateral overflow drain (LOD) is not suitable for small pixels such as 1.1um or below. Since blooming takes place at the pixel level, signal-chain clipping or automatic exposure control in downstream circuits cannot solve the problem effectively. Therefore, antiblooming becomes an important and challenging subject for CIS design. Yet it is seldom discussed in recent literature.

In this article we present several new blooming characterization methods and blooming-related effects observed in our 3MP test chips with integrated 12-bit global ADCs using BSI technology, which has 1.1um pixel, 1.5T, 4-shared structure, operated at 32MHz pixel clock. Antiblooming is demonstrated by lateral overflow barrier control. Various 2x2 and 1x4 pixel designs are experimented to explore the tradeoffs among antiblooming, full well capacity (FWC), and dark leakage.

BLOOMING IN COLOR SENSORS

Blooming is often observed in photos on scenes with spectral highlights. A typical measurement procedure is to focus on a spot light 10% of the sensor height; the antiblooming factor X_{ab} is defined as the ratio of the light level to cause blooming (I_{bloom}) and the light level to saturate the sensor (I_{sat}) [3]. Antiblooming factor up to several thousands [3] or an I_{bloom} up to 10^5 lux [2] were achieved in CCDs, while for CIS they were seldom reported or specified in product data sheets.

In production wafer-level testing, different methods of blooming evaluation without any global lens are preferred. To study blooming in color sensors, we can saturate selective pixels using narrow-band filtered lights to create large contrast ratios among neighbor pixels. Figs. 1A~C show the response curves of R, Gr, Gb, B pixels under R, G, B lights, respectively for on experimental split. The analog chain is designed with a large swing at low gain such that the saturation levels are not clipped.

Multiple regions are clearly identifiable in the response curves depending on the saturation conditions of neighbor pixels. For instance, in Fig. 1A, under R light, all signals increase proportionally to integration time in Region-1 before saturation. In Region-2, R pixel is saturated; the charge spill from R into G and B can be clearly seen as the increase of slopes of G and B. In Region-3, both R & G are saturated. Spread of excess charges into B causes further increase of B slope. Eventually all pixels are saturated in Region-4. Similar behavior under G and B lights are observed in Figs. 1B and 1C. The fact that the slope of the sum of R, Gr, Gb, and B remains approximately constant throughout Regions-1 to Region-3 is a direct evidence of blooming where excess photo carriers almost entirely spill over into neighbors without being removed by recombination.

For quantitative comparison, we may define the blooming percentage from R to G (\boldsymbol{P}_{G}^{R}) and from R to B (\boldsymbol{P}_{B}^{R}) as

$$\boldsymbol{P}_{G}^{R} = \frac{\left(S_{G,2}^{R} - S_{G,l}^{R}\right)}{S_{R,l}^{R}}; \ \boldsymbol{P}_{B}^{R} = \frac{\left(S_{B,2}^{R} - S_{B,l}^{R}\right)}{S_{R,l}^{R}};$$
(1)

Where $S_{R,I}^{R}$, $S_{G,I}^{R}$, $S_{B,I}^{R}$ are response slopes of R, G, and B pixels under R light in Region-1 where R pixels are under-saturated; $S_{G,2}^{R}$ and $S_{B,2}^{R}$ are slopes of G and B pixels in Region-2 where R pixels are saturated. P_{R}^{G} , P_{B}^{G} , P_{R}^{B} , and P_{G}^{B} can be similarly defined. The blooming percentage should be nearly 0% for pixels with ideal antiblooming, while they could be close to 100% for pixels with poor antiblooming protection. Typically the symmetric relations such as $P_{R}^{G} = P_{R}^{G}$ are not expected due to the complicated layout and process asymmetry in shared pixel structures. A systematic characterization of all 6 factors for various process conditions is important to gain insights for pixel cell design.

BARRIER LOWERING EFFECTS

In Figs. 2A~C, multiple saturation levels are observed in different regions. Three discrete levels are distinguished as $(\Delta R_1 \sim \Delta G_1 \sim \Delta B_1) > \Delta G_2 > (\Delta R_2 \sim \Delta B_2)$. This saturation-level split can be understood as the electrostatic barrier lowering effect of unsaturated photodiodes on nearly saturated neighbors explained by the simplified potential diagrams in Fig. 3A. We may classify the states of a nearly saturated pixel into 4 cases according to the charge status of its neighbors, as illustrated in Fig. 3B. The 4 immediate neighbors, in horizontal and vertical directions, might be (1) all unsaturated, (2) 2 saturated and 2 unsaturated, (3) all quasi-saturated with the diagonal neighbors unsaturated, or (4) all saturated including the diagonal neighbors. Comparing to the final saturation in case (4), we observed exactly 3 different barrier lowering magnitudes in each of the case (1), (2), and (3) with respect to case (4), as shown in Fig. 3C. The difference between case (3) and case (4) indicates that the diagonal neighbors also have

indirect and secondary influence, but weaker than the immediate next neighbors on barrier lowering.

The physics causing the saturation split is considered similar to the well-known drain-induced barrier lowering (DIBL) effect in short-channel MOSFETs. Continuously shrinking the pixel pitch and tightening the spacing between adjacent photodiodes makes the barrier lowering an important way to study pixel isolation. The effect is expected to be more severe in 0.9um and smaller pixel generations.

LATERAL OVERFLOW BARRIER

To prevent charge spill and achieve antiblooming in small pixels, the transfer-gate device can be used as a lateral overflow control, or a floodgate. The relative height of the overflow barrier is determined by the transfer off-voltage (TXL) and the inter-pixel isolation structure, which in turn determines whether excess electrons would spread into neighbors or go to the floating nodes to be recombined with externally supplied holes.

Fig. 4A shows the dependence of the Gr and R response curves on TXL under G light. Fig. 4B shows the corresponding slopes of Gr and R when TXL changes. As TXL is gradually raised, the electron overflow barrier potential is lowered. Blooming can be effectively suppressed above -0.4V in this example, where the R slope remains almost unchanged from Region-1 to Region-2. Fig. 4C shows the charge summation of 4 pixels is no longer proportional to exposure after G pixels are saturated. Evidently, the loss of excess carriers takes place gradually when the overflow barrier is lowered.

The blooming percentage calculated according to formula (1) and the measured FWC are plotted against TXL in Fig. 4D. Simplified potential diagrams and the preferred path for excess carriers in two examples of blooming (TXL=-0.8V) and antiblooming (TXL=-0.4V) are shown in Fig. 5A and 5B, respectively.

As TXL goes higher and blooming is suppressed, however, FWC is lowered and dark leakage becomes higher. These are anticipated tradeoffs. One goal in small pixel design is to create a sufficient TXL operation window such that antiblooming, high FWC, and low dark current can be simultaneously achieved, or acceptably compromised.

The TXL operation window also depends on pixel structures. For a pixel without row-select (RSL) device, the floating diffusion node (FN) has to be pulled low to deactivate the source follower (SF) when it is not in the readout mode. As a result, TXL may need to be more negative in order to shut down the leakage current. With a RSL device, such constraint is relaxed. Under a proper FN bias, TXL can be less negative; therefore, it helps to create an antiblooming path under transfer gate. This is in general a design tradeoff since RSL reduces the photodiode fill factor.

BLOOMING AND T₀-OFFSET

An interesting side effect of blooming is found as the light dependence of the T_0 -offset, i.e., offset corresponding to zero integration time. In Fig. 6A, the T_0 -offset shows an abnormal increase beyond a certain light level at TXL=-0.8V and it returns normal when the blooming is suppressed at TXL=-0.4V in Fig. 6B. Fig. 6C shows the T_0 -offsets against light intensity. This phenomenon is attributed to pixel blooming during the long idle time when the integration time is short. Excess carriers flood the non-photodiode area during idle time and cannot be completely removed by photodiode reset. Some of the excess carriers may flow back to the photodiode after reset to cause an artificial signal offset, explained in Fig. 7 potential diagram.

Although idle-time blooming may be prevented by timing control, for example, multiple or periodic resetting the idle pixels, such approaches cannot prevent pixel blooming during actual integration. Thus, the blooming problem can only be solved on the device level, not on the circuit design level.

ANISOTROPIC BLOOMING

Furthermore, in Fig. 8, anisotropic blooming and the Gr-Gb response split are observed in some pixel designs. The physical cause is traced back to the structural difference, such as detailed implant conditions and process flows, between the isolation barriers in horizontal (row) and vertical (column) directions. In shared pixels, such as 1x2, 1x4, 2x2, or 2x4, asymmetry of layout and isolation structures among pixels often inevitably exists. Anisotropic blooming may cause image color artifacts worse than isotropic blooming; therefore, has to be avoided by careful pixel design.

CONCLUSIONS

In summary, antiblooming may be achieved by lateral overflow control through the transfer-gate off-voltage. However, the optimal pixel design with balanced antiblooming capability, full-well capacity, and dark leakage is still under investigation. On the other hand, we demonstrated that the blooming effects could serve as useful characterization and diagnosis tools to examine the inter-pixel isolation structure and various process and pixel design tradeoffs. To reach comparable or better antiblooming capabilities as reported in CCDs would be a crucial task in CIS pixel engineering, especially for sub-micron pixels.

REFERENCE

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Fig. 1: When blooming takes place in a color sensor under narrow-band R, G, B lights, the response curves show 3 or 4 clearly distinguishable operation regions, corresponding to the different saturation levels of neighboring pixels. In this example, the total responsivity, sum of of R, Gr, Gb, and B slopes, is approximately constant until all 4 pixels are saturated.



Fig. 2: Saturation levels of pixels of different colors under narrow-band R, G, and B lights show dependence on the charge states of neighbor photodiodes, which is attributed to the electrostatic barrier-lowering effects. Three levels of barrier lowering can be identified as: $(\Delta R_1 \sim \Delta G_1 \sim \Delta B_1) > \Delta G_2 > (\Delta R_2 \sim \Delta B_2)$.



Fig. 3: Simplified electronic potential diagrams to illustrate the electrostatic barrier-lowering effects. The different levels of barrier lowering can be explained by the difference of charge states of neighbor pixels.



Fig. 4A, 4B, 4C, and 4D: The degree of blooming can be controlled and suppressed by the off-voltage of transfer-gate (TXL).



Fig. 5: Simplified potential diagrams to illustrate the lateral overflow barrier control through transfer-gate off-voltage (TXL).



Fig. 6A: A side effect of blooming (TXL=-0.8V) is observed as the light dependent T₀-offset (offsets at zero integration time) of response curves. Fig. 6B & 6C: The abnormal light dependency disappears when blooming is suppressed when TXL>-0.4V.



Fig. 7: Excess carriers generated during pixel idle time flowing back to the photodiode after reset causes T_0 -offset. Fig. 8: Anisotropic blooming comparing pixel splits SP2 & SP3. Blooming can be a practical diagnostic tool for pixel design.

