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A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout

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Abstract – **This paper proposes a 17.7Mpixel CMOS image sensor with 120frames/s readout at 12b ADC, maximum data rate 34.8Gbps. Dual row-signal readout, a SLVS with Embedded Clock interfaces (2.376Gbps x 16ch) and fast column-counters (2.376GHz counts) in Single-Slope ADC are adopted. The dynamic range and the power consumption are 77.6dB and 3.0W, respectively at 34.8Gbps.**

I. INTRODUCTION

Recently, the demands to achieve both high-speed and high quality imaging – including high AD resolution – have increased. So one of our target specification is Ultra High Definition format (8k4k: 7680 x 4320) with 12b at least 60frames/s, and at 120fps if possible.
The data rate reaches to 24Gbits/s at 8k4k 60fps with 12b, while reported CMOS image sensors have reached up to 6.5Gbits/s [1-5].
This paper presents a 34.8Gbits/s readout CMOS image sensor with high image quality, which realize 17.7M pixels (8192 x 2160) at 120frames/s with 12b resolution and dynamic range of over 75dB (one of the highest image quality, compared with data from [2]). In order to realize a 8k4k 120fps readout with 12b, we used a digital signal processor that expanded the 8k2k of sensor data to 8k4k (8192 x 4320).
In CMOS image sensors, generally there is a trade off between high speed imaging and high image quality. This is because high speed imaging brings high power with high thermal noise which also degrades the signal quality, and because fast data transfer may require more output pins, bringing more interference.

II. ARCHITECTURE

We have solved the trade off using Single-Slope ADC (SS-ADC) which is a very popular architecture for modern CMOS image sensors, because the analog circuit area per column is smaller and progress of fabrication process contributes to diminish the digital circuit area.
First solution is hybrid column counters for SS-ADC that enables very fast A/D conversion with the least power consumption. Second solution is Scalable Low Voltage Signaling interface with Embedded Clock (SLVS-EC) that achieved 2.376Gbits/s per channel.

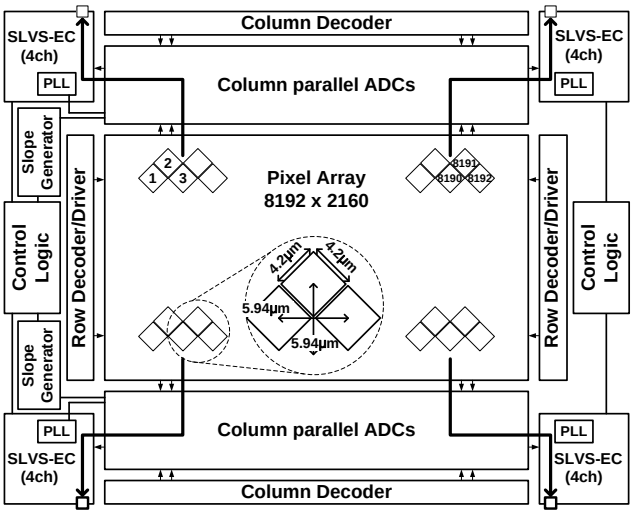

Figure 1: Block Diagram

Figure 1 shows the block diagram of the CMOS image sensor. This sensor consists of a pixel array, column parallel ADCs with upper and lower side allocation, control logic circuits with left and right side allocation, and SLVS-EC of 4 channels at each corner. These

four SLVS-EC circuits receive the sensor input clock individually. The effective pixel array consists of 8192(H) x 2160(V) 4T pixels placed in a zigzag manner; the pixel unit cell size is 4.2μm(H) x 4.2μm(V), the pixel pitch is 5.94μm(H) x 5.94μm(V), the column circuit pitch is 2.97μm. The size of the imaging region is 24.3mm(H) x 12.8mm(V) compatible with the 27.5mm optical format. In the sensor, vertical pixel readout lines are divided into 2 sides – up and down image area – to realize high speed analog readout so that a single row-signal of both sides is read out and converted into digital data simultaneously. Then, ADC outputs are transferred to the left or right SLVS-EC circuits at the same time through sense-amplifier circuits. Since sensor readout data are output from the SLVS-EC circuits at 4 corners simultaneously, they are forwarded into frame memory out of the sensor, if a raster scanning is needed for data processing.

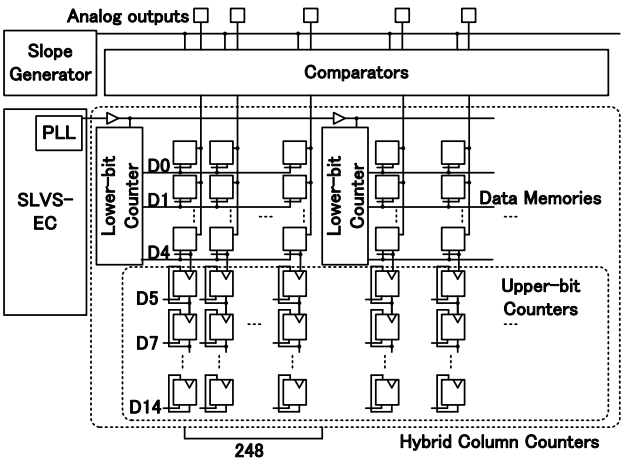

Figure 2: Block Diagram of this SS-ADC

Figure 2 shows the block diagram of this SS-ADC. The SS-ADC is composed of comparators, hybrid column counters including data memories, and slope generator with regulation circuits for an imaging offset between up and down image area. The Imaging offset regulation has a 16b resolution of full scale, which is sufficient not to be recognized as the divided imaging area. SS-ADCs are generally thought to be difficult to get both high-speed and high A/D resolution [2, 4, 6], because the A/D resolution is restricted by the number of clock cycles. Concretely speaking, SS-ADCs with high speed column-counters have 2 big problems, power consumption of column-counters and count-clock signal quality. First, power of column-counters is consumed more in proportion to the number of columns and/or ADC count-clock frequency increase. This degrades image quality due to a chip thermal rise and/or counting errors by IR-drop of count-clock line. This results from the fact that lower bit column-counters which consume more power exist in every single column. Secondly, quality of fast count-clock signal is difficult to be maintained especially at the end of column-counters, because the count-clock signal from PLL is delivered to every single column-counter and degrades gradually. In the other way to achieve high speed, multiple-ramp SS-ADC has been reported [6], but this architecture is difficult to implement and also it consumes more area per column and more power, which reduces advantage of SS-ADC. We realized a SS-ADC operating up to 2.376GHz by re-structuring column-counters (hybrid column counters), which consist of 2 blocks as shown in Figure 2. One is lower 5bit counters in every 248columns, and the other is upper 9bit counters in every single column which are connected with lower bit counter outputs. This re-structuring counter provides a solution to the 2 big problems as mentioned before, by decreasing both power consumption of column-counters and degradation of clock signal quality. The pixel signal can be converted to the utmost 14b digital code by the column parallel slope ADCs.

Figure 3 shows its timing diagram of 1 horizontal scanning period. Dual row-signal readout expands one horizontal scanning period to double of conventional readout, and A/D conversion and horizontal data transfer are done simultaneously. It is once in one scanning vertical period at most that the offset regulation for upper and lower image areas is applied to single slope generators through a 3-wire serial interface from Digital Processing Unit (DSP) out of the sensor. The horizontal scanning time is set to 7.4μs allowing 120fps for 17.7Mpixel with 12b ADC, where hybrid column counters counts at 2.376GHz and SLVS-EC circuit operates up to 2.376Gbits/s per channel at an input clock of 148.5MHz.

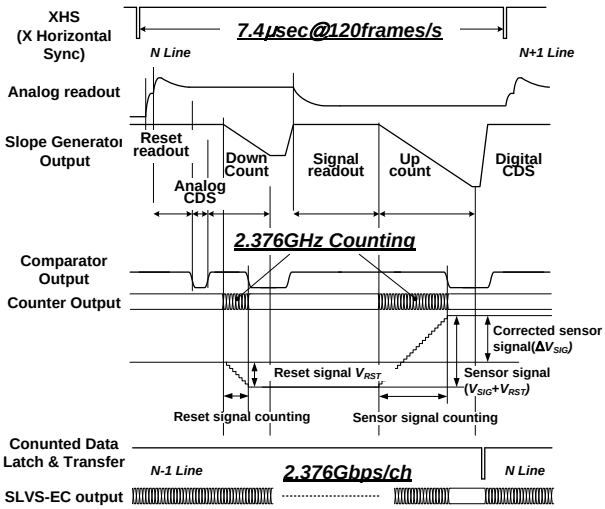

Figure 3: Timing diagram
of one horizontal scanning period

III. MEASUMENT RESULTS

Figure 4 shows the signal quality of SLVS-EC. The differential voltage and the common mode voltage of SLVS-EC signal are 400mV and 200mV respectively. The other advantage of this SLVS-EC is that it is unnecessary for channel skew regulation of transmission line and it can translate data at half power of conventional sub-LVDS, totally around 200mW at 34.8Gbps.

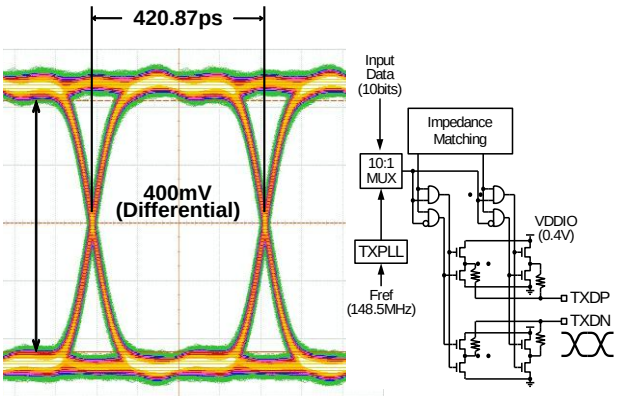

Figure 4: Signal quality of SLVS-EC

The total jitter 42.4ps (around 0.1UI) at 2.376Gbits/s through wire length of 300mm is sufficient for 1E-15 bit error rate which is necessary for high reliable image data transmission.

Figure 5 shows a chip micrograph of our CMOS image sensor. When full 19.3Megapixels including optical black area are readout at 120fps 12b, maximum data rate gets to 34.8Gbps after 8b10b encoding.

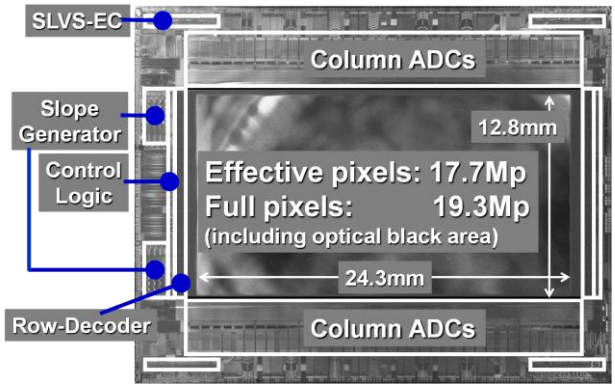

Figure 5: Chip Micrograph

Figure 6 shows sample images taken at 34.8Gbps operation, which is 8192(H) x 4320(V) after pixel interpolation of vertical direction using software treatment. Additional software treatments have not been adapted for this image. In addition image distortion due to the rolling shutter can be negligible at 120frames/s compared to that of 48frames/s.

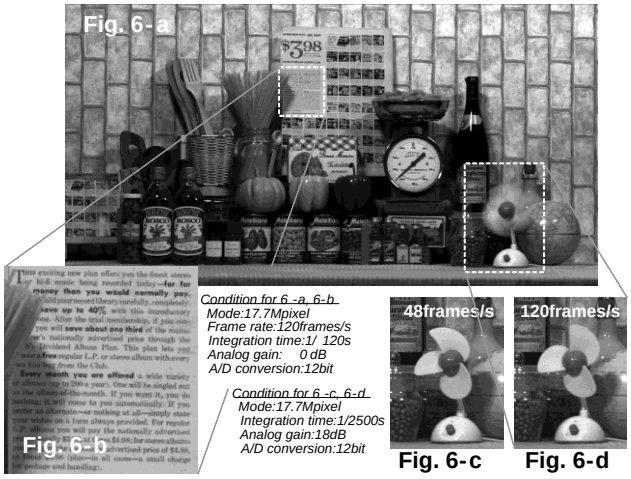

Figure 6: Sample images

Noise characteristics are shown in Figure 7. This data shows that the image quality is maintained even at 2376MHz counting, which leads to high speed imaging with sufficient dynamic range. Figure 8 indicates the sensor linearity. The linearity of this sensor depends on the characteristics of the source follower, comparator, and slope generator. We defined the nonlinearity value as the ratio of the deviation from linear approximation line to saturation signal. Measured nonlinearity at

120frames/s is 0.6% at 90% of saturation.

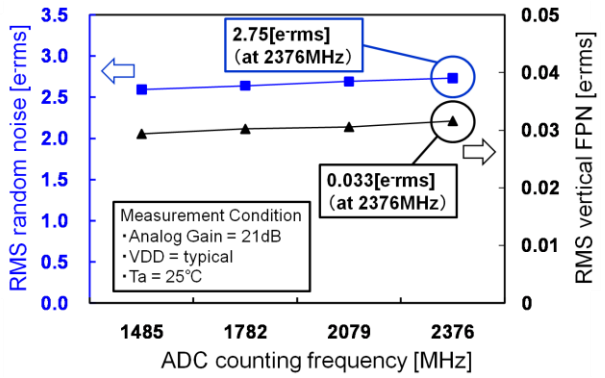

Figure 7: Noise Characteristics

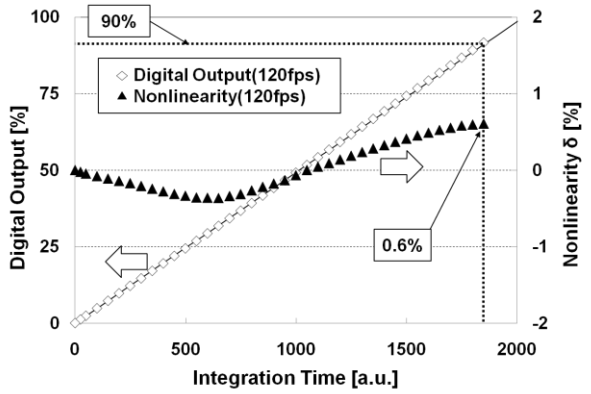

Figure 8: Sensor Linearity

Chip specifications are summarized in Table 1. This sensor is fabricated in a 90nm 1P4M CMOS sensor process. The supply voltages are 2.9V for pixel, 2.7V for the analog circuits, 1.2V for the digital circuits, and 0.4V for the SLVS-EC circuits.

Table 1: Chip Specifications

Fabrication Process	90nm 1P 4M
Supply Voltage	2.9V / 2.7V / 1.2V / 0.4V
Number of effective pixels	8192 (H) x 2160 (V)
Pixel size	4.2 μm (H) x 4.2 μm (V)
Aperture ratio	51% w/o on-chip microlens
Max. data rate	34.8Gbits/s w/ data clocks
Max. frame rate	120 frames/s(fps) at 12b ADC
Power consumption	3.0W at 120fps
Saturation signal	21,000e- at 60 C
Sensitivity	40,000e-/lx-s At 3200K light source with IR cut filter of 650nm cut-off
Image lag	Below measurement threshold
RMS random noise	2.75e-rms at 120fps (AnalogGain:21dB)
RMS vertical FPN	0.033e-rms at 120fps w/o additional correction circuit
Dynamic range	77.6dB at 120fps

The sensor performance is effective 17.7Mpixel 120fps at 12b, and 60fps at 14b resolution. Random noise of 2.75e-rms and a saturation signal of 21,000e- are achieved at 120fps at 12b resolution, so dynamic range is 77.6dB. A sensitivity of 40,000e-/lux*s is achieved. The measured power consumption is typically 3.0W.

IV. CONCLUSION

A 17.7Mpixel CMOS image sensor has realized 120frames/s at 12b ADC, maximum data rate 34.8Gbps. Dual row-signal readout, a SLVS with Embedded Clock interfaces (2.376Gbps x 16ch) and hybrid column-counters (2.376GHz counts) in single slope ADC architecture are adopted. The proposed sensor can realized 5times faster compared to the trend of CMOS image sensor with sufficient dynamic range.

ACKNOWLEDGMENT

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References:

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