A High-Speed Low-Noise CIS with 12b 2-stage Pipelined Cyclic ADCs

JongHo Park*, Satoshi Aoyama*, Takashi Watanabe*, Tomohiko Kosugi*, Zheng Liu*, Tomoyuki Akahori*, Masaaki Sasaki*, Keigo Isobe*, Yuichi Kaneko*, Kazuki Muramatsu*, Tetsuya Iida*, and Shoji Kawahito*†

*Brookman Technology, Inc., 3-1-7 Wajiyama, Nakaku, Hamamatsu 432-8003, Japan
Phone/Fax: +81-53-474-4540, E-mail:parkjh@brookmantech.com
†Research Institute of Electronics, Shizuoka University, Japan

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This paper presents a high speed 1.3M pixel 2000fps CIS operating with low power consumption less than 0.99W. To achieve high speed column signal processing, 2-stage hybrid cyclic ADCs is adopted. The 5.6μm-square global shutter active pixel has high sensitivity of 5 V/lx· s with low noise performance of 7e-$_{rms}$.

1. Introduction

A high speed CMOS image sensor (CIS) has been suffering from difficulties of the performance improvement such as sensitivity, noise and power consumption because of its global shutter and high speed readout operations. Especially, the noise of a global shutter pixel is as high as 10e-rms because of a remained kTC noise after a CDS operation. Another problem of a high speed CIS is its high power consumption due to many high speed analog readout channels, which makes a camera system difficult to handle.

Our approach can address problems described above. True CDS applied to proposed pixel can remove the kTC noise like general 4-TR APS, thus low noise less than 10e-rms is achievable. Signal detection by charge transferring to a floating diffusion (FD) keeps the sensitivity high. Fully parallelized column signal processing including a horizontal scanning helps the sensor work at 2000fps. Two stage cyclic ADC with a class AB operational transconductance amplifier (OTA) enables the sensor to operate with low power consumption.

2. Sensor Architecture and signal flow

Fig. 1 illustrates the block diagram of the sensor. A pixel array is located in the center of the sensor. 2-stage cyclic ADCs followed by a sample and hold(S/H) circuit are located both above and below the pixel array. The sensor includes a reference generator, a PLL, an adder, and LVDS drivers.

A. Pixel structure

For a low-noise global shutter, a new pixel structure with an additional analog charge storage which allows true CDS operation to cancel kTC noise at the floating diffusion is developed. The pixel is carefully designed to achieve low-noise high-speed readout and sufficiently-high parasitic light sensitivity.

B. Column structure

Fig. 2. shows a block diagram of column circuits which includes a novel 2-stage cyclic ADC. A S/H circuit, 1st cyclic ADC, 2nd cyclic ADC, registers and CML drivers for scanning are the main parts of the circuits. 2-stage cyclic ADCs perform a high speed analog to digital conversion. Redundant binary (RB) code from the ADC is converted to a binary code by a column adder. After that, horizontal scanning is carried out using CML driver and horizontal scanner. A scanned data is restored and latched by a sense amplifier, and final output is serialized before the data is output through a LVDS driver. Total output rate of 4 channel LVDS drivers reaches to 33.8Gbps.

3. 2-stage cyclic ADC

A. Architecture

As 1 horizontal period (1H) is 1us, a two stage pipelined cyclic ADC plays very important role to achieve high speed column signal processing within 1us. In this sensor, several operations including a signal sampling, A to D conversions (one of the two stage is for an upper 4bit and the other is for a lower 8bit), and horizontal scannings are fully parallelized with a pipelined architecture. Shortly, operations described above are performed at the same time. Fig. 3. shows detailed schematic diagram of the 2-stage cyclic ADC. The pipelined S/H circuits are embedded in the first cyclic ADC without any additional amplifier. The placement and routing of the each block are extremely cared and the RTZ technique [1]

is also adopted to minimize the coupling noise between a digital routing and a sensitive analog node. Capacitance of the 1st ADC is optimized with relatively large value compared to that of the 2nd ADC for low noise performance. An amplifier with a class AB driver is used for low power and high speed response. As the output of the 1st ADC after its 4bit A/D conversion is amplified with the gain of 16, the 2nd ADC is allowed to operate with lower currents and a smaller capacitance. Furthermore, the ADC except the S/H stage has been designed with low voltage 1.8V Tr. for saving power consumption.

B. Operation

Fig. 4. shows a horizontal timing diagram that several major signals and corresponding operations of the sensor are included. In the operation, a reset level is sampled onto the S/H circuit after the signal RST is activated. After the reset sampling, a CDS operation is performed by sampling a signal level after the signal TX is turned on. An OTA of the 1st cyclic ADC is used for the CDS operation during the time t_{CDS} when the 1st cyclic ADC is paused. Therefore, the S/H does not contain an OTA, which results in low power consumption and low noise performance. Upper 4bit from most significant bit (MSB) to 4th bit is determined by the 1st cyclic ADC after the CDS operation and then the remained bits are decided by the 2nd cyclic ADC. The 2nd cyclic ADC operates faster than the 1st one because the sampling and feedback capacitors are optimized to be small based on an effective analog gain of upper bit and a settling error. Once 12bit A/D conversion is done, the horizontal scanning is stated at the time t_{scan}. The required time from sampling to ADC is only 954ns, although the latency is 2.5 times of a horizontal period.

4. Measurement

Fig. 5. shows a micrograph of the fabricated sensor. The technology used in this sensor is 0.18μm 1P4M CIS process. Fig. 6. shows a relation between signal and effective noise when illuminance is varied. In this result, 1LSB corresponds to 244 μV with 1V reference at 12b resolution. The measurements were performed at room temperature with IR cut filter. Conversion gain obtained from the cross points where the photon shot noise becomes 1 electron is 41 μV/e-. A sensitivity is 5.04 V/lx· s. An input referred dark noise obtained from median of 10,000 pixels is 6.82e^-_{rms} when an analog gain 2 is applied in the CDS operation as shown in Fig. 7. Measured ADC's noise and power consumption are 299μVrms and 118μW, respectively. Table 1 shows FoM comparison of some major works based on several column parallel ADC types (from left: $\Delta\sum$, Successive approximation register, Single-slope, cyclic).

Fig. 8 shows several shots of a flying bird. The image was taken on the conditions of gain of 4, F1.4, and 1706fps. Specifications and characteristics are summarized in table 2.

5. Conclusion

In this paper, a high-speed low-noise CMOS image sensor with a column parallel 2-stage cyclic ADC is presented. Completely parallelized column signal processing makes it possible that the CDS and ADC operations are performed within 1us. Several techniques proposed in the paper make the ADC work with low power consumption of 118μW. The input referred total noise with analog gain of 2 is 7e^-rms although the sensor operates at 1700fps with a global shutter.

ACKNOWLEDGMENTS

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*Figure of merit (FoM) in table1 is given by

$$^{*1}FoM1 = \frac{N_{NOISE} \cdot G_{PA}}{f_H \cdot 2^N} \times 10^9 [e-/MHz \cdot Step],\ f_H = f_{FR} \cdot N_V$$

$$^{*1}FoM2 = \frac{Power \cdot N_{NOISE}}{f_p} \times 10^9 [e- \cdot nJ],\ f_p = f_{FR} \cdot N_V \cdot N_H$$

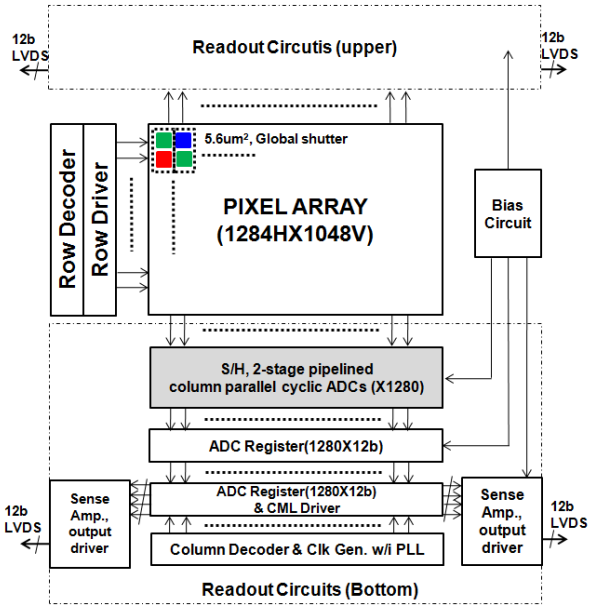

Fig. 1. Block diagram of the sensor.

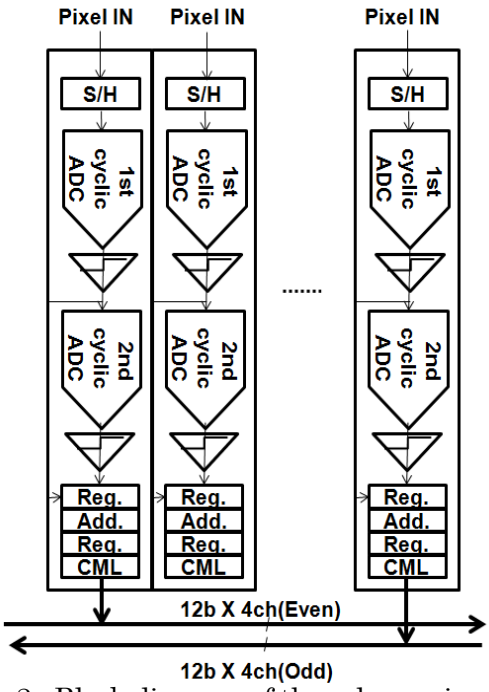

Fig. 2.. Block diagram of the column circuits.

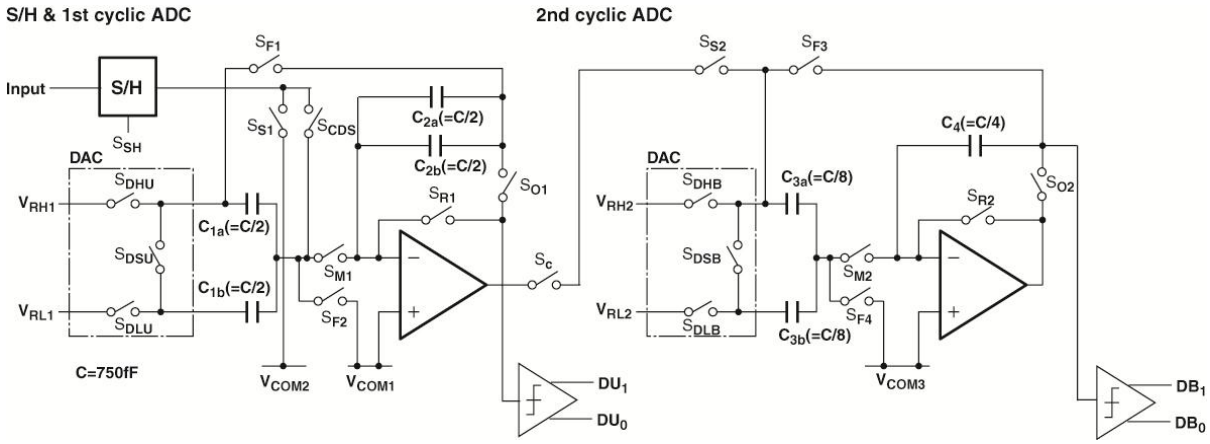

Fig. 3.. Schematic diagram of 2-stage cyclic ADC.

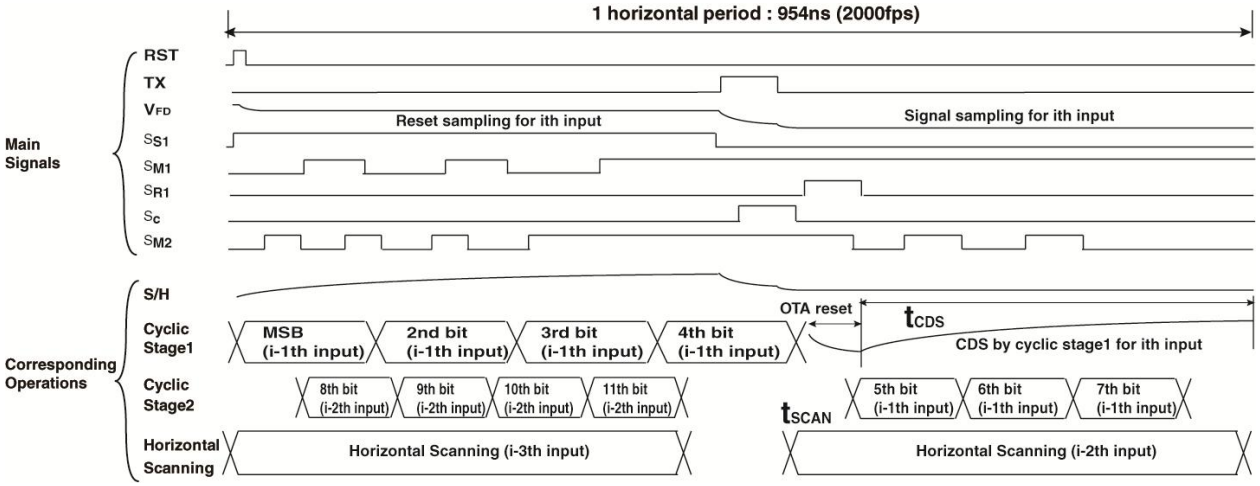

Fig. 4.. Timing diagram.

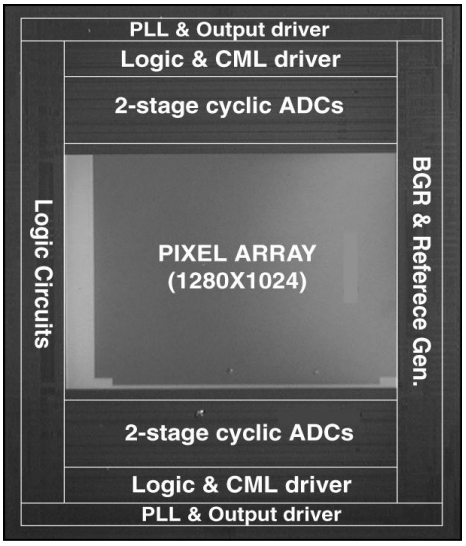

Fig. 5.. Sensor micrograph.

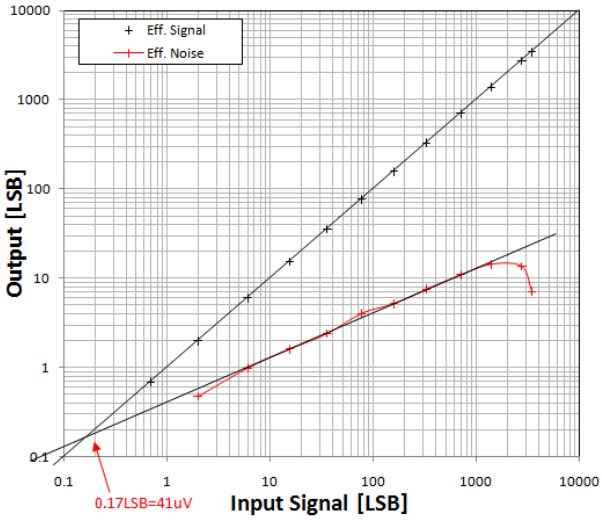

Fig. 6. Signal and noise.

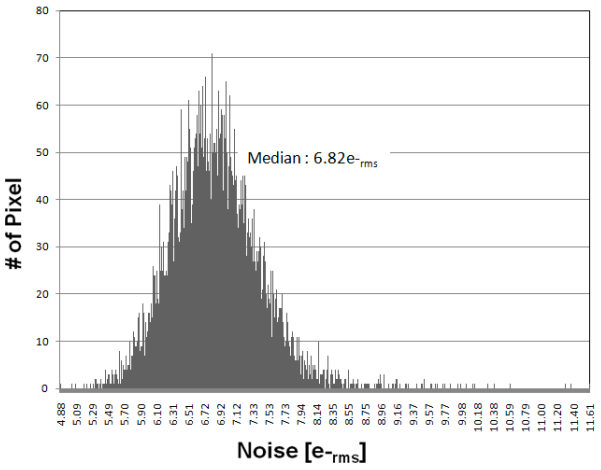

Fig. 7.. Noise histogram of 10,000 pixels at dark.

Fig. 8.. Sample image (1706fps).

Table 1. Performance Comparison.

Ref.	[2]	[3]	[4]	This work
frame rate[fps]	120	50	120	1700
# of pixels	2.1M	9M	17.7M	1.3M
noise [e-$_{rms}$]	2.4	2.9	2.75	7
Shutter type	rolling	rolling	rolling	global
Power [mW]	180	297	3000	908
ADC resolution[bit]	12.5	14	12	12
Column Gain	1	8	10	2
FoM1 *1[e-/MHz·Step]	2.8	13.1	25.9	2.0
FoM2 *2[e-· nJ]	1.8	7.0	3.9	2.9

Table 2. Parameters and performance.

Parameter	Value
Process	0.18um 1P4M
Pixel type	Global
Supply Voltage	Pixel : 3.3V, analog, digital : 1.8V
Number of effective pixel	1280(H)X1024(V)
Pixel Size	5.6μm X 5.6μm
ADC resultion	12b
Column analog gain	1X, 2X
Noise	7e-rms (x2)
Sensitivity	5.04 V/lx.s
DR	59.6 dB
Full well capacity	18000e-
SNR max	40.8dB
Q.Emax	0.67(@530nm)
ADC noise	299uVrms
Power Consumption	908mW
PRNU$_{1288}$	0.84%
DSNU	0.33mV