High speed 36 Gbps 12Mpixel global pipelined shutter CMOS image sensor with CDS

Jan Bogaerts, Koen Ruythooren, Aleksandar Gvozdenovic, Kevin Van Esbroeck, Bart Ceulemans, Werner Ogiers, Gavril Arsinte, Xinyang Wang, Guy Meynants
CMOSIS nv, Coveliersstraat 15, 2600 Antwerpen, Belgium
jan.bogaerts@cmosis.com, +32 3 260 17 36

Introduction

A broad range of industrial machine vision, movie and TV, traffic monitoring and motion control applications require true global shutter sensors with high pixel resolution. More and more applications also demand high resolution combined with high frame rates [1][2]. In this paper we present the development of a high speed 12Mpixel global shutter CMOS image sensor manufactured in TowerJazz 0.18 µm CIS technology. The sensor can output in full resolution approximately 300 frames/s at 10 bit resolution, resulting in a data throughput of more than 36 Gbps. First sensor prototypes are currently being characterized. We describe its unique features and report on the measured specifications.

Sensor and pixel architecture

The image sensor architecture is shown in Figure 1. The pixel array measures 4096 by 3072 pixels at 5.5 µm pitch. One of the unique features of the sensor is the 8-transistor pixel structure, which combines pipelined global shutter operation with CDS [3]. Figure 2 shows the pixel architecture and operation. During the Frame Overhead Time (FOT, global shutter operation), the reset voltage of FD is first sampled for all pixels simultaneously on pixel capacitor C_2. Charges from the pixels are then transferred from PPD to FD and the value is sampled on capacitor C_1. This ends the global sampling operation and the next exposure period can start. Meanwhile, the memorized frame is read out row by row (see Row Overhead Time ROT) by first reading the reset value from C_2 capacitors. The sample_2 switch is then used to obtain charge sharing between the two in-pixel capacitors. Subtraction of both signals in the readout path cancels the pixel kTC reset noise and offset non-uniformity.

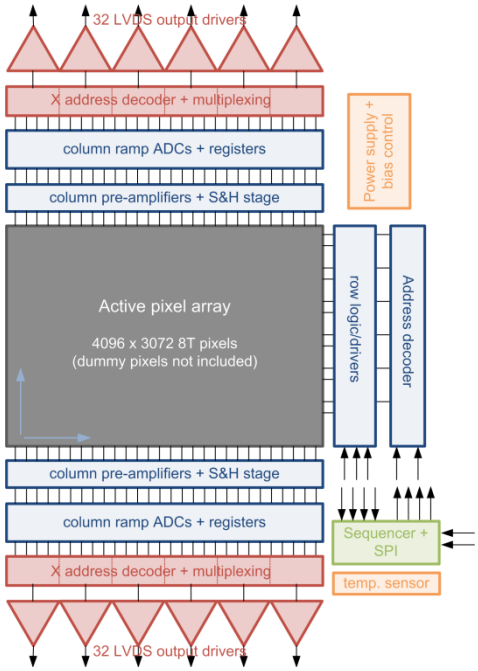

Figure 1. Image sensor architecture

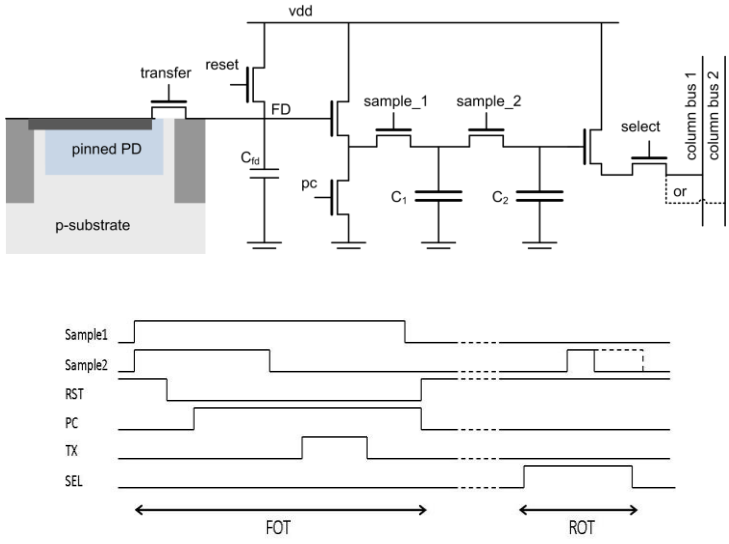

Figure 2. Pixel architecture and operation

Compared to 5T pixels commonly used in the industry for global shutter sensors, this pixel has significant advantages:

- The read noise of this pixel is drastically reduced since the reset noise of the FD is cancelled. The noise of the pixel is mainly determined by the size of the two in-pixel capacitors that are used to store both the reset and the signal level. A noise of less than 10 electrons has been measured. Due to the CDS operation conversion gain and dynamic range are no longer linked and the pixel can be optimized for high sensitivity – as required for many high speed machine vision applications – without sacrificing the dynamic range. The pixel has a linear dynamic range of more than 62 dB.

- Excellent shutter efficiency is another important advantage of this pixel architecture. The shutter efficiency is measured to be better than 99.999 %. This is obtained by the low light sensitivity of the gate capacitor, the differential readout operation of the pixel, and by the large capacitance ratio between the FD and storage capacitors. Even for backside illumination, this pixel architecture exhibits very good shutter efficiency [4].
- Reset and photo-induced signal levels are both sampled globally, simultaneously for the pixels and shortly in time after each other. This results in optimal elimination of power supply noise and RC delay effects and therefore excellent pixel uniformity.

The main pixel characteristics are summarized in Table 1.

Table 1. Pixel performance summary

Specification	Value
Pixel pitch	5.5 µm
Full Well charge	> 13 Ke-
Dark read noise	< 10 e-
FD conversion gain	~ 100 µV/e-
Dynamic range	> 62 dB
Parasitic light sensitivity	< 1/100000
Dark current	350 e-/s (@ room temp)
Peak QE	50 % (with micro lens)

ADC architecture

Another novel feature is the implemented ADC architecture. A single slope ramp column ADC is used. During the readout of a pixel row, the column amplifier with programmable gain performs a first CDS operation on the reset and signal values of the pixels. Both the amplifier reference value and the pixel corrected signal are sampled in the S&H stage but with a fixed offset. High speed A-to-D conversion is achieved through a fast ramp in combination with a high speed clock. The ADC architecture is shown schematically in Figure 3.

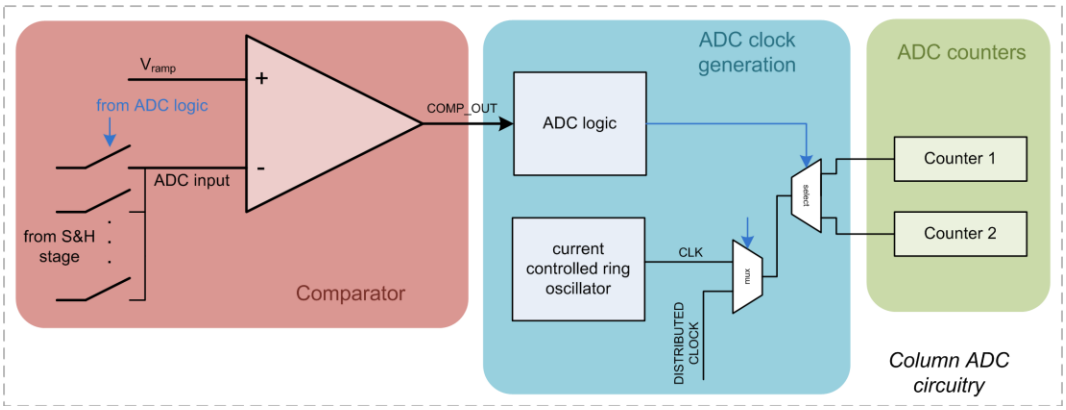

Figure 3. ADC architecture

Each column contains two counters. The clock for these counters is either a locally generated high speed clock or a high speed clock distributed over all columns. The frequency of the local clock can be controlled through SPI and is in the range of 0.8-1.5 GHz. The distributed clock is the LVDS clock running nominally at 300 MHz. The ADC logic that controls the counters enable signals is a small state machine that toggles between four states. This operation principle is illustrated in Figure 4. During a single ramp cycle, the ramp voltage is compared to four signals, respectively a fist reference voltage, the reset voltage, the signal voltage and finally a second reference voltage. As shown in the figure, the first counter is enabled during states s2 and s4 (resulting counter value C1), while the second counter is enabled during s3 (resulting counter value C2). During readout, the two counter values are multiplexed to the output where the final digital value is calculated as the ratio between C2 and C2+C1. C2 depends on the light induced pixel value. The sum C1+C2 depends only on the ramp signal, the clock frequency and the fixed voltage difference of the reference signals. Therefore, the non-uniformity in frequencies of the local clocks as well as temperature and process variations in ramp

signal are eliminated in the final signal. Column amplifier and comparator offsets are cancelled as well (second digital CDS operation). The ADC resolution can be varied almost continuously by programming the ramp slope. We believe that this single slope ADC with locally generated clock provides an excellent architecture for high resolution and high speed sensors. The local clock enables high speed counting without the need for power hungry high speed clock distribution and without the associated clock signal degradation. The ADC architecture is mainly digital in nature and requires only power supply voltages compatible with large analog signals in the comparator. The comparator itself can be simple in design because of relaxed requirements in terms of speed and offset. Because of its digital nature, the architecture allows for smaller area and power consumption for more advanced CIS processes and lower power supply voltages. It is therefore also insensitive to noise introduced by conversion in neighbouring columns or through the power supply and voltage drops in large scale high speed image sensors. Note that the power consumption is kept quasi constant during the complete conversion cycle.

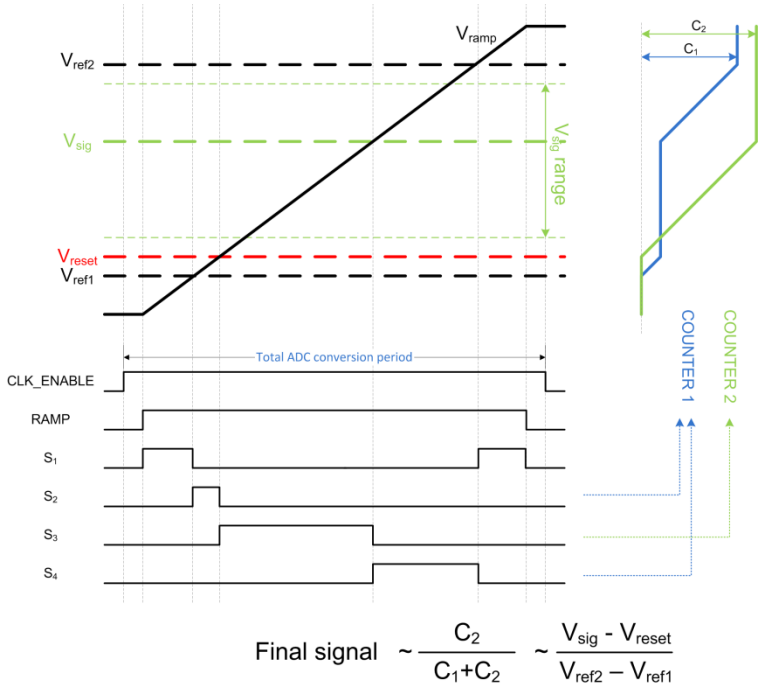

Figure 4. ADC operation principle

Sensor readout, features and performance

Besides the pixel integration and pixel readout, also the readout process itself happens in a pipelined manner as shown in Figure 5. The three processes (pixel access and sampling, A-to-D conversion and data readout) happen in parallel. The slowest process limits the line frequency and frame rate. The total sensor output bandwidth is close to 38 Gbps. This is achieved through 64 LVDS channels running at 600 Mbps. For applications that do not require the high frame rates, the data can be multiplexed to 32, 16, 8, 4, 2 or 1 output(s) with respective reductions in frame rate.

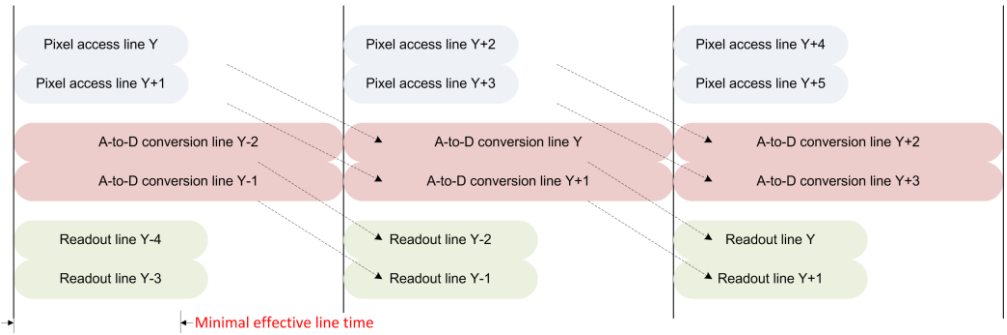

Figure 5. Readout pipeline architecture

The sensor is able to operate in full resolution at 300 fps (10 bits ADC) and 180 fps (12 bits ADC). The sensor also supports windowing, sub-sampling and 2 by 2 pixel binning in monochrome and colour devices. Two output lines per pixel pitch with top/bottom readout allow for windowed readout anywhere in the pixel array. For example, a binned HD format window can be read out at 500 fps (12 bits ADC) and a sub-sampled HD format window at 1000 fps. The main sensor features are summarized in Table 2. A picture of the sensor in its ceramic package is shown in Figure 6.

Figure 7 shows a test chart image taken with the new image sensor at 10 bit full pixel resolution with a magnified part in the inset. In this case, the sensor was operated internally at maximum speed (corresponding to 300 fps), but with data multiplexed to 4 outputs because of test system limitations.

Acknowledgements

The development of the sensor was performed in the framework of the recent EUREKA programme CATRENE (Cluster for Application and Technology Research in Europe on NanoElectronics) and was supported by IWT (Flemish government agency for Innovation by Science and Technology).

References

[1] T. Toyama et al., "A 17.7Mpixel 120 frames/s CMOS Image Sensor with 34Gbits/s readout", ISSCC2011, paper 23.11.
[2] "Sony Announces Next Generation Cinealta Camera with New 8K Cmos Image Sensor", http://www.dcinematoday.com/dc/pr.aspx?newsID=2291, April 2011.
[3] X. Wang, et al, "A 2.2M CMOS Image Sensor for High Speed Machine Vision Applications", proc. SPIE vol.7536, San Jose, Jan. 2010
[4] G. Meynants, et al, "Backside illuminated global shutter CMOS image sensors", IISW 2011.

Table 2. Overview of sensor features

Feature			
Resolution	4096 x 3072		
Pixel size	5.5 um x 5.5 um		
Max. frame rate	180 fps (12 bit)	300 fps (10 bit)	350 fps (8 bit)
Pixel control	Row windowing (up to 32 separate ROIs), sub-sampling, 2x2 binning		
Image flipping	X and Y mirroring		
Output	64 LVDS outputs @ 600 Mbps		
Multiplexing	To 32, 16, 8, 4 and 2 or 1 output(s)		
ADC output	8 bit, 10 bit, 12 bit		
Package	Ceramic µPGA package (237 pins)		
Power consumption	< 3 W (full frame, 300 fps, 10 bit)		

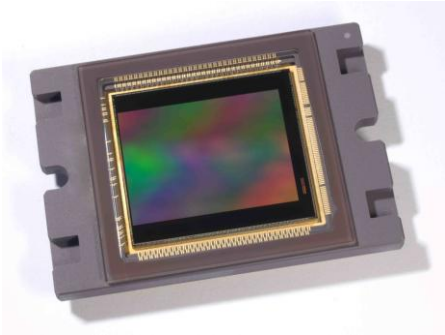

Figure 6. Sensor in ceramic µPGA package

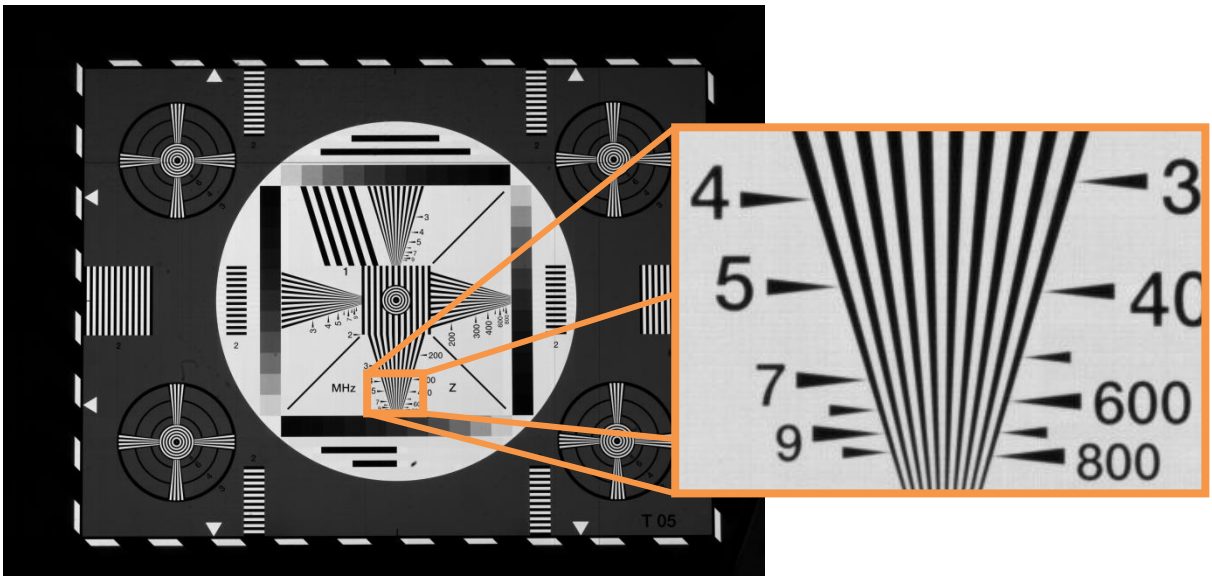

Figure 7. Test chart image taken with new 12 Mpixel image sensor