R57 Progress of Ultra-high-speed Image Sensors with In-situ CCD Storage

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Abstract
This paper reviews progress of technologies on ultra-high-speed image sensors with in-situ CCD signal storage, which was named ISIS, the in-situ storage image sensor. First, the history is summarized. It begins with Kosonosky's sophisticated burst image sensor with SPS-CCD storage. Then, the simplest slanted linear CCD storage was invented by Etoh and Mutoh, which has developed application fields of high-speed imaging at 10 kfps to 1 Mfps. Recently, their backside-illuminated version achieved 16 Mfps with very high sensitivity. On the other hand, a CMOS burst image sensor was developed by Sugawa et al, which achieved 20Mfps. Progress expected in the near future is also presented.

Keywords: ISIS, Burst image sensor, Backside illuminated, CCM, Ultra-high speed, High sensitivity

1. Historical review

1.1 Pixel-based image signal storage

It is a classic idea to achieve ultra-fast motion imaging by installing plural of memory elements in each pixel for simultaneous parallel recording at all pixels. A set of more than one hundred frames replays a motion picture at ten fps for more than ten seconds, which is necessary and sufficient to activate dynamic recognition of scientists and engineers. They can discover phenomena embedded in the motion picture which are difficult to be recognized from a posted series of still images. Table 1 shows image sensors with the pixel-based image storage utilizing CCDs as the memory elements. One recent achievement with CMOS capacitor storage by Sugawa et al is also included [5-6].

The first successful achievement by Kosonocky et al was an image sensor with SPS-CCD storage, as shown in Fig. 6 [1]. However, it was difficult to manufacture the CCD structure with an in-pixel acute direction change from a horizontal series CCD to vertical parallel CCDs by the CCD process technology at that time. Therefore, the major performance indices were all a little lower than the levels required in practice. For example, if the top electrodes of the vertical CCDs are made with the polysilicon layer 1, those of the horizontal CCD have to be made with other polysilicon layers. Therefore, they used a dedicated four-polisilicon layer CCD process developed for this application. The metal wiring was also complicated.

Lazovsky et al achieved 100 Mfps [3]. However, the other indices were far less than practical requirements.

1.2 ISIS with slanted linearly CCD

In 2001, the first practical image sensor with pixel-based CCD storage was developed by the authors and named "ISIS-V2", the in-situ storage image sensor version two [2]. As shown in Fig. 1, the in-situ CCD memory of the sensor linearly extends downward over about ten pixels in a slightly slanted direction to the CCD grid. The senor achieved one million fps. NHK jointly developed the color version, ISIS-V4, with us [4].

1.3 BSI-ISIS

In 2011, the BSI, backside illuminated, ISIS-V16 achieved 16 Mfps [7]. The backside illumination together with CCM (EM-CCD) and cooling, ISIS-V16 achieved very high sensitivity in addition to the ultra-high speed.

Table 1 Ultra-high-speed imagers with pixel-based storage

	Frame rate (Mfps)	Pixel count	No. of frames	FSI	BSI	Image type	Fill factor (%)	Year	Ref.	Type
SPS-CCD	0.5*	32,400*	30	X		Mono.	13.5	1996	[1]	CCD
ISIS-V2+	1	81,120	103	X		Mono.	13	2002	[2]	CCD
Dalsa CCD	100	4,096	16	X		Mono.	1	2005	[3]	CCD
ISIS-V4+	1	295,200	144	X		Color	15	2006	[4]	CCD
ISIS-V16+	16	165,072	117		X	Mono.	100	2010	[7]	CCD
Sugawa CMOS	20	55,296***	104	X		Mono.	35	2010	[5-6**]	CMOS

* The paper claimed "360x360" pixels. However, due to the yield problem, practical one had "180x180" pixels.
** Press release news (in Japanese). *** Pixel count is estimated by T.G. Etoh. + Sensors developed by the authors.

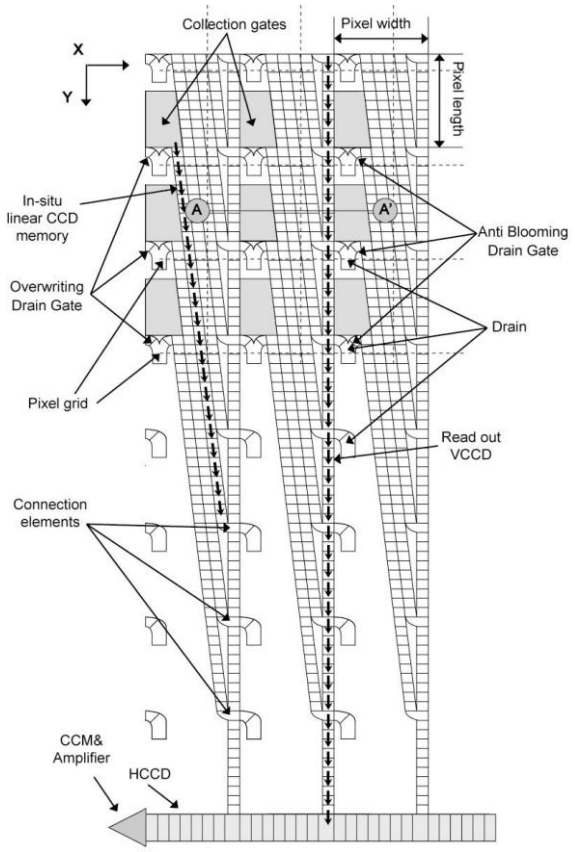

Fig. 1 Plane structure of BSI-ISIS with slanted linear in-situ CCD memories (3x3 pixels) by ISIS-V16

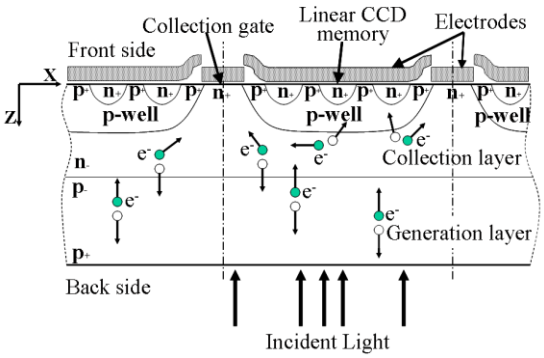

Fig. 2 A cross section of BSI-ISIS (cross section A-A' of Fig. 1)

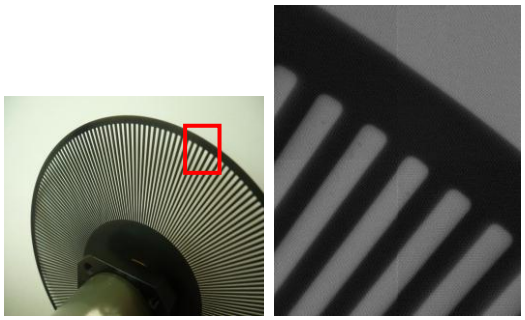

Fig. 3 A laser beam chopper image taken at 16Mfps

The BSI structure increases not only sensitivity with 100% fill factor and high quantum efficiency, but also frame rate with inner metal bus lines densely placed on the front surface of the sensor without reduction of the fill factor and non-uniformity of the pixel structure. The charge handling capacity Q_{max} is 16,000 e- at 8 Mfps. The noise level is independent of the frame rate. Therefore, reasonable dynamic range is guaranteed even at a very high frame rate. Fig. 3 shows an image example taken at 16 Mfps. Modification of the sensor is currently going on for higher frame rate and less noise for practical applications.

1.4 FBI imagers

The chip has a thickness of 33 um, consisting of a 10-um thick n-epi layer and a 23-um thick p-epi layer. In the n-epi layer on the front side, n-type CCD memories are installed, which are protected by the p-wells. This configuration provides the following advantageous functions:

(1) To prevent incident photons from directly reaching the memory CCD to generate additional electrons
(2) To prevent signal electrons generated in the generation layer from migrating to the memory CCD
(3) To deplete the layers all the way along the path of the signal electron

The special cross section configuration serves to create functional BSI imagers by replacing multi-memory elements of each pixel in the p-well by functional circuitry. Hereafter, the image sensor group is called FBI, functional backside-illuminated, image sensors.

2. Example of FBI imagers

2.1 ISAS: Image Signal Accumulation Sensor

An example of FBI imagers is presented. A new function, image signal accumulation, was introduced to the sensor concept in response to a requirement from scientists in the field of pulse neutron radiography. As shown in Fig. 4, in each pixel of the sensor, a folded and looped CCD is installed as in-situ storage. The sensor was named image signal accumulation sensor, ISAS. Since the last element of the memory CCD is connected to the first element, image signals captured in the second experiment trial are automatically added to those captured and stored in the first trial, and, then, transferred in the memory CCD during the second trial. The image accumulation is very useful in scientific research with image capturing of reproducible events with very low light emission, such as fluorescence imaging of brain signal transfer.

To the backside with the fill factor 100%, other electro-magnetic waves than visible ray and charged particles can be applied to FBI imagers, which provides very useful scientific instruments such as imaging TOF MS.

2.2 Hybrid CMOS/CCD ISAS

The Z-shaped electrode, as shown in Fig. 5, was invented to fold a CCD. The CCD with the electrodes can be manufactured by an advanced CIS process with a single polysilicon layer with the space less than 0.2 um.

The CMOS-based CCD technology provides further high functionality, parallel and partial readout, which is utilized in conventional high-speed image sensors. A pixel of the hybrid CMOS/CCD ISAS comprises of a low-noise CCD memory and flexible high-speed CMOS readout circuit. The sensor satisfies most features required from high-speed imaging in advanced science and engineering. The technical feasibility has been confirmed by extensive simulation studies.

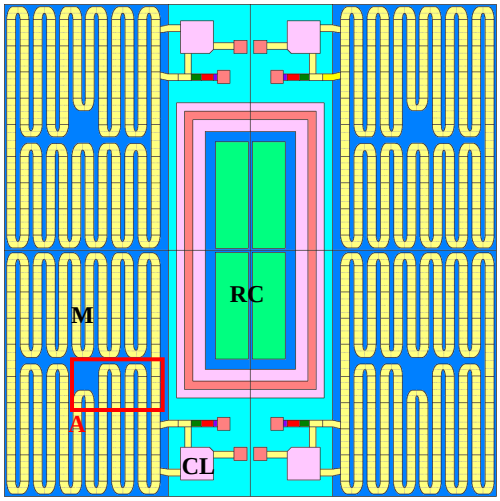

Fig. 4 Hybrid CMOS/CCD ISAS (2x2 pixels):
M: Memory CCD; CL: Collection gate;
RC: CMOS readout circuit

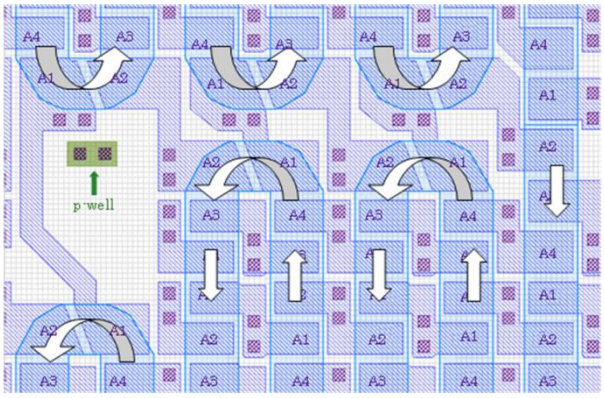

Fig. 5 Z-shaped electrodes to fold a CCD for signal accumulation (enlargement of area A of Fig. 4)

3. CMOS-based ISISes

3.1 Previous trials

The concept of in-situ storage has been implemented in both CCD and CMOS imagers. In the past, though many CMOS-based ISISes were experimentally designed and fabricated, none of them could have yielded successful products for practical applications. The main reason lies in the working principles of CMOS image sensors: an image signal from a photodiode is amplified in-pixel. Therefore, output signal is much larger than the original one, which requires a much larger memory size of the in-situ storage.

3.2 Sugawa's solution

Sugawa et al [5-6], successfully solved the problem by employing a special analog storage technique, a stacked capacitor comprising of a Poly-Si - insulator - Poly-Si (PIP) capacitor and a traditional MOS capacitor. Since the insulation of a PIP capacitor is a very thin dielectric layer on the first poly-Si electrode, which provides very large capacitance. Therefore, the size of one memory element is greatly reduced and a sufficiently large number of storage elements can be installed.

One of the main advantages of this implementation is very high light shield performance, since the storage area is separated from the photo-receptive area and placed in the peripheral light-shielded area of the chip. CMOS switching and multi-parallel signal transfer wires on each pixel column made the separation possible.

Another advantage is low power consumption. Even non-cooling imaging is possible.

4. Heat Generation in CCD-ISIS

4.1 Counter-measures

In ultra-high-speed imaging, power consumption of the image sensor is not as crucial as that in mobile devices. A typical ultra-high-speed imaging system not only requires a special camera, but also a very powerful illumination tool of more than 1KW.

A major problem is heat generation during continuous overwriting operation at ultra-high-speed. A counter-measure is to minimize the duration in which the ultra-high-speed recording operation continues. For example, when capturing images of natural raindrops, we use a strong back-light illumination. To avoid heat-up of the camera, we use a double-trigger method to minimize the duration of the illumination: one laser trigger is set just before the field of vision to start the illumination and the other one is within the field of vision to stop it and the overwriting recording. We can minimize the ultra-fast operation of the sensor by synchronizing the sensor operation with the illumination operation. At first, we operate the sensor at a lower frame rate, accelerate the frame rate instantly at the first trigger signal, and stop at the second one. Therefore, we named the first trigger "Acceleration Trigger", and the second one "Stop Trigger".

Another problem is generation of the dark current noise during readout after cease of overwriting recording operation. The ISIS-V16 has four readout taps. Conventional high-speed image sensors have many readout channels for high-speed parallel readout. For the CCD-ISISes, it is also easy to install many readout taps to reduce the readout time.

4.2. Revival of Kosonocky's SPS-CCD

One promising candidate to reduce power consumption of CCD storage is employment of the Kosonocky's SPS-CCD storage. Our target is to develop an in-situ memory with more than 100 elements. If we make it with the SPS-CCD, we need a memory array of 10 rows and 10 columns within each pixel. During the horizontal series CCD operation, one tenth of the CCD elements work. After every 10 operations of the series CCD electrodes, the parallel CCD electrodes are operated to transfer signal charges stored in the series CCD to the parallel CCDs. Therefore, the working time of the parallel CCDs is one tenth of that of the series one. With the same pixel size, power consumption of the chip is about one-fifth of that of the ISIS with linearly slanted CCD memories. The higher the number of frames is, the lower the power consumption will be.

One disadvantage is that the direction change makes the frame rate a half.

Currently, by using advanced CMOS process, it is possible to fabricate a CCD with a poly gap spacing of 0.20 um or less. With such a small gap, potentials from the adjacent electrodes overlap, which leads to a sufficiently high charge transfer efficiency. The fine metal wiring also serves to make double contacts to small isolated electrodes of the series CCDs to avoid missing contacts.

Advance of deep sub-micron VLSI processes has revived the Kosonocky's SPS-CCD memory.

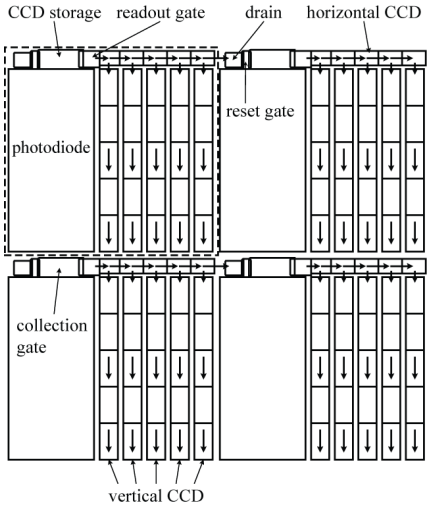

Fig. 6 ISIS with SPS-CCD storage [1]

5. Concluding remarks

Progress of high-speed image sensors with pixel-based signal storage is reviewed.

The FBI, functional backside illumination, structure was created to safely install functional circuitry within a pixel by preventing incident light from direct intrusion to and generated signal electrons from migrating into the storage. The FBI structure together with the slanted linear CCD in-situ storage achieved an image capturing at 16 Mfps for a 165 kpixel format with very high sensitivity.

Another example, the ultra-high-speed ISAS, image signal accumulation sensor, was designed for imaging of reproducible high-speed events with very low-light emission. The design employed a hybrid CMOS/CCD structure with low-noise CCD storage and fast and flexible CMOS readout circuitry.

Sugawa et al developed a practical ultra-fast image sensor by CMOS technology at the first time in the world with a capacitor array with a special structure for pixel based storage, which is placed on the periphery of the chip, separated from the photo-receptive area. The structure is not competitive with the FBI structure. Installation of their capacitor array on the front side of the FBI structure makes all the major performance indices of their sensor, such as the maximum frame rate, the pixel count and the sensitivity, doubled.

Ten years ago, the slanted linear CCD storage was superior to Kosonocky's SPS-CCD storage. However, for the target frame rate of more than 10 Mfps and for the design rule of the CIS process with technology node 0.14 um, the SPS-CCD will be revived, since heat generation of the SPS-CCD is less than 1/5 of that of the slanted linear CCD.

Reference

[1] Kosonocky, W., et al 360 × 360-Element Very High Burst-Frame Rate Image Sensor. In *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*, 1996; pp. 182-183.

[2] Etoh, T.G., etal., A CCD Image Sensor of 1M frames/s for Continuous Image Capturing of 103 Frames. In *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*, 2002; pp. 46-47.

[3] Lazovsky, L., et al, CCD Sensor and Camera for 100 Mfps Burst Frame Rate Image Capture. In *Proceedings of Airborne Intelligence, Surveillance, Reconnaissance (ISR) Systems and Applications II*, 2005; pp. 184-190.

[4] Ohtake, H., et al, 300,000-Pixel Ultra-High-Speed High-Sensitivity CCD and a Single-Chip Color Video Camera Mounting This CCD. *Broadcast Technol. NHK STRL* **2006**, *28*, 2-9.

[5] Tochigi, Y., et al, A prototype high-speed CMOS image sensor with 10,000,000 fps burst-frame rate and 10,000 fps continuous-frame rate. In *Proceedings of SPIE-IS&T*, Vol. 7876, 2011, pp. 78760G-1-8.

[6] URL: http://www.itmedia.co.jp/news/articles/1104/06/news030.html

[7] Etoh, T.G., et al, 16Mfps 165kpixels Backside-illuminated CCD. In *IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers*, 2011; pp. 406-407.