A Common Gate Pinned Photodiode Pixel

Yannick De Wit, Manuel Innocent

On Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
Yannick.DeWit@Onsemi.com tel +3215 448773, fax +32 15 448

***Abstract* -- This paper presents a new pixel architecture improving the performance of conventional 4T pixels. Functionally the pixel consists of 4 transistors where the gates of the reset and transfer transistors are physically shortened. In this common gate 4T pixel, dedicated voltage levels on the common gate allows charge to be transferred to the floating diffusion without resetting the floating diffusion. The floating diffusion can be surrounded by this common poly-silicon gate which will reduce leakage of the floating diffusion, improving parasitic light sensitivity and providing intrinsic tolerance to radiation, enabling space applications. Furthermore, due to the fact that both transfer and reset are shared, the pixel operates with one signal line less compared to conventional 4T pixels. This allows smaller pixels with possibly better yield.**

1. Introduction

Today, CMOS image sensors most commonly use 4T pinned photodiode pixel architectures (Figure 1). These pixels have superior performance compared to 3T based pixel architectures in regard to noise, dark current, linearity and conversion gain. The 4T pinned photodiode pixel also allows global shutter operation without additional sample and hold stages.

However, for the global shutter applications, these pixels lack in terms of pixel storage node leakage (PSNL) and shutter efficiency, also quantified by parasitic light sensitivity (PLS) compared to pixels with a buffered sample and hold stage (Figure 2).

The proposed common gate 4T pixel will enable the manufacturing of smaller pixels compared to conventional 4T pixels. Furthermore it will provide the possibility to layout the pixels in such a way that they possess significant improvements in regard to PSNL, PLS, and radiation tolerance.

2. A Common Gate 4T Pixel

Figure 3 presents a layout of the new common gate 4T pixel architecture. As can be seen, the gates of the transfer transistor and reset transistor are shortened, in other words: they have a common gate. As with conventional 4T pixels, the transfer transistor is located between the photodiode (source of the transfer transistor) and the floating diffusion (drain of the transfer transistor) while the reset transistor is between the floating diffusion (source of the reset transistor) and the pixel power supply Vpix (drain of the reset transistor).

The common gate pixel as such has the advantage that it can operate with one signal line less compared to traditional 4T pixels. This enables making significantly smaller pixels. Also, due to this, yield can be improved because in conventional 4T pixels, a short between the reset and transfer line will result in a black row.

Further performance improvements can be expected when the common gate is constructed with a ring layout (Figure 4). The ring layout of the common gate has the consequence that the floating diffusion has no interface with STI. This will reduce surface generated dark current at the floating diffusion (PSNL) and makes the pixel suitable for environments with large levels of radiation [Inno 09]. This ring common gate layout has the additional advantage that PLS is reduced [Lep 07].

This paper will focus on the theory of operation as well as presenting the measurements in rolling and snapshot shutter mode of operation for the common gate pixel architecture similar to the one presented in figure 3. The common gate pixel with ring layout is part of our on going investigation.

3. Principle of operation

At first sight it seems like this pixel architecture can't work due to the fact that when you apply a voltage to the common gate to transfer the charge, the photodiode will be reset via the floating diffusion resulting in a black row. However, due to the fact that the source of the reset and transfer gate are not on the same node, it can work when different dedicated voltages on the common gate are used separately for the reset and transfer cycle.

During reset of the photodiode and floating diffusion, a high voltage is applied at the common gate (Vcg) so that both are reset (hard reset for floating diffusion), this happens when:

$$Vcg_{reset\_fd} \geq Vpix + Vt_{reset} \quad \text{hard reset of floating diffusion} \tag{1}$$

$$Vcg_{reset\_pd} \geq VPIN + Vt_{transfer} \quad \text{reset of photodiode} \tag{2}$$

With:

Vpix: Pixel high power supply, *VPIN:* Photodiode depletion voltage, Vt_{reset}*:* Threshold voltage of reset transistor, $Vt_{transfer}$*:* Threshold voltage of transfer transistor

After the integration period , a lower voltage is applied at the common gate which can not exceed $Vcg_{transfer\_max}$ (so as not to reset the floating diffusion) but needs to be at least equal to $Vcg_{transfer\_min}$ (to transfer all charge from photodiode to floating diffusion) as indicated below:

$$Vcg_{transfer\_min} \geq VPIN + Vt_{transfer} \quad (3)$$

$$Vcg_{transfer\_max} \leq (Vpix - \Delta reset - \Delta Vsignal) + Vt_{reset} \quad (4)$$

With: $\Delta Vsignal$ *:* Required signal swing when photodiode is saturated on the floating diffusion due to charge transfer, $\Delta reset$ *:* Voltage drop on the floating diffusion after reset due to reset clock feed-through.

The reset transistor will not conduct as long as its gate-source voltage (Vgs_{reset}) is significantly lower than its threshold voltage (Vt_{reset}). During that time, it is possible to transfer the charge from the photodiode to the floating diffusion without resetting the photodiode and/or floating diffusion. During transfer, the voltage on the floating diffusion will drop and this drop will ultimately be limited by the photodiode charge or (if the photodiode charge is sufficient) by the common gate transfer voltage according to:

$$Vfd_{min} = Vcg_{transfer\_min} - Vt_{reset} \quad (5)$$

So, to increase the possible full well charge that can be read out, the voltage on the common gate during transfer should be as low as possible. The consequence is that the depletion voltage of the photodiode (VPIN) should also be as low as possible, just enough to provide the required full well charge that can be read out.

4. Measurements: rolling shutter

All measurements are done on a 6.1um square common gate pixel with a similar layout to what is shown in figure 3. The pixel is processed with a VPIN of 1.2V in a commercial 0.18um image sensor technology.

Figure 5 presents the rolling shutter timing for the common gate pixel. As can be seen, correlated double sampling is achieved. However, compared to traditional 4T pixel timing, the sampled reset value of the pixel will be on the floating diffusion during the entire integration period. This has the consequence that for high illuminations, the photodiode charge will spill over to the floating diffusion (blooming) which degrades the reset value. Also parasitic light sensitivity and dark leakage on the floating diffusion will degrade the reset value.

The response measurement in Figure 6 shows the expected result for different common gate voltages during the transfer phase. The swing is reduced for higher common gate transfer voltages due to reset clipping as forecasted in Equation (5).

The reverse saturation slope due to blooming is also observed. This reverse saturation slope should not be a problem as it can easily be detected by an algorithm or solved by a clipping circuit inside the sensor. However, it can also be reduced significantly by adding a reset transistor on the photodiode to serve as an anti-bloom transistor. As seen in Figure 7, this reduces the reverse saturation slope significantly. The remaining reverse saturation slope observed is mainly due to PLS and PSNL.

The dark temporal noise measured for all used common gate transfer voltages is less than 360uV.

The image lag measurements for the different transfer voltages are presented in Figure 8. Image lag is lower than 0.15% and not significantly different compared to a traditional 4T pixel. We see a slightly higher image lag for the lowest transfer gate voltage due to incomplete transfer.

An overview of the results for rolling shutter mode of operation are presented in Table 1. We note that the chosen VPIN for the test vehicle containing this common gate pixel was not optimized, a lower VPIN will enable us to increase the readout swing significantly, this is part of our ongoing investigation in regard to the development of the common gate pixel.

5. Measurements: snapshot shutter

Figure 9 presents the snapshot shutter timing for the common gate pixel. Similar to conventional 4T pixels, double sampling (DS) is possible and CDS is not.

Figure 10 shows the response measurement for different common gate voltages. As with the rolling shutter measurements, we observe a similar behavior, however, the reverse saturation slope is less pronounced. This is as expected because the reset value is sampled right after resetting the floating diffusion. The blooming occurs but the time to degrade the floating diffusion value is now limited to the sampling time of the reset value whereas in the rolling shutter mode of operation, the integration time was also included. The response measurements with anti blooming shows no reverse saturation whatsoever as illustrated in Figure 11.

The image lag measurements are shown in Figure 12 and show no significant differences compared to similar conventional 5T pixels.

An overview of the results for snapshot shutter mode of operation are presented in Table 2. Parasitic light

sensitivity and dark leakage of the floating diffusion has not yet investigated as the currently measured common gate pixel does not have the ring layout as is shown in Figure 4 and consequently no improvement is expected on those parameters compared to a normal 4T pixel.

6. Conclusion

A common gate 4T pixel architecture is developed at ON Semiconductor which enables making smaller 4T pixels with possible better yield. The proof of concept for this novel pixel architecture is shown and measurements are in excellent agreement with the theoretical analysis.

The common gate pixel architecture allows using a ring gate around the floating diffusion which is expected to yield in significant performance improvements on PSNL, radiation tolerance, and PLS.

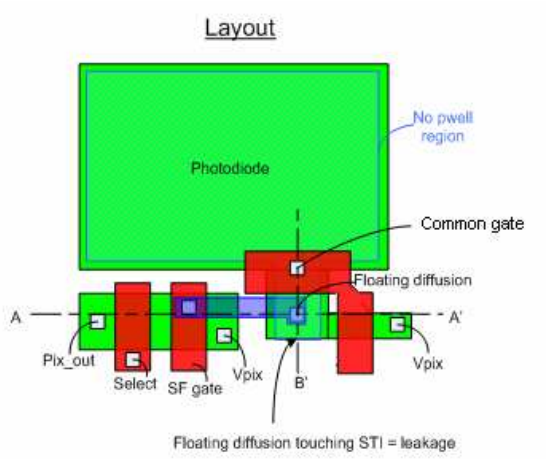

Figure 3: **Simplified layout example of top view for common gate pixel**

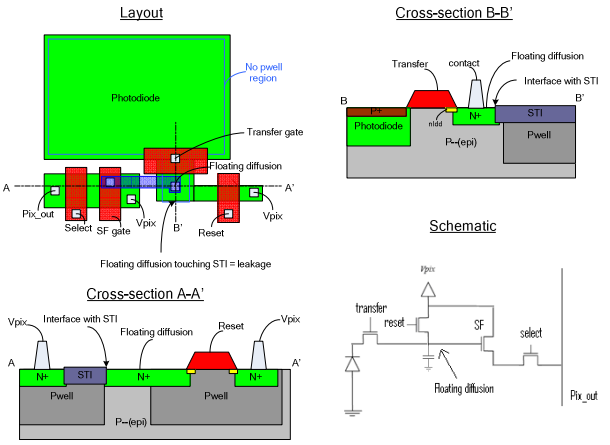

Figure 1: **Simplified layout example, cross-section and schematic of a traditional 4T pixel**

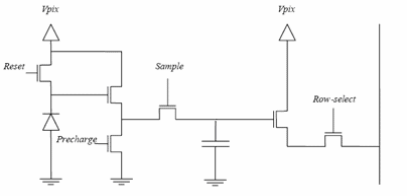

Figure 2: **Schematic example of a pixel with buffered sample and hold stage.**

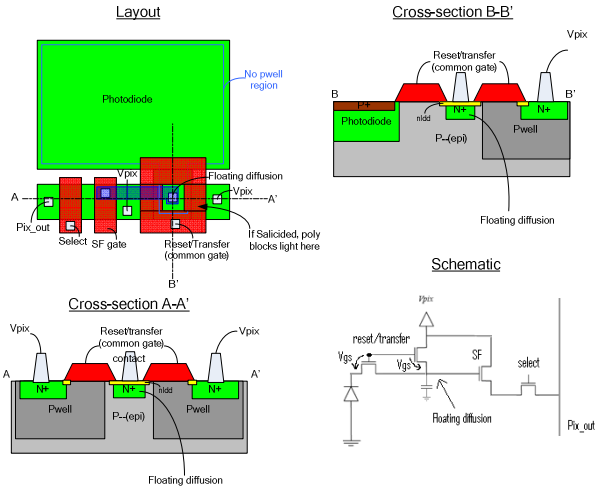

Figure 4: **Simplified layout example, cross-section and schematic of a common gate 4T pixel with optimized layout for improved performance**

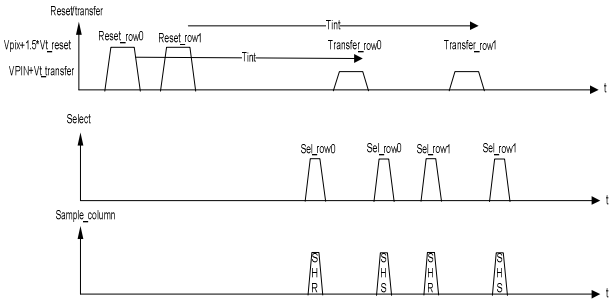

Figure 5: **Timing for rolling shutter mode of operation for the common gate pixel**

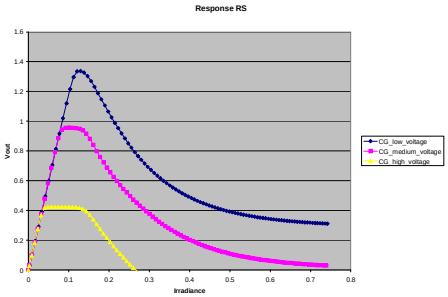

Figure 6: **Response measurements for different common gate transfer voltages in rolling shutter mode of operation without anti-blooming**

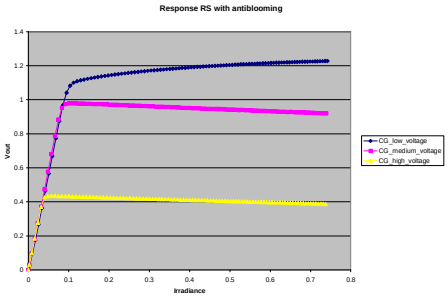

Figure 7: **Response measurements for different common gate transfer voltages in rolling shutter mode of operation with anti-blooming**

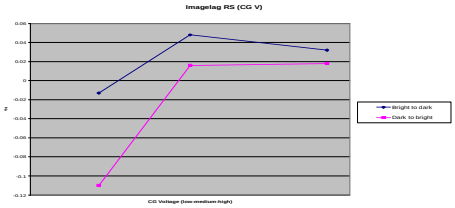

Figure 8: **Image lag measurements for rolling shutter mode of operation for different common gate transfer voltages**

CG V	*FD cap(fF)*	*Swing (V)*	*Noise (uV)*	*PRNU (%)*	*IL Bright to dark*	*IL Dark to bright*
Low	**2.75**	**1.09**	**<360**	**< 0.8**	**-0.013**	**-0.11**
Medium	**2.75**	**0.97**	**<360**	**<0.8**	**0.048**	**0.016**
High	**2.75**	**0.43**	**<360**	**<0.8**	**0.032**	**0.01**

Table 1: **Rolling shutter results for the common gate**

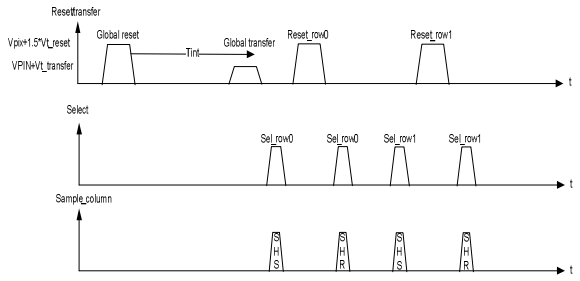

Figure 9: **Timing for snapshot shutter mode of operation for the common gate pixel**

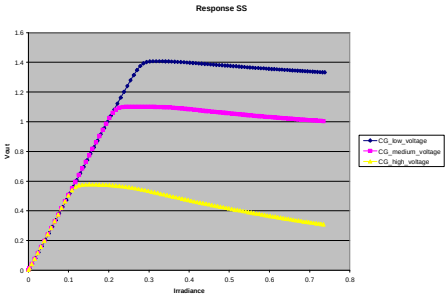

Figure 10: **Response measurements for different common gate transfer voltages in snapshot shutter mode of operation without anti-blooming**

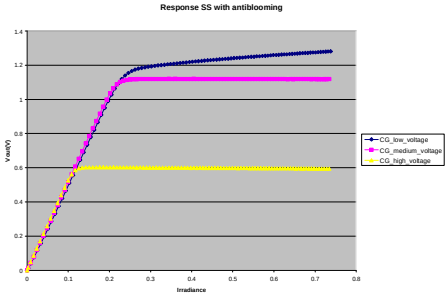

Figure 11: **Response measurements for different common gate transfer voltages in snapshot mode of operation with anti-blooming**

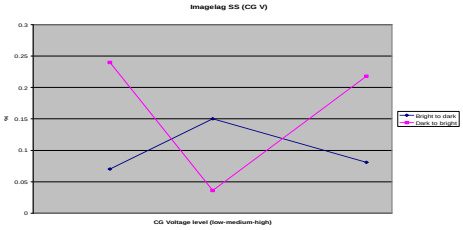

Figure 12: **Image lag measurements for snapshot shutter mode of operation for different common gate transfer voltages**

CG V	*FD cap(fF)*	*Swing (V)*	*PRNU (%)*	*IL Bright to dark*	*IL Dark to bright*
Low	**2.75**	**1.26**	**<0.8**	**0.07**	**0.24**
Medium	**2.75**	**0.95**	**<0.8**	**0.15**	**0.03**
High	**2.75**	**0.43**	**<0.8**	**0.08**	**0.2**

Table 2: **Snapshot shutter results for the common gate**

References

[Lep 07] G.Lepage, A.Materne, and C.Renard, “A CMOS image sensor for Earth observation with high efficiency snapshot shutter,” *Proceedings of 2007 International Image Sensor Workshop, IISW 2007*, pp. 299-302, June 2007.

[Inno 09] M. Innocent, “A radiation tolerant 4T pixel for space applications,” Proceedings of 2009 International Image Sensor Workshop, IISW 2009, June 2009.