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Dark Current Characterization of CMOS Global Shutter Pixels Using Pinned Storage Diodes

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***Abstract*— This paper describes dark current characterization of two-stage charge transfer pixels, which enable a global shuttering and kTC noise canceling. The proposed pixel uses pinned diode structures for the photodiode(PD) as well as the storage diode(SD), thereby a very low dark current can be expected. The measured dark current of the PD and SD with the negative gate bias results in 19.5 e-/s and 7.3 e-/s (totally 26.8 e-/s) at ambient temperature of 25°C(the chip temperature is approximately 30°C). This value is much smaller than that of conventional global shutter pixels, showing the effectiveness of the pinned storage diode.**

I. Introduction

Recently, kTC-noise-free global shutter(GS) pixels [1]–[4] have been developed, and the noise performance of GS-type CMOS imagers are greatly improved. Taking advantage of such a low noise performance requires low dark current less than 100e-/s in order to keep the noise floor from the shot noise of dark current [5]. However, no CMOS GS pixels which can satisfy low dark current characteristic have been reported.

5T-GS pixels [1], [6] suffer from high dark current at a charge storage node due to the use of a floating diffusion as an analog memory. In the 8T pixel [2], in-pixel sampling capacitor should be small to maintain a high fill factor, causing relatively high leakage. The two-stage charge transfer pixels [3], [4] using a pinned storage diode have demonstrated its low-noise performance and a high shutter efficiency. Though the pixel structure is suitable for reduced dark current, the measured dark current is still higher than rolling shutter CISs.

This paper describes dark current characterization of the two-stage charge transfer pixels using pinned storage diodes under negative gate bias conditions for charge transfer gates. The negative gate biasing [7]–[10] is a well known method to suppress dark current due to Shockley-Read-Hall(SRH) surface generation process. In this paper, temperature dependence of the PD and SD dark current under negative gate biasing is also described.

II. Proposed Pixel

Fig.1 shows the proposed pixel structure, and the potential profile. Unlike in the previous design for a dual global shutter [3], the pixel is optimized for single global shutter and consists of six transistors and two pinned diodes: a photodiode (PD) and a storage diode (SD). The PD and SD are used for photoelectron generation and charge storage, respectively. In this pixel, kTC noise is canceled by a true CDS. The proposed pixel introduces a dual doping technique for n_1 and n_2, and stepwise potential (created by p_1 under the GS gate) in order to attain a higher charge transfer efficiency. It has an another p-type doping (p_2) beneath the n_2 layer for charge shielding. This shielding layer improves the shutter efficiency to be 99.7% at incident light wavelength of 550nm [4]. The shutter leakage is dominated by carriers which are generated at deep substrate and diffuse into the SD. Therefore, the shutter efficiency can be improved with higher concentration of p_2 doping [11].

Generally, there are three components in dark current: the generation current generated in depletion layer(depletion dark current), the generation current at Si-surface(surface dark current), and the diffusion current generated in the bulk neutral region (diffusion dark current). In the proposed pixel, both the PD and SD employ a pinned-diode structure, which can suppress surface dark current. In pinned diode structures, it is well known that edges of the transfer gates become the primary source of dark current [9], [12], [13]. The edges of PD are covered by p_1 layer, which helps to accumulate holes under the GS gate. On the other hand, the surface of the SD is not covered by p_1 layer, causing large depletion dark current. This depletion dark current can be suppressed by applying the negative gate bias technique.

III. Experimental Results

Fig.2 shows the timing diagram for measurements of the PD and SD dark currents. Only the integration time of the PD, $T_{a,PD}$, is varied from approximately 15s to 30s to measure the PD dark current. Similarly, only the integration time of the SD, $T_{a,SD}$, is varied for the measurements of SD dark current. These measurement methods allow us to measure the PD and SD dark currents separately. The dark currents are measured by the gradient of the plot of the dark signal versus accumulation time. A test chip with many test elements of the proposed pixels is fabricated in a 0.18um CIS technology(Fig.3). Each test element consists of 3x480 pixels. In this paper, a measurement result of only one type of the test elements is described. The pixel size is 7.5um × 7.5um, and the fill factors of the PD and SD area are approximately 20% and 14%, respectively.

Fig.4 shows the measured SD dark current as a function of V_{GSL} or V_{TXL} where, V_{GSL} and V_{TXL} are low levels of GS and TX gate pulses, respectively. In the measurements, either V_{GSL} or V_{TXL} is varid from 0V to -1.0V in order to measure

the effect of the negative gate biasing on the SD dark current. The ambient temperature is 25°C, and the chip temperature is approximately 30°C. As shown in Fig.4, the negative gate bias of the TX gate effectively suppresses the SD dark current, and the dark current with V_{TXL} = -1.0V is measured to 1/3 of that of V_{TXL} = 0V. The cumulative probabilities of the SD dark current are shown in Fig.5 and Fig.6. The negative gate bias reduces the number of "hot" pixels. For instance, in Fig.6, the number of pixels which have dark current of over 200e-/s is 2% of entire pixels at V_{TXL}=0V, and it is reduced to be approximately 0.3% at V_{TXL}=-1.0V.

As shown in Fig.5, the dark current reduction effect of negative gate bias on GS gate is smaller than that of the TX gate. This is because the region without the p_1 layer under the GS gate is about half of that under the TX gate. The number of pixels with the SD dark current of over 200e-/s at V_{GSL}=-1.0V is reduced to be half of that at V_{GSL}=0V.

Figs.7 and 8 show the measured PD dark current as a function of V_{GSL} and the cumulative probability. The negative gate bias of the GS gate has no significant effect to the PD dark current. These results indicate that the p_1 layer creating the stepwise-potential under GS gates helps to attract a hole accumulation at Si-surface, and the depletion dark current is suppressed sufficiently. Although the large negative gate bias leads to the increase of another dark current component due to Gate-Induced-Leak(GIL) Trap Assisted Tunneling(TAT) process [10], Fig.7 and Fig.8 do not show the PD dark current increase for V_{GSL} of up to -1.0V. The dark current generated from GIL-TAT process cannot be observed in this sensors.

Fig.9 shows the temperature dependence of PD and SD dark currents. In this measurement, both V_{GSL} and V_{TXL} are set to -1.0V. The activation energy is extracted from the Arrhenius plot [14]. The activation energy of PD dark current is 1.12eV, which is the same as the band-gap energy of Si, E_g. Therefore, the diffusion current is dominant in the PD dark current. On the other hand, the dominant sources of SD dark current are different at operating temperatures. At low temperatures below 25°C, the activation energy of SD dark current is around $E_g/2$, which indicates that the depletion dark current is dominant. At high temperatures over 50°C, the activation energy equals to E_g. The diffusion dark current of the SD is ten times smaller than that of the PD by the use of shielding structure.

IV. Conclusions

In this paper, the dark current characteristics of the two-stage charge transfer global shutter pixel are presented. By means of the negative bias technique, total dark current is reduced to 26.8 e-/s (PD:19.5 e-/s, SD: 7.3 e-/s) at ambient temperature of 25°C(the chip temperature is approximately 30°C), which is much smaller than that of other global shutter pixels. From the Arrhenius plot, the diffusion component of SD dark current is reduced to be ten times smaller than that of the PD, showing an advantage of the proposed pixel for reduced dark current. In the present structure, the PD dark current is dominated by diffusion component, which can be reduced by using of other structures such as an n-substrate structure.

Acknowledgment

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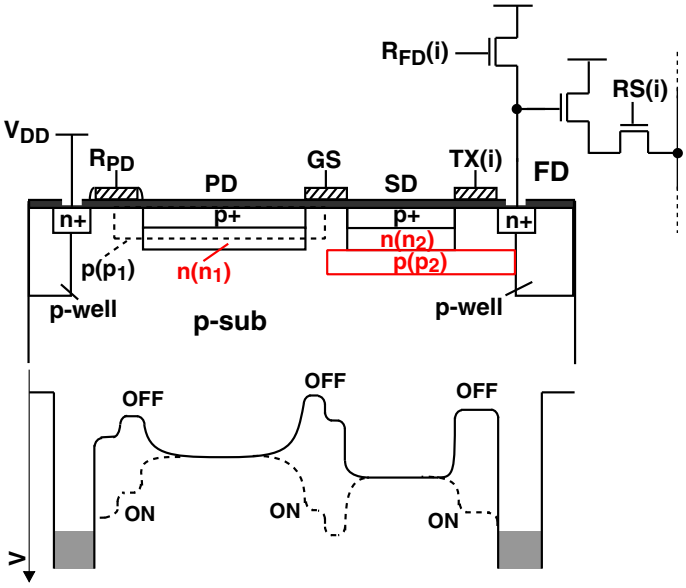

Fig. 1. Pixel structure and potential profile.

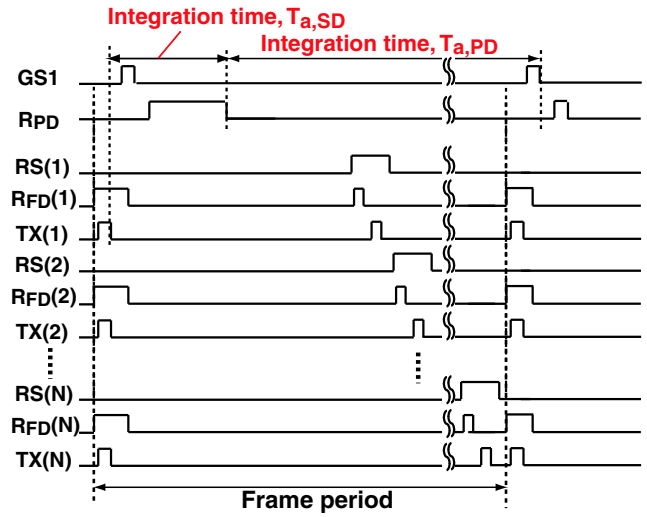

Fig. 2. Timing diagram for Measurements of the PD and SD dark current.

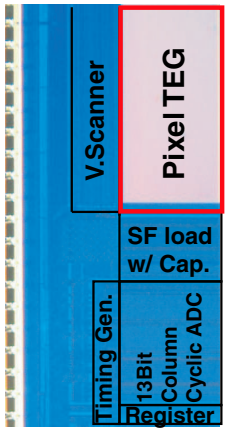

Fig. 3. Chip photograph.

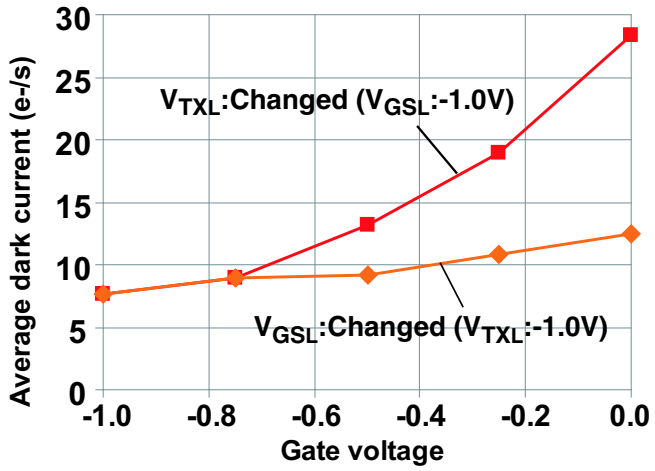

Fig. 4. SD dark current for various V_{GSL} and V_{TXL} voltages.

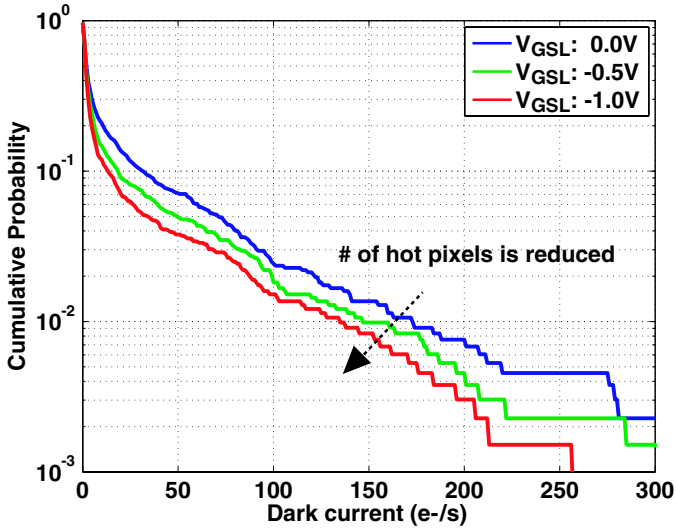

Fig. 5. SD dark current distribution for various V_{GSL} voltages.

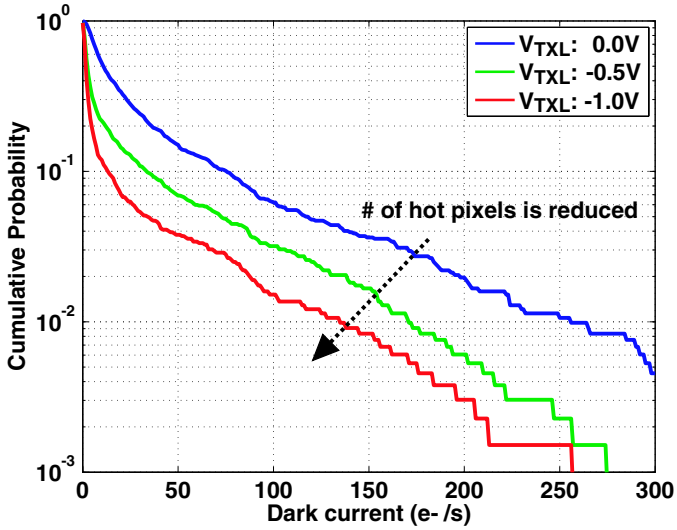

Fig. 6. SD dark current distribution for various V_{TXL} voltages.

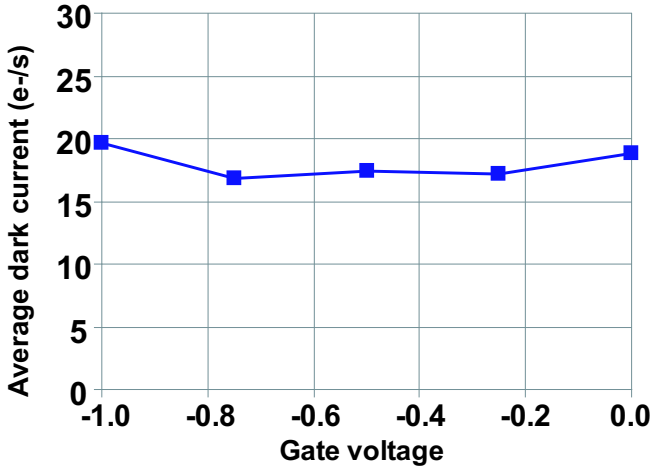

Fig. 7. PD dark current as a function of V_{GSL}.

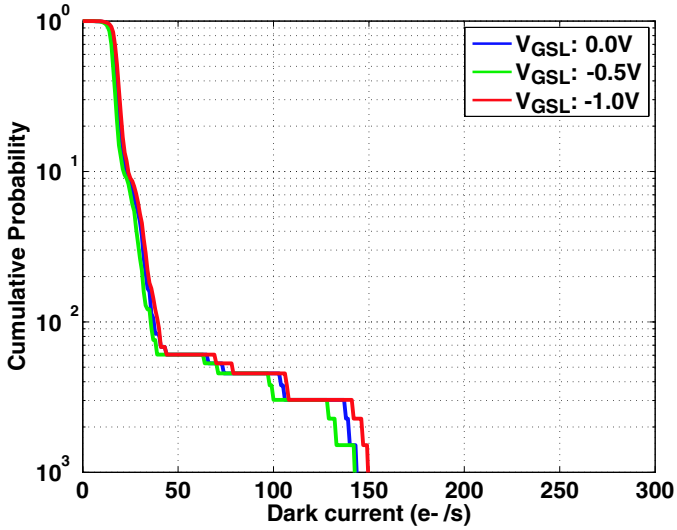

Fig. 8. PD dark current distributions for various V_{GSL} voltages.

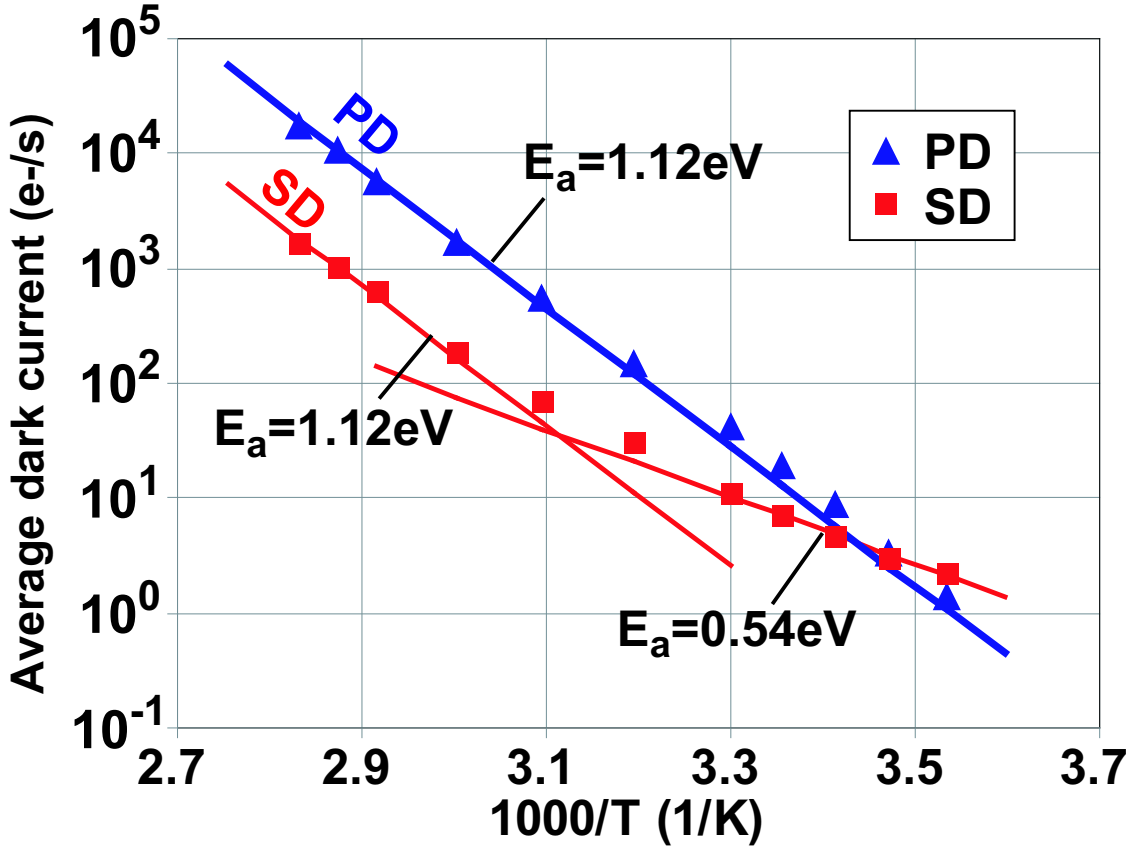

Fig. 9. Temperature dependence of PD and SD dark currents (V_{GSL} : $-1.0V$, V_{TXL} : $-1.0V$, V_{RPDL} : $0.5V$).