A Low Noise Low Power Global Shutter CMOS Pixel Having Single Readout Capability And Good Shutter Efficiency

Yannick De Wit, Tomas Geurts

ON Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
Yannick.DeWit@Onsemi.com tel +32 15 448773, fax +32 15 448

Abstract **This paper presents newly developed pixel architectures for low noise, low power high speed global shutter applications with good shutter efficiency. These pixels enable in-pixel correlated double sampling while requiring only a single readout. In high speed imaging, this allows to increase the speed by a factor of 2 compared to pixels which require to perform the subtraction outside the pixel (and thus require 2 separate reads). Multiple pixels with this architecture in different sizes have been developed, from 8.6 um to as small as 4.8 um, all developed in a commercial 0.18um technology.**

1. Introduction

Pipelined global shutter pixels are generally 5T pinned photodiode pixels (see **Figure 1**). They allow global shutter with double sampling (FPN correction) in pipelined readout mode. However, with these pixels it's not possible to do correlated double sampling (CDS). The consequence is that the noise performance is limited by the kTC noise of the floating diffusion capacitance degrading the performance in the dark which limits the obtained dynamic range.

Multiple attempts have been made to develop global shutter pixels with CDS capability [1,2,3]. Most of these require many transistors and capacitors or significant process changes. In [4], an alternative architecture is described similar to the first architecture in our paper. However, neither of these approaches achieves the combination of low noise, low power with single pipelined read and good shutter efficiency in a relatively small pixel.

The proposed architecture in this paper achieves this unique combination allowing state of the art global shutter performance.

2. In-pixel CDS Architecture Option 1

Figure 2 presents an in-pixel CDS with relatively poor shutter efficiency. The pixel consists of a 5T front end with CDS backend circuitry including 1 capacitor. A possible timing to operate such pixel is presented in **Figure 3**.

The disadvantage of this pixel is two fold. First of all, it requires a constant bias current for the first source follower (SF1) which will increase the total power consumption of the imager. The second disadvantage is that the signal is sampled on the floating diffusion in the 5T front end. The consequence of this is that it has high pixel storage node leakage (PSNL) and relatively poor shutter efficiency, also expressed as parasitic light sensitivity (PLS). This is a major drawback for global shutter pixels, especially when the readout time of the pixel array is long compared to the integration time. To improve the PLS, PSNL and to reduce the power consumption, a new in-pixel CDS architecture is developed as described in the next chapter.

3. In-pixel CDS Architecture Option 2

Figure 4 presents the in-pixel CDS architecture which enables to do CDS with single pipelined readout, low power and good shutter efficiency.

This pixel consists of a 4T front end with a CDS backend circuitry including 2 capacitors. In this case, the signal value is not sampled on the floating diffusion as in pixel architecture 1 but on the sample and hold capacitor C1 via SF1 and a sample switch. Due to sampling on this sample and hold capacitor, SF1 does not need a constant bias as in pixel option 1. This will reduce power consumption significantly. The second advantage of this pixel architecture is the improvement in PLS and PSNL. This is due to the fact that this sample and hold capacitor can be much larger than the floating diffusion capacitance combined with the fact that it does not need to only consist of a junction. In case of pixel architecture 1, a larger floating diffusion capacitance will not improve the parasitic light sensitivity because the floating diffusion capacitance also determines the conversion gain of the pixel. In pixel architecture 2, capacitor C1 has no impact on the conversion gain which allows it to be much bigger, reducing the parasitic light to voltage conversion directly.

4. Principle of Operation

The principle of operation for these pixel architectures consist of 2 phases, namely: sampling of the reset value and sampling of the signal value. During this second phase (sampling of the signal value), the CDS operation (R-S) occurs automatically due to the inherent nature of the architecture. The principle of operation will be described below for pixel architecture 2 according to the schematic and timing diagram of **Figure 4** and **Figure 5**.

Before integration, the photodiode is reset via the floating diffusion. After this photodiode reset, integration starts (frame capturing). After the integration time, the floating diffusion is reset to the pixel high power supply Vpix. This introduces kTC noise and for hard reset the rms noise voltage equals Eq 1.

$$V_{fdn_{rms}} = \sqrt{\frac{k \cdot T}{C_{fd}}} \quad \text{Eq 1}$$

With:

k: constant of Boltzmann, T: temperature in Kelvin, C_{fd}: floating diffusion capacitance in F.

This reset value including its kTC noise is now sampled on the capacitors C1 and C2 via the first source follower M3 and the sample switch M4. In the beginning of the sample period, these capacitors are precharged to erase their previous sampled voltage to enable the source follower M3 to conduct to sample a new voltage. This precharge operation can occur by using a separate precharge transistor as is the case in the pixel architecture presented in **Figure 2**. However, it can also be achieved by pulsing the drain of source follower M3 to a low voltage during the beginning of the sample period as is the case in **Figure 4**. The first source follower will then act as a precharge transistor. The advantage of the latter is that the pixel can operate with one transistor less, enabling the manufacturing of smaller pixels or pixels with a higher fill factor.

During the reset sampling period, the calibration transistor is turned off, effectively sampling the reset value on C1 while the right node of capacitor C2 is calibrated to a DC voltage, in this example Vpix.

After the reset sampling phase, charge transfer from the photodiode to the floating diffusion is enabled. This charge transfer is noiseless due to the fact that the photodiode is fully depleted after the charge transfer (a pinned photodiode is required). As a consequence, the new voltage on the floating diffusion will still have the same reset kTC noise as the one which is sampled during reset sampling. The floating diffusion voltage after charge transfer is then expressed in Eq2.

$$Vfd_{transfer} = Vpix - \Delta V_{ktc\_fd} - \Delta reset - Vt_{SF1} - \Delta V_{signal} \quad \text{Eq 2}$$

With:

$\Delta V_{signal} = \frac{Q_{charge\_pd}}{Cfd}$: the voltage drop on the floating diffusion due to the charge transfer, Vpix: The pixel high power supply, V_{ktc_fd} : the kTC noise due to the reset of the floating diffusion capacitance, $\Delta reset$: voltage drop on the floating diffusion due to reset clock feed-through, Vt_{SF1}: The threshold voltage of the first source follower .

This floating diffusion voltage is then sampled on C1 via the first source follower M3 and the sample switch M4. As a consequence, the voltage on C1 will drop from its previous reset value to a new value depending on the amount of charge transferred. Due to the fact that the right node of capacitor C2 is floating during this sampling phase, the amount of charge on C2 stays equal compared to the reset sampling phase (conservation of charge on C2). This means that the right node of C2 (Y) will drop from it's calibrated voltage (Vpix in this example) with the same range as the voltage drop on node X. The right node Y will not include the reset noise because it is always calibrated to a fixed dc voltage (Vpix in this case) when the reset noise is sampled during reset sampling phase.

This means that the output of the pixel will not include the kTC noise and the threshold variations of the first source follower implying that an effective CDS operation has been performed inside the pixel. Furthermore, this means that the pixel can perform CDS in a single readout enabling low noise high speed imaging. However, the drawback of single read out is that the FPN due to the threshold voltage variations of the second source follower will not be cancelled. To enable full FPN correction, double readout is still required. This is also shown as an option in the timing presented in **Figure 5**.

The in-pixel CDS operation is unfortunately not perfect. To accurately predict the performance of our pixels we need to include a more advanced model including the kTC noise of the capacitors C1 and C2, the temporal noise of the source follower transistors, their attenuation factors, as well as the parasitic capacitance which attenuates the signal. This is achieved by using the electrical model shown in **Figure 6**. There, the source followers M3 and M6 are modelled by amplifiers with attenuation factors A_{SF1} and A_{SF2} respectively whereas the total parasitic capacitance which influences the subtraction gain is modelled by capacitance Cp (this Cp also includes the gate-drain capacitance of the second source follower). The detailed derivation of the expected pixel performance can then be obtained as is shown below.

During reset sampling (after the calibration transistor is off), the charge on C2 and Cp is expressed in Eq3 and Eq4. The charge on C1 doesn't matter at this point in time as it is still driven by source follower 1.

$$Q_{reset\_C2} = C2 \cdot \left[\Delta V_{ktc\_fd} \cdot A_{SF1} + Vt_{SF1}\right] \quad \text{Eq 3}$$

$$Q_{reset\_Cp} = Cp \cdot Vpix \quad \text{Eq 4}$$

During signal sampling, the charge on C1, C2 and Cp is expressed in Eq5, Eq6 and Eq7.

$$Q_{signal\_C1} = C1 \cdot \left[Vpix - Vt_{SF1} - \left(\Delta V_{ktc\_fd} + \Delta V_{signal}\right) \cdot A_{SF1}\right] \quad \text{Eq 5}$$

$$Q_{signal\_C2} = C2 \cdot \left[Vy - \left(Vpix - Vt_{SF1} - \left(\Delta V_{ktc\_fd} + \Delta V_{signal}\right) \cdot A_{SF1}\right)\right] \quad \text{Eq 6}$$

$$Q_{signal\_Cp} = Cp \cdot Vy \quad \text{Eq 7}$$

Due to conservation of charge on node Y, we obtain Eq8.

$$Vy = Vpix - \left(\frac{C2}{C2 + Cp}\right) \cdot A_{SF1} \cdot \Delta V_{signal} \quad \text{Eq 8}$$

However, at the output of the pixel, the attenuation and threshold drop of the second source follower comes into the equation yielding in Eq9.

$$Vout = Vpix - Vt_{SF1} - \left(\frac{C2}{C2 + Cp}\right) \cdot A_{SF1} \cdot A_{SF2} \cdot \Delta V_{signal} \quad \text{Eq 9}$$

Because Vpix and Vt_sf1 are dc offset values, the output signal in function of the input signal equals Eq10.

$$\Delta Vout = \left(\frac{C2}{C2+Cp}\right) \cdot A_{SF1} \cdot A_{SF2} \cdot \Delta V_{signal} \qquad \text{Eq 10}$$

As expected, the kTC noise of the floating diffusion is not observed at the pixel output proving the CDS operation. However, there is attenuation of the signal voltage depending on the source follower gains and the ratio between the serial capacitor C2 and parasitic capacitor Cp. For optimal performance, C2 should be as big as possible while Cp needs to be as small as possible.

The pixel output noise will be dominated by the kTC noise of capacitor C1 and C2 as well as the noise of the source follower transistors. When the reset sampling occurs, capacitor C2 and Cp will introduce kTC noise at node Y of Figure 6 according to Eq11. Depending on the transconductance of the first source follower, the noise will be in the range as expressed in equation 11.

$$\sqrt{\frac{k \cdot T}{C2+Cp}} \leq Vn_{ktc\_Y} \leq \sqrt{\frac{k \cdot T}{\left(\frac{C2 \cdot C1}{C2+C1}\right)+Cp}} \qquad \text{Eq 11}$$

If the first source follower is operating in saturation during the reset sampling phase, for example in pixel architecture 1, the kTC noise will be close to that of the left side of Eq11 whereas in pixel architecture 2, the source follower will go near cut-off region so that the kTC noise will be more closer to the expression at the right side of Eq11.

During signal sampling, capacitor C1 and the serial combination of C2 with Cp will introduce kTC noise at node X of **Figure 6** according to Eq12.

$$Vn_{ktc\_X} = \sqrt{\frac{k \cdot T}{C1+\left(\frac{C2 \cdot Cp}{C2+Cp}\right)}} \qquad \text{Eq 12}$$

After including the second source follower temporal noise, source follower attenuation and the attenuation due to voltage divider C2/Cp we obtain Eq13 for the final output noise voltage.

$$Vn_{out} = \sqrt{\left[(Vn_{ktc\_Y})^2 + \left(\frac{Vn_{SF2}}{A_{SF2}}\right)^2 + \left((Vn_{1/f\_SF1})^2 + (Vn_{ktc\_X})^2\right) \cdot \left(\frac{C2}{C2+Cp}\right)^2\right]} \cdot A_{SF2} \qquad \text{Eq 13}$$

With:
Vn_{1/f_sf1}: The 1/f noise contribution of source follower 1,
Vn_{sf2}: The noise contribution of the second source follower (including temporal and 1/f noise).

The expression of Eq13 enables to optimize capacitor sizes C1, C2 as well as the size of the source followers. The size and shape of the second source follower is particular important because it has direct influence on its noise performance, its gain and the parasitic capacitance Cp.

5. Characterization Results

Both pixel architectures 1 and 2 have been developed in three different pixel sizes: 8.6um, 6.1um and 4.8um. The pixels are manufactured in two different commercial 0.18um image sensor foundries, the 8.6um pixels in technology 1 and the 6.1 and 4.8um pixels in technology 2.

The expected results for the pixels of architecture 1 are shown in **Table 1** and these for the pixels of architecture 2 in **Table 2**.

The measurement results are available for the 8.6um pixels which are presented in **Table** 3. As can be seen, the predicted performance parameters match excellent with the measured values. The measured response curves for these pixels are shown in **Figure** 7.

The improvement in shutter efficiency between option 1 and option 2 for these 8.6um pixels is significant (a factor 8.7 better in option 2 compared to option 1) proving the advantage of architecture 2 compared to architecture 1.

The 6.1um and 4.8um pixels are developed in another 0.18um technology (technology 2). The pixel design has been improved significantly compared to the 8.6um pixels. Their expected results are state of the art as is shown in **Table 1** and **Table 2**.

6. Conclusion

ON Semiconductor developed low noise global shutter pixels for high speed image sensor applications with improved noise performance, shutter efficiency and power consumption compared to current existing global shutter pixels. The first silicon results are in excellent agreement with the expected performance from the theoretical analysis.

The authors would like to thank Thomas Cools for his technical review and input.

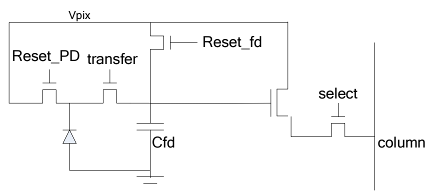

Figure 1: 5T pixel schematic

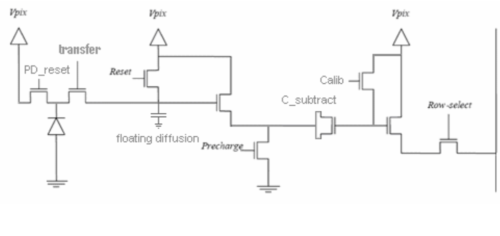

Figure 2: Schematic of the in-pixel CDS pixel with poor shutter efficiency (option 1)

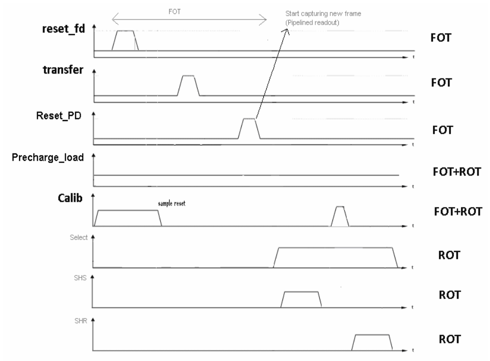

Figure 3: Possible timing for the in-pixel CDS pixel with poor shutter efficiency (option 1)

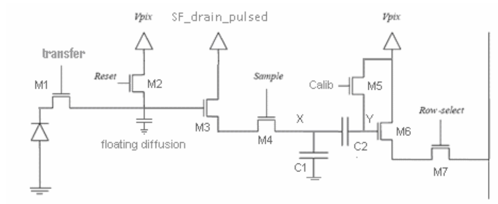

Figure 4: Schematic of the in-pixel CDS pixel with good shutter efficiency (option 2)

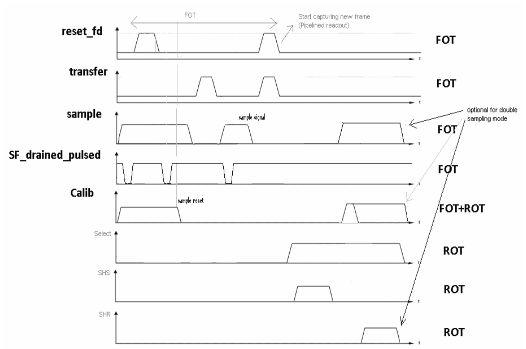

Figure 5: Timing for the in-pixel CDS pixel with good shutter efficiency (option 2)

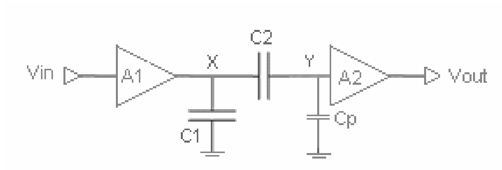

Figure 6: Electrical model for pixel architecture 2

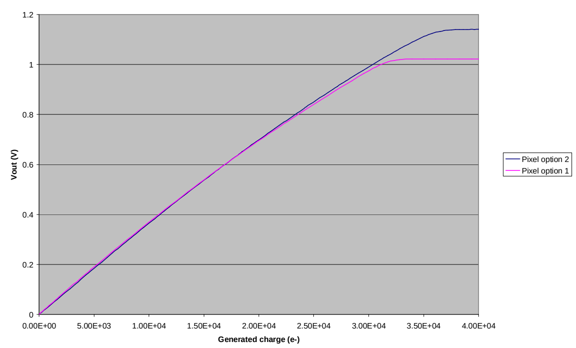

Figure 7: Measured response curves of the 8.6um in pixel CDS pixels.

Parameter	*4.8um*	*6.1um*	*8.6um*
Conv. Gain (dark)	150uV/e-	128uV/e-	40.4uV/e-
FWC	7900e-	10400e-	25200e-
Noise single read	4.6e-	4.9e-	12.7e-
Noise double read	6.4e-	6.9e-	18e-
Dynamic range single read	64.9dB	66.5dB	65.9dB
Dynamic range double read	61.9dB	63.5dB	62.9dB
PLS	<1/400	<1/600	<1/800

Table 1: Expected performance for different in-pixel CDS pixels of architecture 1

Parameter	*4.8um*	*6.1um*	*8.6um*
Conv. Gain (dark)	145uV/e-	134uV/e-	40.4uV/e-
FWC	8400e-	9500e-	25200e-
Noise single read	7.1e-	5.8e-	13.8e-
Noise double read	9.4e-	7.65e-	18.4e-
Dynamic range single read	61.4dB	64.3dB	65.2dB
Dynamic range double read	59dB	62dB	62.7dB
PLS	<1/3000	<1/4000	<1/6000

Table 2: Expected performance for different in-pixel CDS pixels of architecture 2

Parameter	*8.6um architecture 1*	*8.6um architecture 2*
Conv. Gain (dark)	39.5uV/e-	37.7uV/e-
FWC	29500e-	34000e-
Noise single read	13e-	13.9e-
Noise double read	N.M.	N.M.
Dynamic range single read	67.1dB	67.7dB
PLS	1/1000	1/8700

Table 3: Measurement results for the 8.6um in-pixel CDS pixels

References:

[1] Two-Stage Charge Transfer Pixel Using Pinned Diodes for Low-Noise Global Shutter Imaging

Keita Yasutomi[1], Shinya Itoh[1], Shoji Kawahito[1], Toshihiro Tamura[2]. [1]Research Institute of Electronics, Shizuoka University, Japan; [2]Photron Ltd., Japan, 2009 Image sensor workshop Bergen, Norway.

[2] Comparison of Global Shutter Pixels for CMOS Image Sensors

Stefan Lauxtermann, Adam Lee, John Stevens, and Atul Joshi (Teledyne Imaging Sensors, Camarillo, USA), 2007 Image sensor workshop Ogunquit, ME.

[3] High-end CMOS Active Pixel Sensor for Hyperspectral Imaging

J. Bogaerts, B. Dierickx, P. De Moor, D.S. Tezcan, K. De Munck, C. Van Hoof, IEEE workshop on CCD and AIS, Karuizawa, Japan, 9-11 June 2005.

[4] kTC Noise Cancellation Pixel

R.B. Merrill, Foveon, Inc, 2001, Image sensor workshop, Lake Tahoe, Nevada USA.