A 1.2MP 1/3" Global Shutter CMOS Image Sensor with Pixel-Wise Automatic Gain Selection

Johannes Solhusvik[1], Sergey Velichko[2], Trygve Willassen[1], Sohrab Yaghmai[1], Jenny Olsson[1], Anders Rosnes[1], Tore Martinussen[1], Per Olaf Pahr[1], Siri Eikedal[1], Steve Shaw[3], Ranjit Bhamra[3], Dan Pates[2], Scott Smith[2], Lingtao Jiang[2], David Wing[2] , Jenny Bai[2], Satyadev Nagaraja[2], Ajaya Chilumula[2]
[1]Aptina Norway AS, Oslo, Norway,
[2]Aptina, LLC, San Jose, CA, USA,
[3]Aptina (UK) Limited, Bracknell, UK

A 1280x960 45fps CMOS image sensor with global shutter is presented. Main novelties are (i) 3.75µm pixel pitch which is smallest GS pixel pitch published to date in CMOS, and (ii) per-pixel automatic gain selection (AGS) which improves intra-scene dynamic range. The pixel circuit is illustrated in fig.1. A vertical two-way shared architecture yields four transistors per pixel (4T) compared to 6T in a non-shared configuration. Each pixel has a storage gate transistor (SGA or SGB) which controls charge transfer from photodiode (PDA or PDB) to the storage diode (SDA or SDB).

The storage gate (SG) and its accompanying storage diode (SD) act as a photon-charge storage node as illustrated in the pixel cross section in fig.2. Since the storage node is electrically isolated from the floating diffusion (FD) correlated double-sampling (CDS) readout is supported. Each pixel row-pair has an extra reset transistor (labeled AB) which can be turned ON to drain charge from the photodiode (PD) to 2.8V power supply. This can occur simultaneously to, and without impacting, the CDS readout process. Thus, a new image capture can commence whilst reading out the previous frame. Note that since AB is globally controlled it too can be shared between two rows to save area. During photon integration the voltage on AB gate is kept slightly positive to act as an anti-blooming drain.

A high-level timing diagram for global shutter capture operation is illustrated in fig.3. The vertical axis represents time and starts with 30 row-times of vertical blanking (VB). Inside this VB phase SG is pulsed to transfer the captured image from PD to SD. Reference pixels for offset calibration are read out during VB. Thereafter, frame readout can commence, i.e. CDS readout of all rows sequentially until the end of the array. During frame readout a new picture can be captured by turning OFF the AB gates which initiates PD photon integration. At the end of integration (and frame readout) SG is pulsed again to freeze and store the captured frame, and the readout process can re-commence.

Fig.4 illustrates the analog readout architecture. Column-parallel and top-bottom readout was selected to minimize power and read-noise. Note that the top section of the readout block (above the array) is omitted in fig.4 for simplicity. Every column-pair has a 2:1 multiplexer (MUX), a 1x, 2x, 4x, 8x configurable gain amplifier, and a 12-bit successive approximation (SA) ADC running at up to 750kpix/sec. The CDS and A/D conversion process for one row takes approximately 5.5µs.

The CDS readout includes automatic gain selection (AGS) which is used to suppress noise contribution from the ADC when sensor operates in unity gain mode. AGS operates on a per-pixel basis and involves three phases as illustrated in fig.5: (i) compare pixel output against threshold, (ii) adjust gain accordingly, (iii) allow amplifier output to settle and then start A/D operation. The pixel signal level is measured after CDS and compared against a fixed voltage threshold approximately equal to Vref/G_{HI}. The comparator (re-used from ADC) output signal is routed to the differential column amplifier to select which gain to use, i.e. either G_{HI} (8x, 4x or 2x) or G_{LO} (1x). This gain select bit is also used in the digital signal processing path to linearize the pixel output value. To avoid non-linearity issues, the G_{HI}/G_{LO} gain ratio value must be precisely measured. This is done during vertical blanking time using dedicated reference pixels read out with high and low gain. It is worth noting that area and power penalty for AGS is kept small thanks to re-using the comparator belonging to the ADC.

The imager was fabricated in a 2.8V 130nm CMOS 2LP4LM process. Initial results on monochrome pixels without any process tuning or design optimization are provided in below plots and tables. A comparison is made with a 6µm GS product (Aptina's MT9V024). Overall conclusion is that light sensitivity and noise level is excellent and outperforms the 6µm imager, virtually no lag is observed, and the AGS function performs as predicted.

Shutter efficiency on initial silicon is measured to 310:1. In comparison, minimum acceptable shutter efficiency in interline CCDs is in the order of 1000:1 or better. Our goal is to reach this value after process tuning and optimization of optical stack and readout timing.

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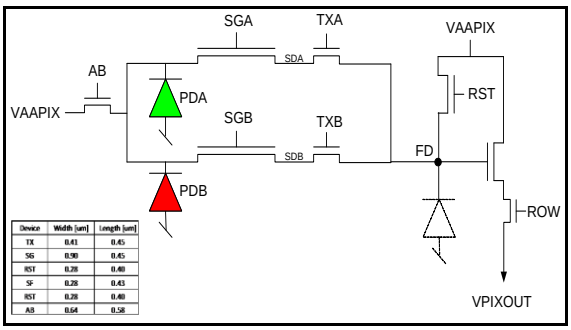

Fig.1

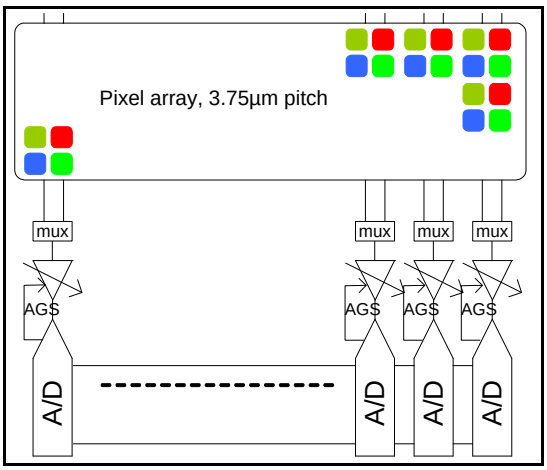

Fig.4

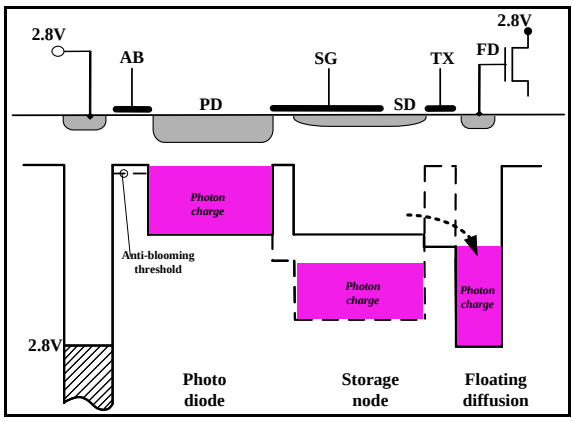

Fig.2

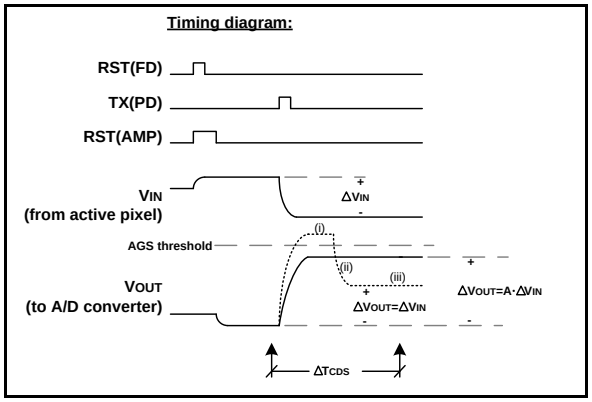

Fig. 5

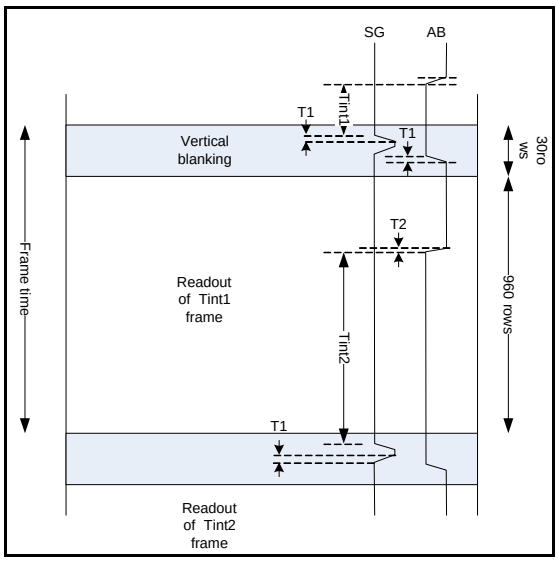

Fig.3

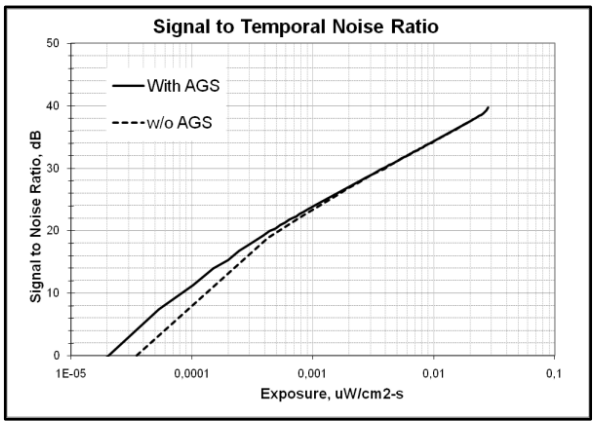

Fig. 6

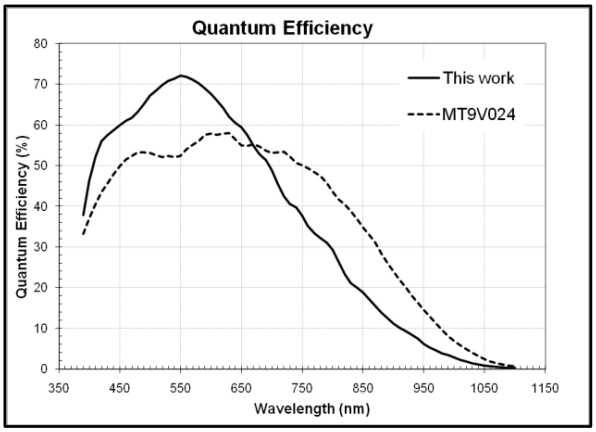

Fig.7

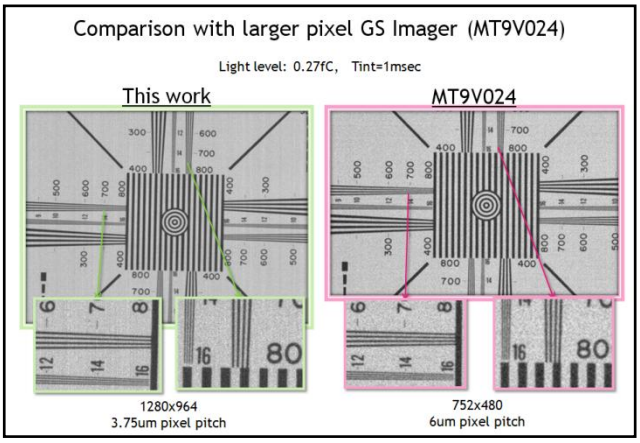

Fig.8

Parameter	Symbol	Units	MT9V024	This work
Readout noise	st	e	**21.9**	**2.4**
Photoresponse non-uniformity	PRNU	%	**0.76**	**0.86**
Row/Column FPN at 50% signa	Row/ColFPN	%	**0.09, 0.19**	**0.10, 0.22**
Dark signal non-uniformity	DSNU	%	**0.48**	**0.18**
Non-linearity		%	**+3/-3**	**+1/-1.5**
Total SNR at 50% signal	SNR	dB	**38.0**	**33.5**
Dynamic Range	DynR	dB	**58.1**	**69.0**
Responsivity	R	Ke/µW/cm2*s	**551**	**289**
Linear Full-well Capacity		Ke	**17.5**	**7.5**
Discharging Lag @ 40%	DL40%	%	**<0.5**	**0.01**
Charging Lag @ 40%	CL40%	%	**<0.5**	**0.05**
Max Quantum Efficiency	QEmax	%	**55.3**	**73.6**
MTF at 80 cys/mm	MTF80c/mm		**0.35**	**0.58**
Global Shutter Efficiency	GSE	%	**1000:1**	**310:1**

Table 1