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Backside illuminated global shutter CMOS image sensors

Guy Meynants, Jan Bogaerts, Xinyang Wang, Guido Vanhorebeek
CMOSIS nv, Coveliersstraat 15, 2600 Antwerp, Belgium
guy@cmosis.com, +32 3 260 17 32

Introduction

We report on 2- and 4 megapixel backside illuminated image sensors with a 5.5 µm global shutter pixel manufactured in 0.18 µm CMOS. Global shutter pixels require an in-pixel storage node next to the photodiode. This storage node should not be light sensitive. This is specified by parasitic light sensitivity, which is the ratio of the amount of light detected by the storage node divided by the amount of light detected by the photodiode. In many global shutter pixels, the signal is stored on a junction, either the floating diffusion [1], a combination of floating diffusion and other capacitance [2] or a dedicated buried diode implantation [3]. In either case, the in-pixel storage node is shielded from light by a metal shield. Parasitic light sensitivity is worse for longer wavelengths and typically around 1/500 to 1/1000 for a frontside illuminated sensor. For a backside illuminated sensor parasitic light sensitivity is considered to deteriorate considerably due to the lack of a light shield on top of the storage node. The approach taken for this backside illuminated sensor avoids storage of the pixel signal on a diffusion. This guarantees a good parasitic light sensitivity, even for a backside illuminated device.

Pixel structure

The pixel is an 8-transistor active pixel with 2 storage nodes, shown in fig. 1, which has been reported earlier in its frontside version [4]. It stores the reset and signal values on two equal in-pixel capacitors of 16 fF each. These capacitors are actual NMOS transistor gates in inversion regime. The signal on both capacitors is subtracted in the column amplifiers. Correlated double sampling is combined with global shutter operation.

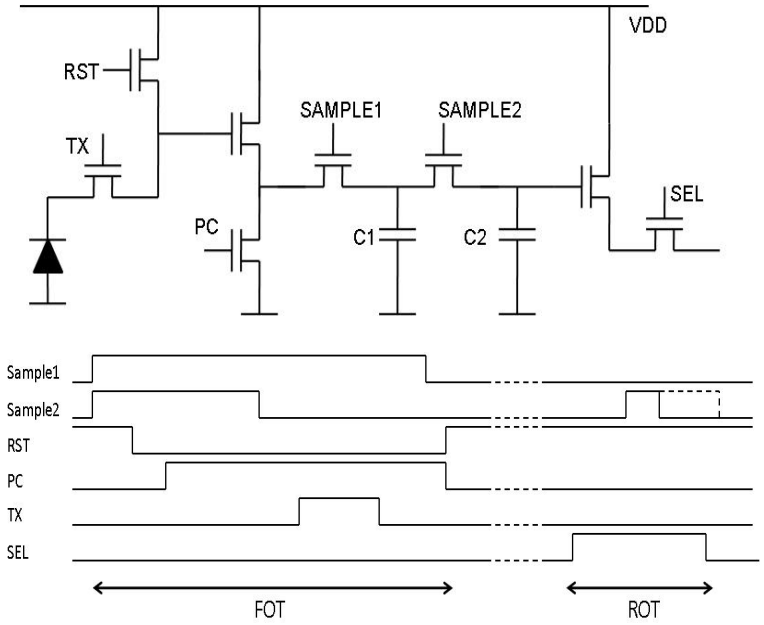

Figure 1: pixel schematic and timing

The pixel inherently has a good parasitic light sensitivity because of the following 3 measures:

1. the signal is stored on the gate, which does not collect any photocharges. Only the very small source junctions of the sample switches may collect some photocharges
2. the floating diffusion is designed for max. conversion gain, in this case 100 µV/e-. The storage capacitors are 16 fF, which corresponds with a conversion gain of the storage nodes of 10 µV/e- . This means that the impact of a charge collected by the storage node instead of the photodiode on the signal is 10x smaller.

3. Both in-pixel capacitors have a nearly equal chance that a photocharge is collected by one of them. The signal stored on both capacitors is subtracted for the CDS operation. The parasitic light sensitivity signal is a common-mode signal on both capacitors, and it is cancelled out by CDS.

Parameter	**Value**
Pixel size	5.5 µm
Conversion gain	100 µV/e-
Full well charge	13,500 e-
Read noise	10 e- RMS
Dynamic range	62.6 dB
Peak QE	60% (without optimized AR coating) (60% peak frontside illuminated with microlens)
Shutter efficiency Parasitic light sensitivity	99.996% (99.999% on frontside illuminated) 1/25,000 (1/110,000 frontside illuminated)

Table 1: pixel parameters measured on the backside illuminated sensor

Measured pixel parameters are given in table 1. The parasitic light sensitivity of the storage node is 1/25,000 for the backside sensor resulting in a shutter efficiency of 99.996%. With frontside illumination the parasitic light sensitivity and shutter efficiency are 1/110,000 and 99.999% respectively. Since such low parasitic light sensitivity is not simple to measure, we also clarify the measurement procedure here:

1. take an image at shortest exposure time, with strong illumination (near to saturation). In this image, row #1 has the shortest signal storage time, row#2048 has the longest storage time.
2. take an image with the same conditions, but revert the row readout (read out last row first). In this image, row#1 has the longest signal storage time
3. subtract the 2 images and take the average per row.
4. Plot the profile of the subtracted row averages, this shows the parasitic signal in function of the storage time, linearly variable from the first row to the center row. From this slope, the light sensitivity of the storage node can be calculated.
5. Divide this number by the light sensitivity of the pixel to get the parasitic light sensitivity.

Process flow and optimization of the UV response

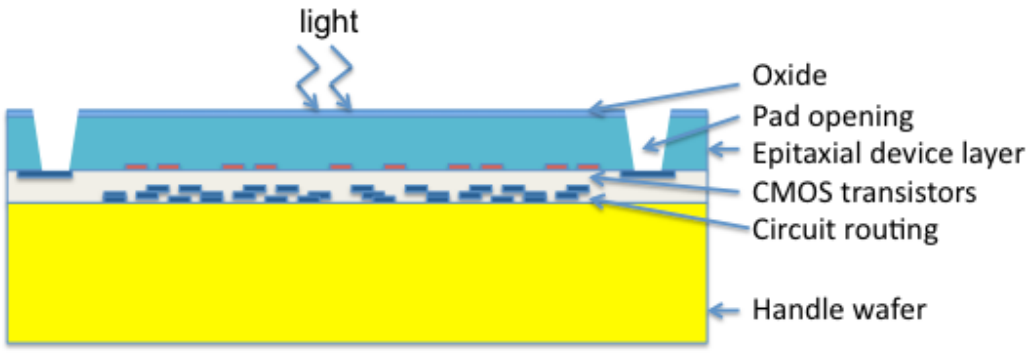

Figure 2: device cross-section after thinning

The backside thinning is done on wafer level and based upon an SOI flow. It starts from CMOS wafers processed on 5.0 µm SOI substrates. Two different wafer bonding mechanisms were used: oxide-oxide bonding and glue bonding between the handle wafer and device wafer. After bonding, the device is thinned down to the buried oxide layer. In some variants, the buried oxide remained on the backside surface, serving as an AR coating. In other variants, the buried oxide was etched away and replaced by a thin oxide, to allow further postprocessing steps which are discussed below. Bond pads are opened to the metal1 level from the illuminated side. Figure 2 shows a cross-section of the device.

Figure 3 shows the quantum efficiency on BSI devices and FSI devices with microlens. When the original buried oxide is still present, the peak QE is 60% which is similar to the FSI QE around 600 nm. The oxide acts as a (non-optimal) AR coating. When the buried oxide is etched away, the QE drops to 48%. The peak QE can be further improved by anti-reflective coating, this was not further explored in the frame of our research project. Instead, an increase of the response in the blue and UV region is investigated, as the response is rather weak for blue light, and as our applications are situated in that area.

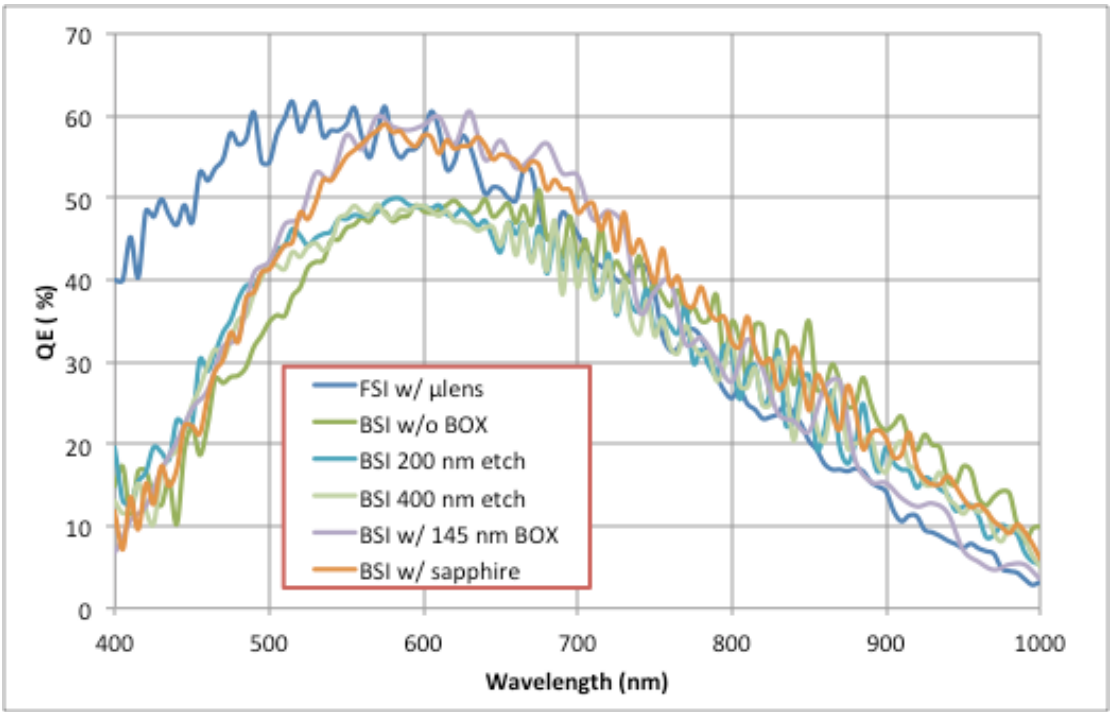

Figure 3: measured QE on the FSI sensor (with µlens), the BSI image sensor (without AR coating) with and without oxide at the backside surface, and with an additional etch of 200/400 nm

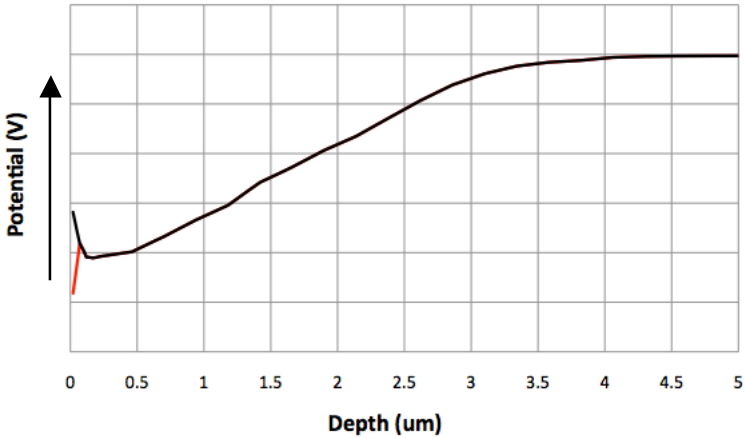

Figure 4: potential profile cross-section showing dead zone; effect of sapphire on the potential profile (red curve)

Initially the substrate is highly doped at the backside. However, after CMOS processing, the doping profile has a peak concentration slightly below the backside surface, due to strong outdiffusion during the various thermal CMOS processing steps. This creates a potential peak below the surface (shown in the profile of figure 4), which creates a dead zone near the surface. This reduces the blue and UV response. There are several ways to remove the dead zone, each requiring a removal of the (originally buried) oxide first: 1) ion implantation and laser anneal at the backside; 2) further etching (thinning) of the silicon; and/or 3) deposition of a layer with fixed negative charge. We report here on the latter 2 routes, namely a further etch of the silicon of 250 and 400 nm to make sure that the peak doping concentration is at the surface; and the deposition of a 60 nm layer of sapphire (Al2O3). Sapphire has a fixed negative charge that can compensate the potential profile (fig. 4). Results of both experiments are shown also in figure 3. The results at this moment are showing no improved blue response. We conclude that a combination of the etch step with sapphire deposition or an ion implantation will be required to improve the QE in the blue region. The QE is increased by sapphire deposition at longer wavelengths compared to the case without buried oxide due to the buried oxide due to improved anti-reflective properties of the sapphire coating.

Further results

		FSI	400nm etched BSI	250nm etched BSI	BSI with sapphire
Detector thickness		5.5 µm (epi)	4.6 µm	4.75 µm	5.0 µm
MTF	Blue	0.70	0.51	0.61	N/A
	Green	0.72	0.60	0.69	N/A
	Red	0.61	0.62	0.64	N/A
Dark current (22ºC)		105 e-/s	406 e-/s	370 e-/s	1028 e-/s

Table 2: measured MTF and dark current on the FSI and BSI sensors

Table 2 shows measured MTF data for red, green and blue light, as well as dark current data. Dark current increases most for the sapphire covered BSI chips.

Wafers containing 2 and 4 Mpixel imagers were thinned. The imagers operate at 300 fps (2 MPixel) and 180 fps (4 MPixel) in 10 bit on-chip AD conversion mode, and at 75 fps (2 MPixel) and 45 fps (4 MPixel) in 12 bit AD conversion mode. Figure 5 shows images captured with the 2 Mpixel device in front- and backside illumination.

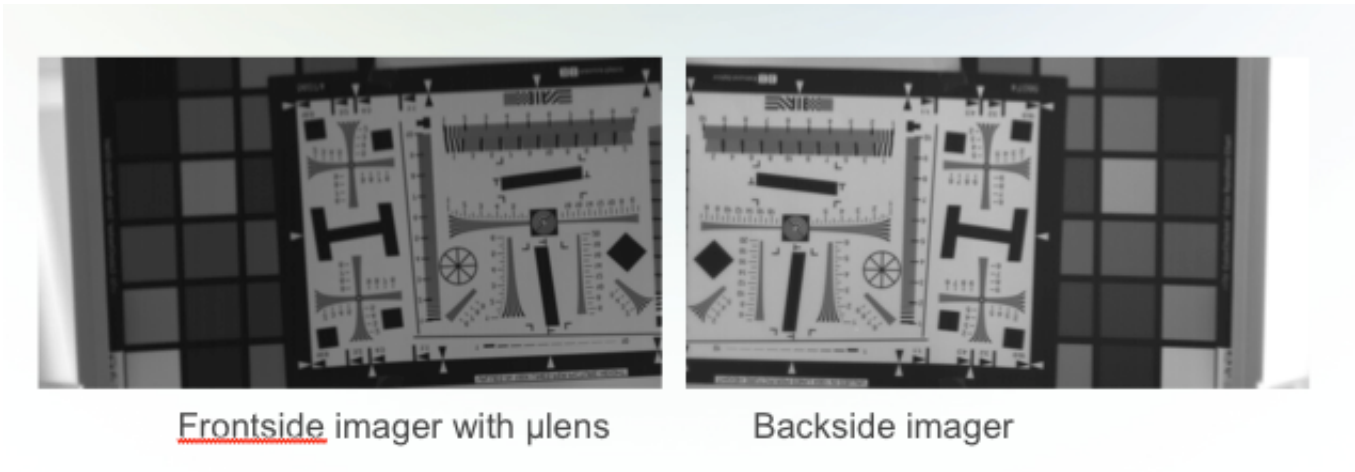

Figure 5: images captured with frontside and backside sensor

Conclusion

A global shutter pixel on a backside illuminated image sensor was demonstrated. This was developed on an SOI based flow with pre-profiled epitaxial layer substrate. However, the outdiffusion of the pre-doped layer requires additional process steps to generate a good QE for short wavelengths. Such BSI global shutter pixel can be used to extend the wavelength range and may find applications in scientific and machine vision applications.

Acknowledgement

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