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Single Grain TFTs and Lateral Photodiodes for Large Area X-ray Detection

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Abstract

Amorphous-Si thin-film-transistors (TFT) which require a lower process temperature compared to IC technology permit use of large area glass substrates and have been used for digital X-ray detection. However, because of the low field effect mobility (1 cm^2/Vs) and high trap density, image lag problem exists. Poly-Si TFTs improve mobility but due to existence of random grain boundaries, light sensitivity is low.

Motivation of this paper is to develop an indirect X-ray detector with photodiodes and readout circuits inside 2D-location controlled silicon islands. A low-temperature process, based on the μ-Czochralski technique with excimer-laser crystallization of a-Si film has been used to control the positions of the islands. The proposed X-ray image sensor is a solution to the lag problem and frequency limitation of a-Si TFT via high mobility while achieving a detection area for chest radiography without the tiling process which causes data lost at the connection of the detector arrays.

Lateral PIN photodiodes, which enable the integration of TFTs on the same pixel, are employed to detect the visible light. We have controlled position of 6 μm x 6 μm silicon grains with excimer laser crystallization of a-Si film. Upon laser irradiation to the a-Si layer, crystallization occurs from the grain filter locations forming location-controlled Si grains there whereas the outside crystallizes as micro-crystalline silicon as it fully melts. Channel region of the SG-TFTs and intrinsic region of the PIN PDs were designed to be located in each single grain, since at the grain boundaries there are dangling bonds which trap electrons limiting the carrier mobility. Lateral PIN photodiode (PD) arrays have 1 μm, 1.5 μm and 2 μm intrinsic region length and 4 μm width. SG-PDs were fabricated using 1 μm thick crystallized Si layer to increase the sensitivity of the silicon layer for long wavelengths (>400 nm). 100 μm x 100 μm size single grain photodiodes have dark and saturation currents in the order of 0.1 nA and 10 nA resulting in a light sensitivity of 200 with an exposure of 150 W white light. Dark current increases with array size. For comparison, we fabricated same photodiode designs using SOI and a-Si deposited wafers, as well. Fabricated SG and c-Si photodiodes reach higher photocurrent values than a-Si photodiodes at forward bias mode. Moreover, fabricated a-Si photodiodes have very low light sensitivity (<10).

Single grain TFTs are fabricated with 250 nm thick crystallized silicon layer with 1.5 μm gate length and 4 μm gate width. Fabricated NMOS and PMOS TFTs inside the grains have field effect mobility of 526 cm^2/Vs and 253 cm^2/Vs, respectively.

Keywords: X-ray, thin-film-transistor (TFT), single grain, large area detection, image sensor, μ-Czochralski process

1. INTRODUCTION

Digital X-ray radiography detectors are currently using a-Si thin-film-transistors (TFTs) which can be fabricated with lower process temperature compared to IC technology and therefore enable use of large area glass substrates [1]. However, because mobility is very low (1 cm^2/Vs) and trap density is high, image lag problem arises. Poly-Si TFTs can improve mobility and hence enables higher resolution, but trap states at random grain boundaries [2] reduce the light sensitivity in the photodiode.

The proposed indirect X-ray detector [3] employs photo sensitive 2D-location controlled silicon islands as photodiode array and readout electronics, as illustrated in Figure 1(a). To control the positions of the islands, the μ-Czochralski technique developed in TU Delft using excimer-laser crystallization of a-Si film has been used. Because of the low temperature process, the proposed X-ray image sensor can achieve detection area for chest radiography without the tiling process of bulk Si CMOS chips [4] which causes data loss at the connection of the detector arrays and solve the lag problem and frequency limitation of a-Si TFT via high mobility [5].

In this paper, first the μ-Czochralski technique is explained and then the SG-TFT and SG-PD designs are presented. In order to increase the sensitivity of the silicon layer for long wavelengths (>400 nm), SG-PDs were fabricated using 1 μm thick crystallized Si layer. In this novel image sensor, we used lateral PIN photodiodes, which can be integrated with TFTs on the same pixel to detect the visible light converted from X-ray by scintillator material (Figure 1(b)). For comparison, lateral PDs were fabricated using SOI wafer and a-Si layer, as well. SG-PDs were fabricated in three different sizes to optimize the pixel size of the image sensor. Measurement results show that, SG-PD can be substitute for single crystalline PDs with its

high sensitivity and low dark current. SG-TFTs were fabricated with 250 nm thick crystallized silicon layer with 1.5 µm gate length. Transfer characteristics of N- and PMOS SG-TFTs are demonstrated.

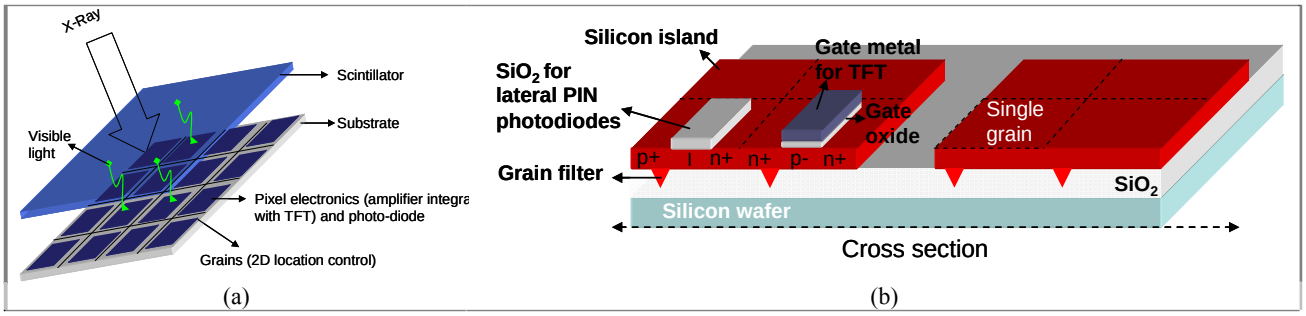


Figure 1 (a) Scheme of the indirect-detection X-ray image sensor with single grain (SG) photo-diode and thin-film transistors. (b) Schematic of integrated SG-lateral PIN photodiodes and SG-TFTs in the same pixel.

2. 2D-LOCATION CONTROLLED CRYSTALLIZATION and FABRICATION of SG PDs and SG-TFTs

2D-location controlled Si grains are fabricated using low temperature µ-Czochralski process. Process flow started with oxidation of 4-inch Si-wafer. 1 µm x 1 µm size cavities were patterned in SiO_2 and the cavity diameter was reduced to 100 nm with depositing 855 nm tetra-ethyl-ortho silicate (TEOS) using plasma-enhanced chemical vapor deposition (PECVD) at 350 ºC. After defining the cavities which later serve as the grain filter, a 250 nm or 1 µm thick a-Si is deposited on different wafers. Grain size is defined by the pitch and size of the grain filters, and excimer laser energy density. As shown in Figure 2(a), crystallization of Si starts at the grain filter location and extends the outside which is completely melted. 6 µm x 6 µm sized, square shaped grains have been successfully obtained with 1 µm thick Si as shown in the SEM image of the crystallized layer in Figure 2(b).

Channel region of the SG-TFTs and intrinsic region of the PIN PDs (Figure 3(a)) were designed to be located in each single grain since the carriers are otherwise trapped by the dangling bonds at the grain boundaries reducing the carrier mobility and photodiode sensitivity. Intrinsic region length (L) of the lateral PIN photodiodes was varied with 1 µm, 1.5 µm and 2 µm. To increase the intrinsic area, photodiodes were interdigitated as shown in Figure 3(a). We designed three different total PD array areas; 100 µm x 100 µm, 250 µm x 250 µm and 500 µm x 500 µm.

For SG-TFTs, gate length and width were kept at 1.5 µm microns and 4 µm microns, respectively. TFTs were fabricated in 250 nm thick crystallized silicon and SOI, while the PD arrays were fabricated using SOI (device thickness=340 nm), a-Si (thickness=1 µm) and the SG-Si (thickness=1 µm and 250 nm). 30 nm thick SiO_2 was deposited by PECVD using TEOS at a temperature of 350 °C for gate oxide.

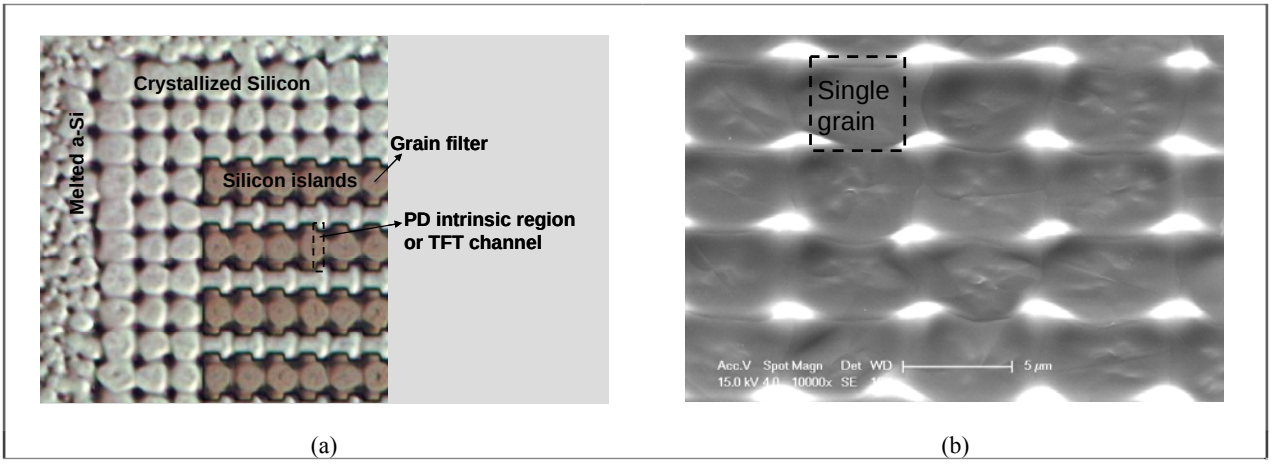


Figure 2 (a) Optical image of crystallized silicon layer. (b) SEM picture of 6 µm x 6 µm size grains in 1 µm thick a-Si layer.

(a) (b)

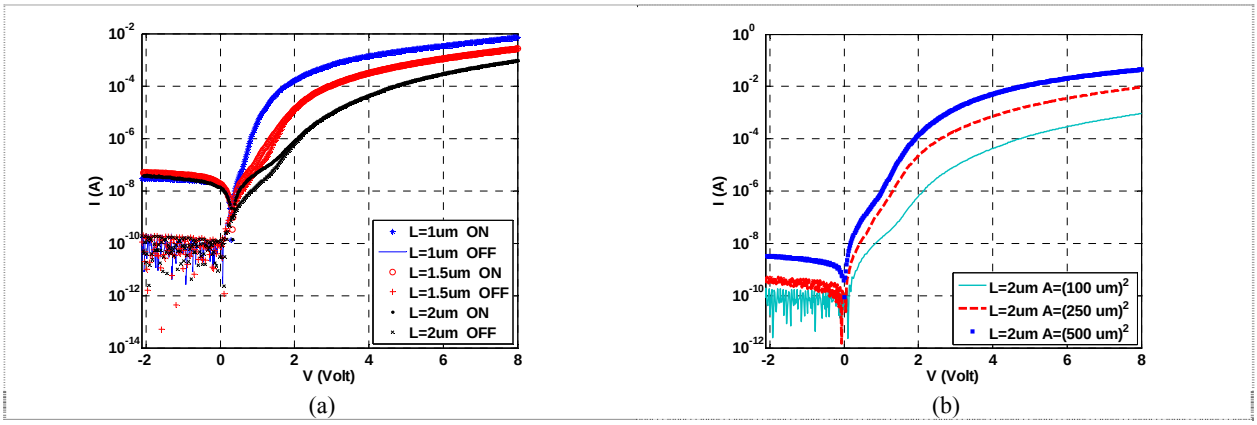
Figure 3 (a) SEM picture of fabricated lateral SG-PIN photodiode array with 1 µm thick crystallized silicon layer. (b) Picture of the test chip mounted on a test PCB.

3. ELECTRICAL MEASUREMENTS of LATERAL SG-PDs and SG-TFTs

Electrical characteristics of the fabricated PD arrays and TFTs are illustrated in this section. Fabricated dies ($4cm^2$) were attached on test PCB via wirebonding, as shown in Figure 3(b).

In I-V measurements of the fabricated PD arrays, we used a white light source with 150 W powers. I-V curves of 100 µm x 100 µm size and 1 µm thick SG-PDs are compared with respect to different L values in illuminated (ON) and dark states (OFF) and illustrated in Figure 4(a). Dark current and the saturation currents of the devices are in the order of 0.1 nA and 10 nA at -2V, respectively, and those do not depend on the L value. Obtained sensitivity is about 200. Moreover, the ideality factor of the lateral PIN depends on L. While intrinsic area length increases, the I-V characteristic of SG-PDs deviates from ideal. As seen in the figure, increasing intrinsic area length results in photocurrent reduction at forward bias mode while the sensitivity stays same.

Dark state I-V curves of SG-photodiodes are compared in Figure 4(b). Sample array sizes are 100 µm x 100 µm, 250 µm x 250 µm and 500 µm x 500 µm, while the intrinsic region length L was fixed at 2 µm. PD dark current in both forward and reverse linearly increases with array size. This figure shows that, we are able to scale down the PD array size further, so that number of detector pixel can be increased.



(a) (b)

Figure 4 (a) I-V curve comparison of 1 µm thick SG-PDs. Sample intrinsic region sizes are: 1 µm, 1.5 µm and 2 µm. Sizes of the PD arrays are 100 µm X 100 µm. (b) Dark current comparison of 1 µm thick SG-PDs with respect to array size. Sample array sizes are: 100 µm X 100 µm, 250 µm X 250 µm and 500 µm X 500 µm. Intrinsic region length is 2 µm.

Figure 5(a) shows I-V curves of the lateral photodiodes with 100 µm x 100 µm array size and 1 µm intrinsic region length. It shows that dark current under reverse bias is the same for those diodes. Photo-generated current of SOI- and SG-PDs (1 µm thick) are almost the same level, giving the light sensitivity of 260 and 230, respectively. However, 1 µm a-Si photodiodes have a very low value (less than 10) due to the dense defects. SG and c-Si photodiodes reach higher photocurrent values than a-Si photodiodes at forward bias mode. In comparison to the 1 µm thick SG-PDs, the 340 nm thick SOI-PDs reaches slightly higher photocurrent at forward bias probably due to slightly higher mobility of the SOI. However, 250 nm thick SG-PDs have a higher photocurrent than the SOI-PDs.

The SG-TFTs were fabricated in 250 nm thick crystallized silicon layer. Id-Vg characteristics of SG-NMOS and PMOS TFTs are presented in Figure **5**(b). Gate length (L_g) and width are 1.5 µm and 4 µm, respectively. Field effect mobility was derived from the linear region at drain voltage Vd of 200mV. Mobility, subthreshold swing and threshold voltage values of

the sample SG-TFT and SOI-TFT devices are shown in Table **1**. Those values correspond well with our previous report [6,7] and show that SG-TFT mobility is as high as the silicon-on-insulator (SOI) counterpart.

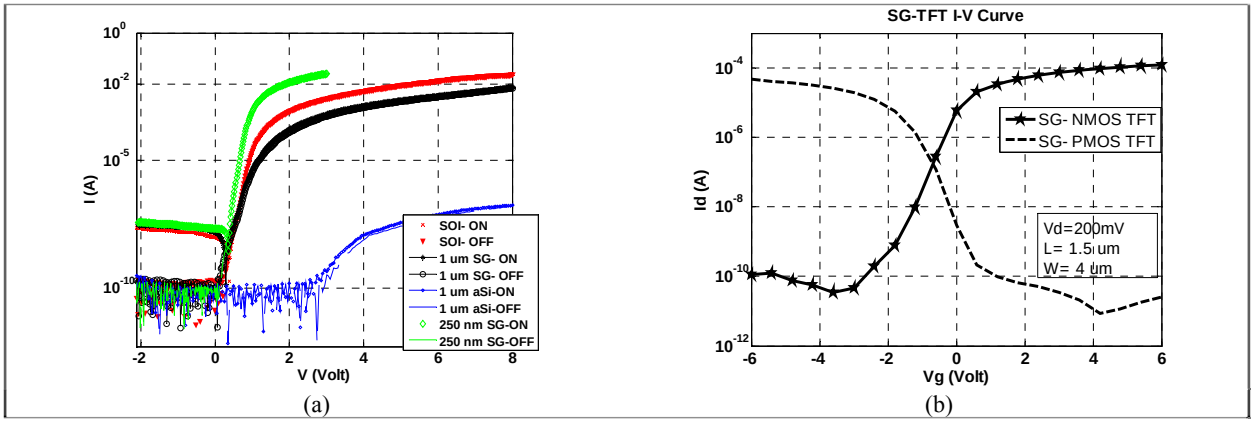


Figure 5 (a) I-V curve comparison of PD arrays which fabricated in c-Si (340 nm), a-Si (1 µm) and SG-Si (250 nm and 1 µm) layers. (b) Id-Vg curve of fabricated SG N- and PMOS TFTs in 250 nm crystallized silicon layer.

Table 1 Measured mobility, subthreshold swing and threshold voltage values in average of the SG- and SOI-TFTs.

	SG NMOS-TFT (L_g=1.5 µm)	SG PMOS-TFT (L_g=1.5 µm)	SOI NMOS-TFT (L_g=2 µm)	SOI PMOS-TFT (L_g=2 µm)
Mobility (cm^2/Vs)	526	253	460	220
V_{th} (V)	-0.3	-0.5	-0.2	0.6
S (V/dec)	0.4	0.37	0.175	0.2

4. CONCLUSION

SG-photodiode arrays and SG-TFTs were designed and fabricated to develop a large area and low dose X-ray image sensor. Devices were fabricated in 2D-location controlled single grains. PD array size and intrinsic region length were varied and the electrical measurement results were presented. Dark current of 100 µm x 100 µm size arrays are on the order of 0.1 nA for SG-photodiodes with 1 µm, 1.5 µm and 2 µm intrinsic region length and degrades in larger arrays. The sensitivity of the SG-PDs is higher than 200. Mobility of the SG-NMOS and PMOS transistors are 526 cm^2/Vs and 253 cm^2/Vs, respectively and comparable with SOI-TFT. Due to high mobility of SG-TFTs and high sensivity of SG-PDs, c-Si TFTs in X-ray image sensors can be substituted by crystallized silicon layer fabricated using location controlled µ-Czochralski technique.

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