R45: A 300mm Wafer-Size CMOS Image Sensor for Low-Light-Level Imaging

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Abstract

In this paper, we describe the architecture of a wafer size CMOS image sensor with on-chip RGB color filter enabling to enlarge the size of the large format sensor while maintaining good signal quality. This sensor has programmable in-pixel voltage gain amplifier and column level differential readout circuitry. A 202×205mm^2, 1.6Mpixel, 100fps CMOS image sensor is fabricated on a 300mm wafer in 0.25μm 1P3M CMOS. The diagonal of the sensor is 1.5× larger than that of the conventional wafer-size imager on a 200mm wafer. In addition, the differential readout circuitry on the column signal path ensures tolerance to common mode noise and the drift of power/ground voltage.

Introduction

A high frame rate and high sensitivity image sensor gives us a new form of vision such as the security camera operating under moonlight and real-time astronomical observation beyond the ability of human vision. To enlarge the size of a pixel and a sensor is one approach to increase the sensitivity. The image sensors commonly comprise thin film transistors and photodiodes (PDs) on amorphous silicon. The capabilities of the amorphous silicon sensors, however, are insufficient due to the low carrier mobility of the TFTs. Recently several large-format CCDs [1] and CMOS image sensors [2] [3] have been developed on crystal silicon wafers for faster readout speed, reduced image lag, high sensitivity and reduced noise. However, the larger size of a sensor chip leads to larger parasitic resistance and capacitance of signal and power line. These parasitics impede the high frame rate readout for two reasons: (1) the signal line parasitics slow the signal settling (2) the parasitic resistance of power line causes power/ground drift depending on the intensity of subject brightness, and result in inter-pixel crosstalk read out at the same timing. It has been an obstacle to accelerate the throughput of the large-format CMOS image sensor.

Design and Implementation

A. Chip Overview

Figure 1 shows a conceptual view of the sensor. The chip is formed by stitching 3 fragments named block A, B and C because the area of the chip is larger than the maximum field of view of existing steppers. Stitching one block of A, nineteen blocks of B and one block of C yields one subarray. The subarray includes pixels of 128 columns × 1248 rows, a pair of output buffers for reset and integrated signals, a horizontal scanning circuit (HSC), and a vertical scanning circuit (VSC). Ten subarrays compose the wafer-size image sensor. The VSC is embedded in the array of pixels, therefore the pixel pitch between adjacent pixels at the border of subarrays is the same as that in the subarray.

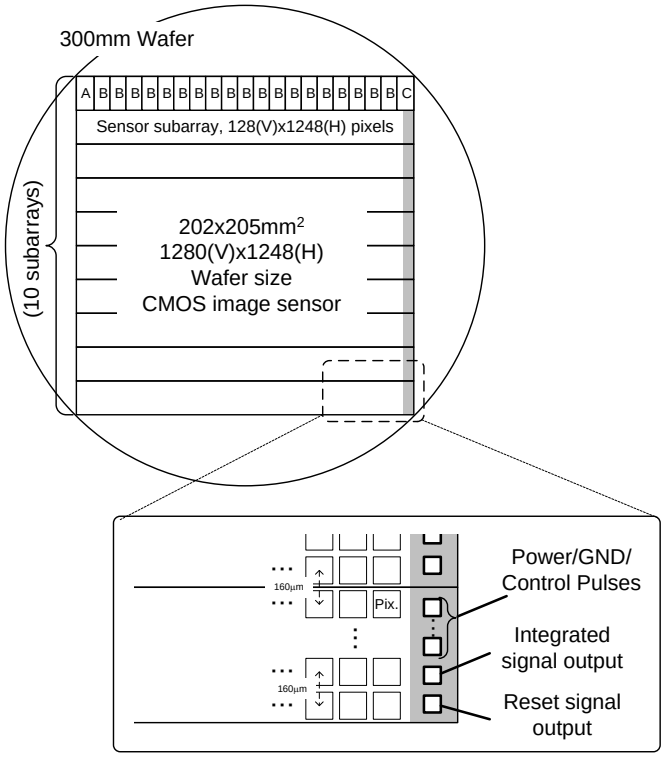

Figure 1: Concept view of the wafer size image sensor.

In addition, the sensor can be arranged to 2-by-N tiles to form larger image area because there is no margin both on the edge of block A and on the long sides of the subarray. In order to realize color imaging, RGB Bayer color filter is formed on the wafer, as illustrated in figure 2. The color filter is fabricated by stitching method same as the wafer fabrication.

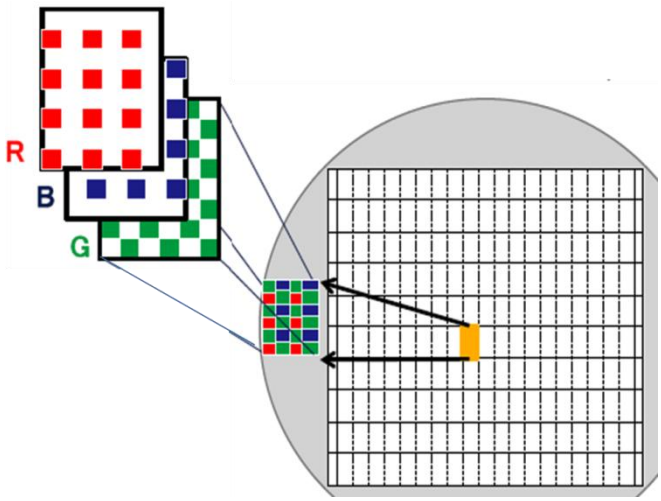

Figure 2: Concept view of on-chip color filter layout.

B. Differential Column-Signal Readout Circuitry

Figure 3 shows the layout concept of a pixel array. In the array, a row is flipped horizontally onto its adjacent rows, which yields a space between every 2 rows. Unit cells of both the VSC and the HSC are placed at the spaces between rows. Repeaters are inserted between unit cells of the VSC to regenerate a vertical shift pulse. The body of the PD is fully depleted, and connected with a conductor at its center.

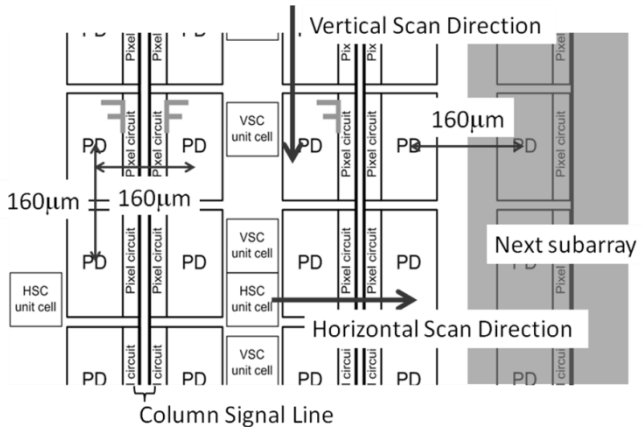

Figure 3: Pixel and scan circuit layout.

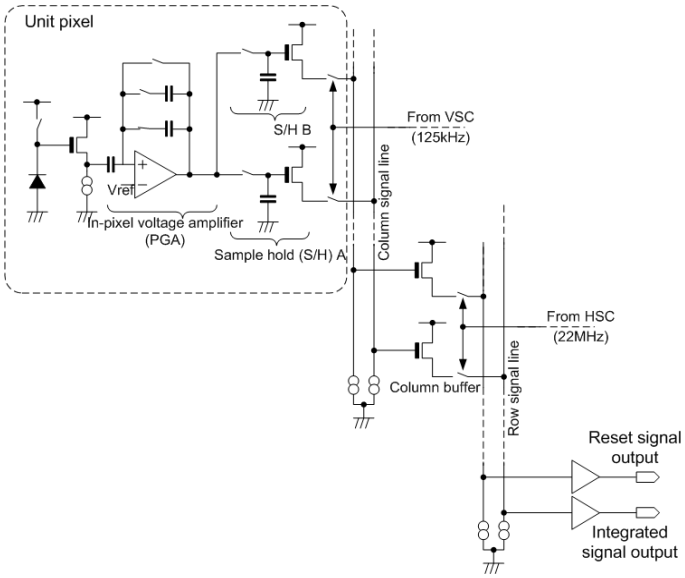

Figure 4: Schematic view of the signal path from a PD to reset/integrated signal output terminals.

Figure 4 is a schematic view of the signal path from a PD to output terminals. A unit pixel consists of a PD, a source follower (SF), in pixel voltage amplifier (PGA), and 2 S/H amplifiers for reset and integrated signals. The PGA is an inverting voltage amplifier with capacitive feedback. Its gain is configured to 0, 18, or 24dB, which enables a maximum conversion gain of 318µV/e^-. The PGA consists of an nMOS-input single-staged operational amplifier with 40dB DC open-loop gain.

C. Chip Operation

Figure 5 describes its operation as follows: (1) signal integration, (2) holding an integrated signal at the S/H A, (3) resetting the PGA, (4) resetting the PD while resetting the PGA, and (5) holding the reset signal. All pixels are stimulated at the same time, achieving synchronous shutter operation. The reset signal and the integrated signal held at the S/Hs do not contain kT/C noise of the PD because it is filtered out by the PGA. The kT/C noise generated when resetting the PGA, however, cannot be canceled. The reset signal and the integrated signal from a pixel are read out to a pair of column lines of 200mm long each, and transmitted simultaneously to a column buffer within a period of 2.0µs. Unlike a conventional column signal line that transmits reset and integrated signals sequentially, the differential signal line cancels the drift of ground/power line due to insufficient settling time while transferring high-amplitude integrated signals. It enables almost the same column read time as that of a small-format CMOS image sensor.

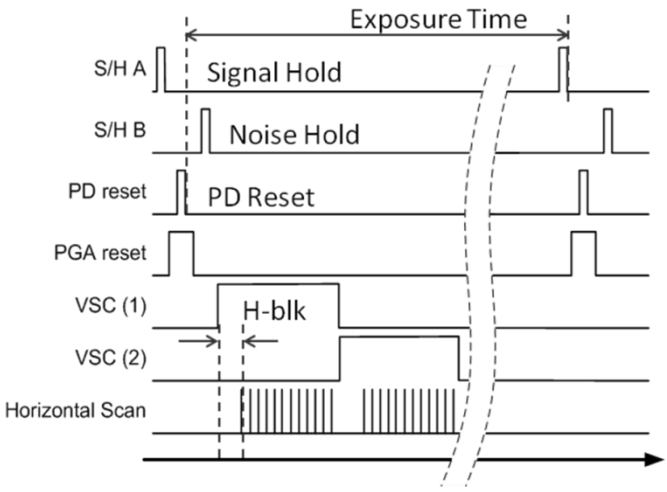

Figure 5: Timing diagram.

A synchronous shutter operation is important to remove the effect of Vref drift at the PGA. The change of Vref multiplied by the gain appears on the output of the PGA. If the sensor is in rolling-shutter operation, signals of the pixel obtained from a different row i.e. at a different time have a large difference due to the Vref drift. It results in line noise flickering in the horizontal direction. Under synchronous operation, the change of Vref affects the entire pixel identically, which can be removed by frame-offset compensation using all the vertical optical black pixels of more than one row.

The subject-dependent crosstalk of conventional readout circuitry employing single-end signal readout and that of the differential signal readout are compared in Figure 6. Although the standby periods of 2μsec are given both reset and integrated signal for single-end readout, the crosstalk is 50× larger than that of the differential readout. The crosstalk results in 0.1% signal change for 2.0V signal saturation and not acceptable for high-quality imaging application. The 0.002% crosstalk of the differential readout is below detection limit in 8-bit image after a gamma correction.

	crosstalk [V]	crosstalk [%]
Conventional circuit	1.9×10^{-3}	0.095
Differential circuit	3.7×10^{-5}	0.002

Figure 6: Comparison of crosstalk between two readout circuit.

Results

Figure 7 summarizes the specifications and performance of the sensor. Due to high conversion gain, measured full-well capacity is limited to 77ke$^-$ at 1× pixel gain. Minimum random noise of 13e$^-_{rms}$ is measured at 16× pixel gain. A conversion gain of 318μV/e$^-$, and a voltage sensitivity of 7.8kV/lx-s are obtained with a 2856k light source and IR cut filter. Electron sensitivity is 25Me$^-$/lx-s. Maximum power consumption is 320mW per subarray for a total of 3.2W. The maximum power occurs during a V-blanking period when the SFs and the PGAs of all the pixels are activated. The average power is very small because the two amplifiers above are in power-down mode when the data are read out from S/H amplifiers.

Process	0.25μm 1P3M CMOS
Chip size	202(H)mm x205(V)mm
Pixel size	160μm x 160μm
Number of total pixels	1280(H) x 1248(V)
Number of effective pixels	1280(H) x 1128(V)
Maximum Frame rate	100 fps
Pixel rate	220MHz (22MHz x 10ch)
Pixel gain setting	0[dB] (x1), 18[dB] (x8), 24[dB] (x16)
Conversion gain @ x16	318 μV/e$^-$
Sensitivity @ x16	7800 V/lx/s
	25Me$^-$/lx/s
Full well capacity @ x1	77000e$^-$
Random noise	13 e$^-_{rms}$
Maximum power consumption	3.2W

Figure 7: Specifications and performance of the sensor.

Figure 8 is a night scene taken using the presented chip along with F6.8 lens under 0.1 lx ambient light and 20ms exposure time. Neither low-pass filtering nor other filtering to reduce random noise is employed. Line defect is not found. Pixel defects are not compensated. No visible crosstalk is seen around dark area adjacent to the bright area. It shows that the subject-dependent crosstalk is sufficiently suppressed. The wafer-size CMOS sensor enables to identify eighth-magnitude stars of the starry heavens in a 60fps movie. Figure 9 is real-time astronomy observation. We aimed at Orion Nebula, using schmit camera, having aperture of F3.1. This shot is made possible by cooperation of Kiso observatory of the University of Tokyo.

In order to remove the offset variation of column buffers, the image was compensated by the column offset data generated by projecting the vertical optical black pixel data of the image itself. To remove the offset voltage variation of S/H amplifiers, the averaged dark image, which was prepared beforehand, was subtracted from the raw image.

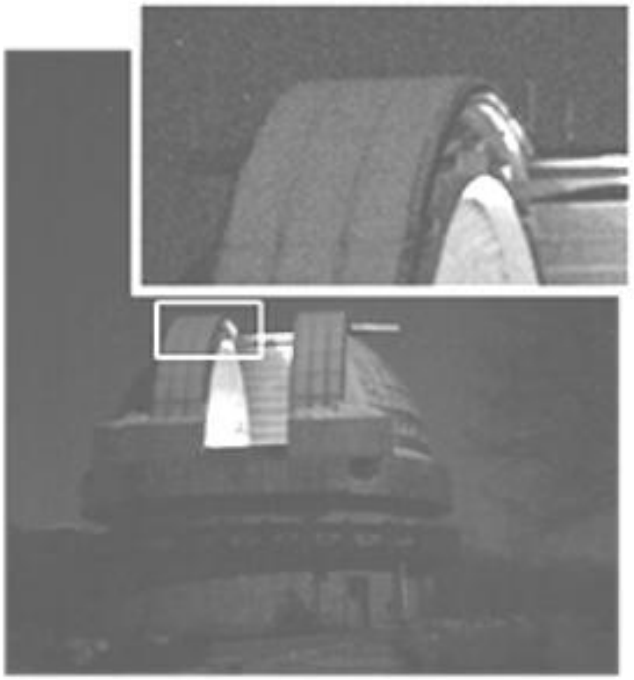

Figure 8: Night scene taken using the presented chip.

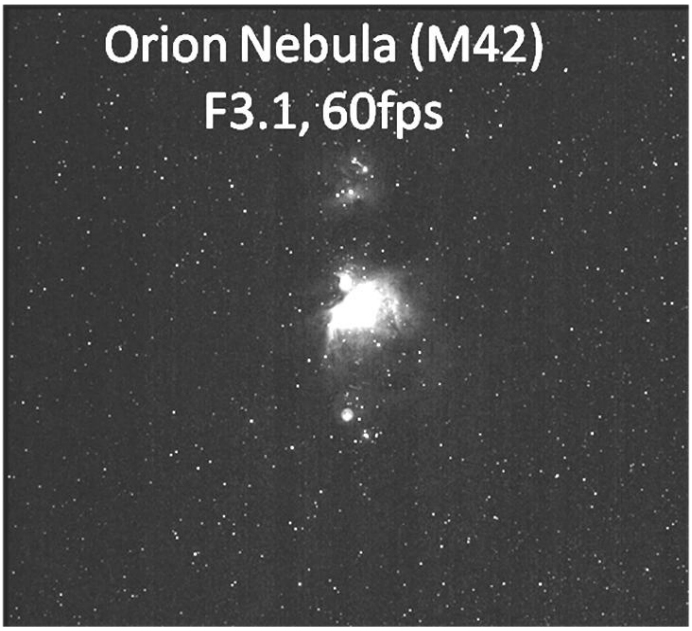

Figure 9: Astronomy observation.

Figure 10 shows photographs of the sensor with RGB color filter on a 300mm wafer and a package. The lines between subarrays are visible, implying irregularity on the chip. The image taken by the sensor, however, is not affected by the irregularity because the size of PD and the pixel pitch, i.e. the sensitivity and the spatial frequency are kept constant among all the pixels.

Acknowledgement

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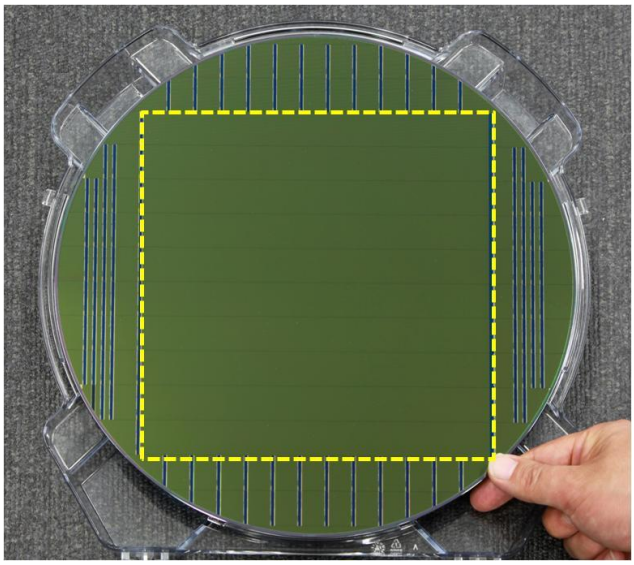

Figure 10: Photograph of the wafer and the packaged chip.

References

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[3] R. Reshef, et al., "Large-Format Medical X-Ray CMOS Image Sensor for High Resolution High Frame Rate Applications," International Image Sensor Workshop, June 2009.