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A 32x32 SPAD Pixel Array with Nanosecond Gating and Analog Readout

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ABSTRACT

CMOS Single Photon Avalanche Diode (SPAD) arrays are emerging as appealing solid-state detectors in imaging applications where high sensitivity and timing resolution are required. In this work, a 32x32-pixel array where SPAD digital output is processed in the analog domain in a 12-transistor pixel is presented. A 25μm pixel pitch with a remarkable 20.8% fill factor was achieved thanks to a very compact pixel electronics, and gating pulse widths down to 1.1ns FWHM at 80MHz repetition rate were demonstrated.

INTRODUCTION

Among solid-state detectors, SPADs offer unique features such as single photon detection capabilities and picosecond timing resolution [1], which are jointly present only in photomultipliers and micro-channel plates. A rugged and cost-effective solid-state alternative to these detectors would be highly desirable in application fields such as fluorescence imaging and time-of-flight optical ranging. Although the CMOS integration of SPADs was demonstrated several years ago, the design of effective SPAD-based pixels for imaging applications still presents many challenges: since each SPAD produces a digital pulse for every detected photon, a complex electronic circuit should be implemented at the pixel level to perform data storage while preserving timing information in a small area and with a reasonable fill factor. SPAD-based image sensors presented so far [2-5], despite offering additional functionalities and excellent timing resolutions with respect to standard pixels, feature fill factors in the order of some percent, which spoil their overall efficiency and are difficult to recover by means of optical concentrator arrays.

In this work, a compact SPAD-based pixel is presented, which includes an analog gated counter in a 25μm pitch with a state-of-the art fill factor of 20.8%. A 32x32 pixel array was implemented in a 0.35μm High Voltage CMOS technology together with a digital PLL for on-chip nanosecond gating signal generation.

DESIGN

The all-NMOS 12-transistor pixel presented here includes a passively quenched SPAD, an inverter working as a digital comparator, a gating circuit and an analog counter (Fig. 1). A compact pixel layout was possible because both the SPADs and the ptub including the n-type MOSFETs were integrated in the same deep-ntub, as shown in Fig. 2.

The pixel working principle is illustrated in Fig. 3. A 5V quenching transistor (M1) determines the recharge time of the SPAD after each avalanche event. Transistor M2 is used to clamp the voltage pulse at node B, allowing the use of 3.3-V transistors in the next part of the circuit. In this way, excess bias voltages larger than 3.3V can be used to bias the SPAD without damaging the inverter. Each avalanche event generates a positive pulse at node B and a negative and slightly delayed pulse at node C, after passing through the inverter formed by M4 and M5. Transistor M3 was included for testing purposes to generate an electrical pulse simulating an avalanche event. If the event occurs inside the time window WIN, a negative picosecond voltage pulse is generated by the gating circuit, formed by transistors M6, M7 and M8. This pulse removes a small charge packet from the integration capacitor through transistor M9, generating a voltage step ΔV at node E (Fig. 3b). If the event occurs outside the gating window WIN, the pulse is not generated and the event is not counted (Fig. 3a). The value of ΔV can be set through the reference voltage V_{bAC}. The final part of the pixel is composed of a reset transistor (M10), a source follower (M11) and a select switch (M12) as in a standard 3T active pixel. Therefore, the pixel output can be read-out as in a common active pixel image sensor.

A digital PLL working at a maximum frequency of 40MHz was also implemented on-chip for gating signal (WIN) generation. Fast gating signals can be also provided externally for maximum flexibility. The floorplan and the layout of the sensor are shown in Fig. 4 and 5 respectively.

CHARACTERIZATION

A typical pixel output voltage oscilloscope trace, where each counted photon corresponds to a voltage step ΔV, is shown in Fig. 6. The output voltage histogram, obtained from 10000 acquisitions of a single pixel, is shown in Fig. 7. The histogram shows that single photons can be resolved and therefore shot noise limited operation is maintained even if the pixel is operating in the analog domain. An 11% non-uniformity in the voltage step ΔV among the pixels is

present, but can be mostly compensated with a pixel-by-pixel calibration. To confirm the effectiveness of the correction procedure, a histogram of all the pixels in the array after calibration has been collected and is shown in Figure 8. It can be noticed that, although the resolution is slightly worsened with respect to the histogram in Fig. 7, single photon events can be clearly discriminated and shot noise limited operation is maintained.

The main source of noise in this sensor is represented by the dark count rate (DCR) of the SPAD. The DCR distribution measured at 4V excess bias voltage is shown in Fig. 9 together with a DCR map, evidencing a typical dark count of 500Hz and 15% of bad pixels. A complete characterization of SPADs fabricated in the same technology with a slightly larger area had already been reported in previous publications [6,7].

This sensor was mainly intended for time-resolved sensing applications, exploiting the excellent timing resolution offered by SPAD detectors. The gating performance of the sensor was characterized using a picosecond pulsed laser (PicoQuant, λ=470nm, FWHM = 70ps) to illuminate the sensor and recording the average sensor output as a function of time delay between gating signal and laser signal. Gating windows with variable width were generated by the on-chip PLL running at 20MHz, while variable delays were set using an external pattern generator (HP8110A). The average sensor output is shown in Fig. 10 for three different gate widths. As can be observed, the minimum gating width is around 1ns, which is suited for most of the common fluorescent tags used in biology.

Finally, a fluorescence measurement of a CdSe/ZnS Quantum-Dot (Evident Technologies) reference slide was performed. A collection optics including a high numerical aperture aspheric lens and a high pass optical filter (500nm) was used to form an image of the fluorescent sample on the sensor focal plane. The fluorescence was excited using the picosecond laser previously mentioned, collimated into a Gaussian beam with 0.7 mm FWHM diameter, and using oblique incidence to avoid the strong excitation signal to be directly incident on the collection optics. Gate width was set to 1.9ns and several measurements with 2ns time shifts were performed in order to measure the time decay curve of the fluorescent emission. The fluorescent decay curve averaged on all the pixels is shown in Fig. 11. An intensity and a lifetime image acquired with the sensor are shown in the insets.

Finally, the main sensor characteristics are summarized in Fig. 12.

CONCLUSION

A SPAD-based image sensor featuring a compact analog pixel design was demonstrated. The proposed pixel include a fast gating circuit and an analog counter for photon time discrimination and accumulation. Analog domain processing combined with time-gating technique allowed the realization of a compact 25μm pixel with a remarkable 20.8% fill factor. A standard CIS readout chain can be used to process the pixel analog output, thus taking benefit of the consolidated techniques developed for standard CMOS image sensors. Porting the proposed analog approach to more advanced technology nodes could likely enable the realization of high-resolution single-photon pixel arrays available for a variety of applications ranging from advanced microscopy and time-of-flight range imaging to night vision and high speed imaging.

ACKNOWLEDGMENT

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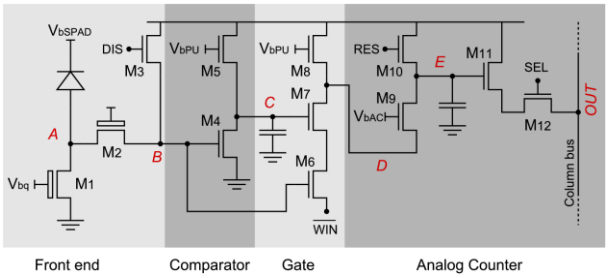

Figure 1. Pixel schematic diagram.

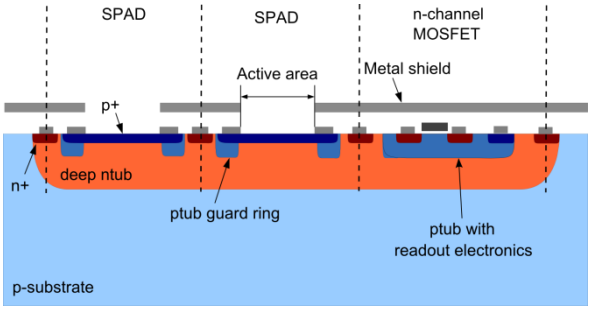

Figure 2. Pixel-array cross section.

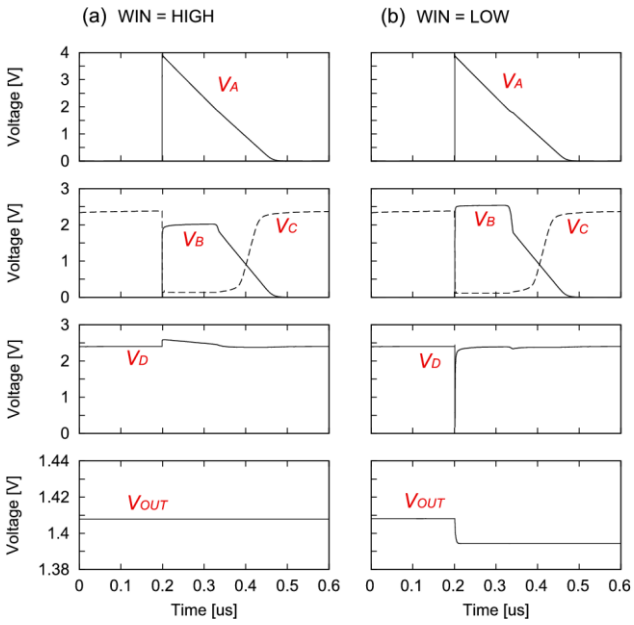

Figure 3. Pixel transient simulations when the photon detection occurs (a) outside the gating window (b) inside the gating window.

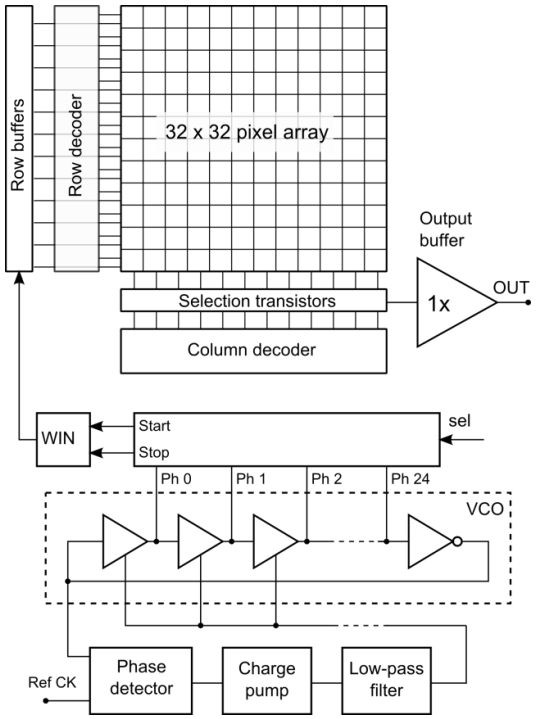

Figure 4. Sensor architecture.

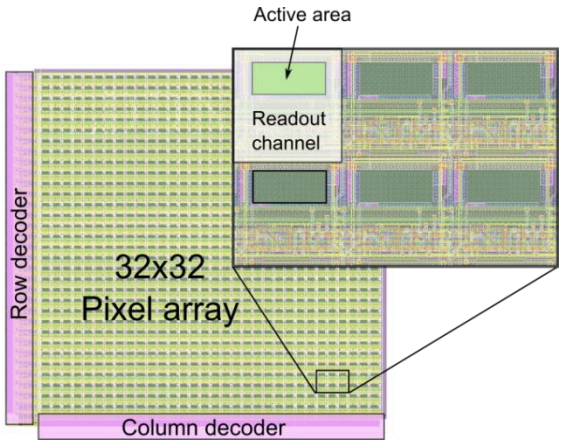

Figure 5. Sensor and pixel layout.

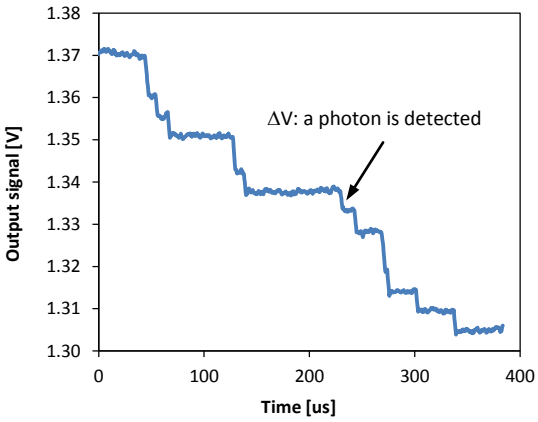

Figure 6. Pixel output voltage under illumination.

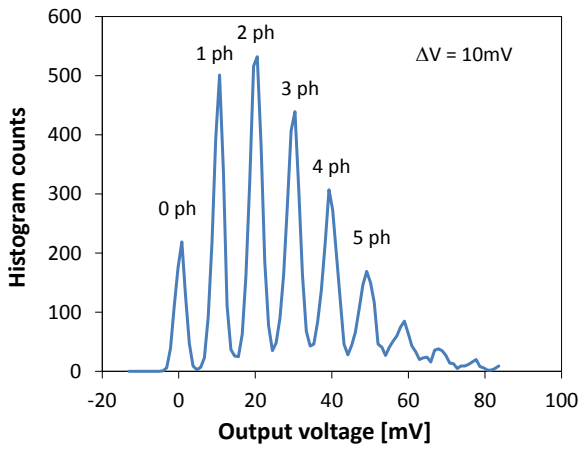

Figure 7. Pixel output voltage histogram (with 10000 acquisitions).

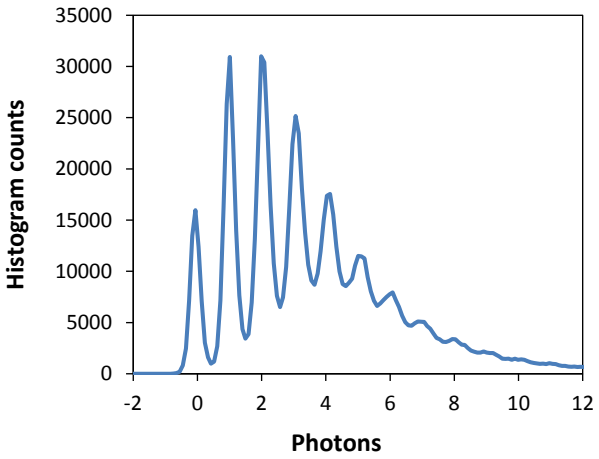

Figure 8. Output histogram of the whole array after calibration (with 1000 acquisitions).

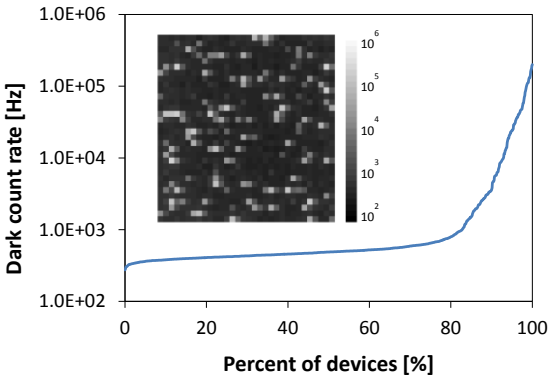

Figure 9. Dark count rate distribution and dark count rate map of the array.

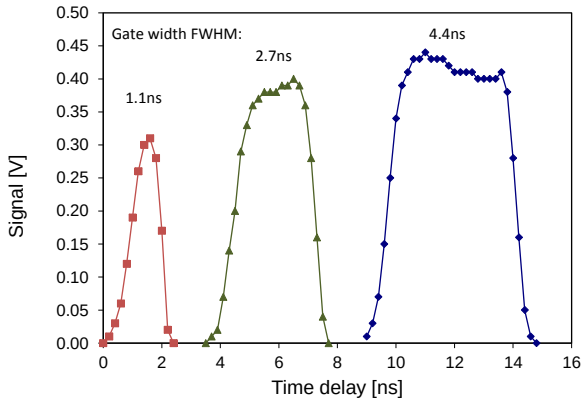

Figure 10. Characterization of time-gating performance of the sensor: convolution between gating window and 70ps FWHM pulsed blue laser (470nm).

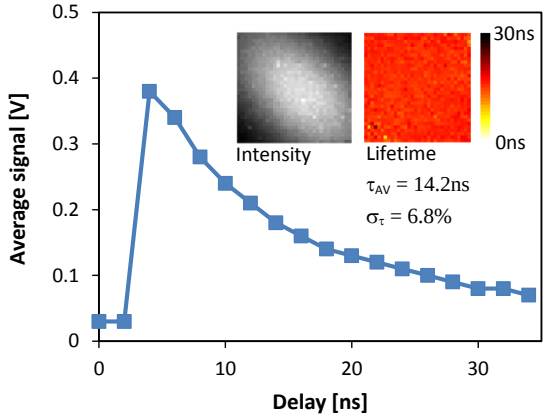

Figure 11. Average fluorescence signal from a Quantum Dot reference slide as a function of gate delay (gate width = 1.9ns). In the inset: fluorescence intensity and lifetime images of the slide region hit by the collimated excitation laser (Ø =0.7mm).

Pixel number	32 x 32
Pixel size	25um
Fill Factor	20.8%
Transistors per pixel	12
Output voltage range	1.5V
Time-gate width	> 1ns
Maximum gating frequency	40MHz with on-chip PLL, 80MHz with external delay generation
Current consumption	Sensor: 7mA @ 180 fps PLL: 4 mA @ 20MHz

Figure 12. Summary of the sensor main characteristics.