Single-Photon Avalanche Diodes in 90nm CMOS imaging technology with sub-1Hz Median Dark Count Rate

Eric A. G. Webster, Justin A. Richardson, Lindsay A. Grant, Robert K. Henderson

***Abstract*—A family of Single-Photon Avalanche Diodes (SPADs) is reported in 90nm CMOS imaging technology with active diameters of 8, 4 and 2µm. An imaging-specific low doped *p*-well is used to create a junction with relatively high breakdown voltage (≈17.5V) to reduce tunnelling and lower the DCR. The devices achieve: a peak photon detection efficiency of ≈33% at 450nm and a spectral response comparable to 130nm SPADs; improving median DCR as the diameter is reduced of 132, 5, and 0.8Hz, respectively, at room temperature; improving timing jitters of ≈130, ≈92, and ≈78ps FWHM, respectively; and a relatively low afterpulsing of ≈3.725% for the 4µm device.**

I. Introduction

ARRAYS of Single-Photon Avalanche Diodes (SPADs) with on-chip CMOS readout electronics are providing new capabilities in low light level, time correlated imaging. Large format SPAD sensors for fluorescence lifetime imaging (FLIM), positron emission tomography (PET) [1] and 3D cameras [2] are beginning to challenge commercially-available systems based on sensitive photo multiplier tubes (PMTs) or charge coupled device (CCD) sensors. Further advances in the resolution and sensitivity of these SPAD imagers, demand scaled detectors with low median dark count rate (DCR), low pixel defectivity and high photon detection efficiency (PDE). The use of advanced nano-scale CMOS processes is mandatory in order to shrink pixel pitch and provide high speed processing electronics. As a result, a number of SPAD structures have recently been demonstrated in 0.18µm, 130nm and 90nm CMOS process generations [3-5].

The main challenge of scaling SPADs into nano-scale CMOS processes is in choosing an appropriate multiplication junction and guard ring. The traditional *p*+-*n*-well SPAD junction with a *p*-well guard ring was first implemented by Rochas [6] at the 0.8µm node, and followed by others in 0.35µm [2] and 0.18µm [3] processes. However, this SPAD construction was found to be no longer successful at the 130nm node [7] due to high noise rates which were dominated by band-to-band tunnelling. Indeed, a similar SPAD structure implemented in 90nm technology yielded hundreds of kilohertz DCR at low excess bias [5], indicating the unsuitability of SPAD constructions based on *n*+/*p*+ implants. The high noise evident at nanometre nodes is due to the increasing concentration of the source/drain implants required to maintain MOSFET performance as transistor geometry is shrunk. The increased implant dose lowers the breakdown voltage of SPADs made from this junction, and correspondingly reduces the junction width, leading to an exponential increase in band-to-band tunnelling.

The high noise rates resulting from SPADs based on *n*+/*p*+ implants therefore led to the development of a SPAD with the multiplication junction based on the lower doped well implants in 130nm CMOS with a guard ring formed by preventing *p*-well formation [8]. This new structure successfully raised the breakdown voltage and reduced the dark count rate.

In this paper we present a family of SPADs implemented in a 90nm CMOS image sensor technology which achieve the lowest median DCR yet reported. This low noise is achieved by building on the improved performance realised from *p*-well-based SPADs at 130nm. We demonstrate that the resulting devices are easily scaled from 8–2µm in diameter with improving DCR, jitter and yield properties making them highly suited to future high resolution single photon sensor arrays.

II. Device Structure

The SPAD structures, passive quench components, and read-out electronics are fully integrated in STMicroelectronics's 90nm CMOS imaging technology. The implemented devices are of identical construction to that reported in [8]. The anode is formed with an imaging-specific low doped *p*-well available for formation of pinned-photodiodes with a *p*+ contact implant on top. The guard ring is formed by inhibiting the normal procedure of implanting either *p*-well or *n*-well above deep *n*-well (DNW) by use of an implant stop layer. A 'virtual' guard ring structure is created where the graded doping profile of the retrograde deep *n*-well cathode implant encourages breakdown in the central active region rather than at the device periphery. STI is spaced from the edge of *p*-well

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This work was supported by The University of Edinburgh & ST Microelectronics (R&D) Ltd., Edinburgh, U.K.

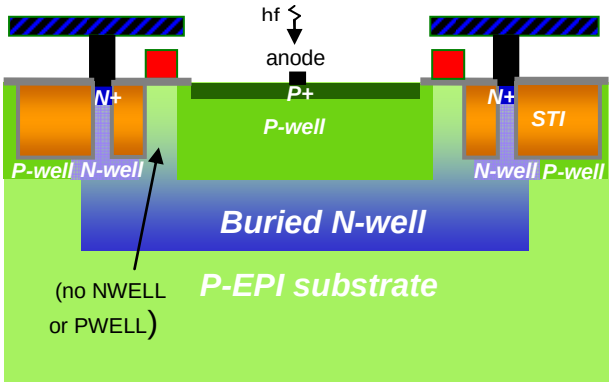

Fig. 1. **Device structure**

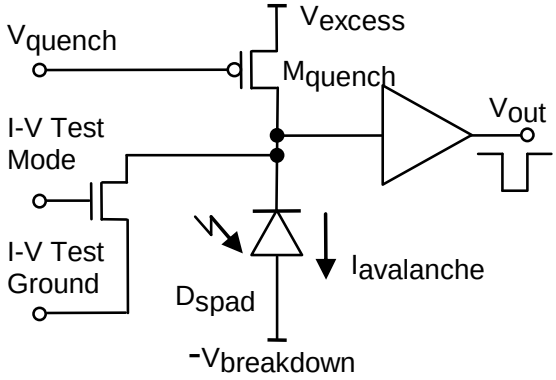

Fig. 3. **SPAD test circuit which enables I-V characterisation as well as passive quench Geiger-mode operation.**

by drawing a poly thin-oxide spacer ring coincident with the *p*-well block. A cross-section of the SPAD is illustrated in Fig. 1

The different SPAD diameters are drawn whilst maintaining constant *p*-well to STI guard ring spacing of 1µm and are illustrated in device micrographs of the 8µm, 4µm and 2µm structures shown in Fig. 2. A passive quench PMOS transistor and readout buffer circuit are integrated on chip next to each SPAD. This circuit enables I-V and Geiger-mode characterisation of each device and is illustrated in Fig. 3.

III. Results

The I-V characteristics of typical 2, 4 and 8µm devices are plotted in Fig. 4 and exhibit abrupt breakdown at 17.56V, 17.47V, and 17.37V, respectively. Interestingly, the breakdown voltage (V_{BD}) is observed to decrease as device size increases. These breakdown voltages are relatively high for a 90nm process as we discovered that the standard *p*-well required for small geometry MOS transistors yielded a breakdown voltage of only ≈11.5V compared with the ≈14.4V for the same junction in 130nm, indicating the degree to which dose-scaling occurs.

The Photon Detection Efficiency (PDE) measured for the 8µm device at 1.2V excess bias is illustrated in Fig. 5 with the 130nm results at the same excess bias plotted for comparison. The peak PDE of ≈33% is achieved at 450nm which is a shorter wavelength than the ≈34.5% at 470nm achieved in 130nm [8]. Moreover, a slightly higher PDE is also achieved at short wavelengths in the 90nm process, suggesting a shallower junction. A different diffraction and interference pattern is also evident between the two process nodes which is consistent with differing dielectric stacks. The high PDE achieved at short wavelengths is well suited to PET applications [1].

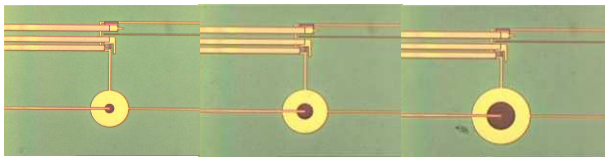

Fig. 2. **2µm, 4µm and 8µm diameter device micrographs (left to right). The SPAD test circuit (Fig. 3) is visible above each device.**

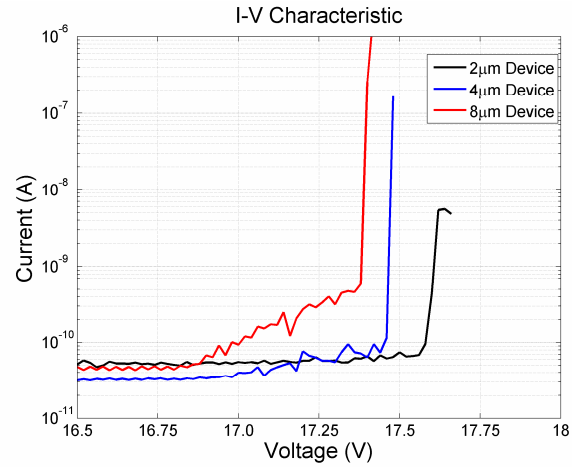

Fig. 4. **I-V characteristics for 2µm, 4µm and 8µm diameter SPADs**

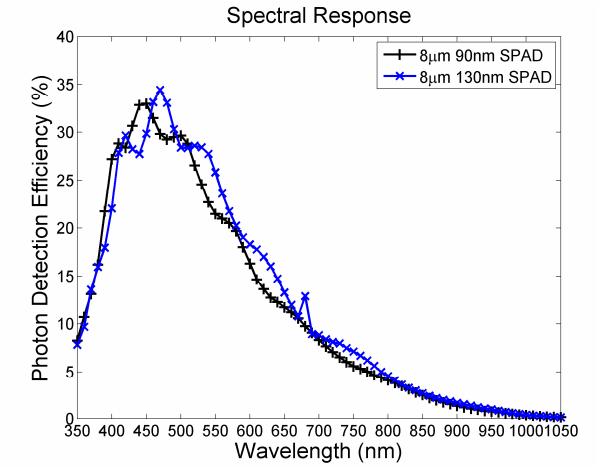

Fig. 5. **Photon detection efficiency of the 8µm device operating in Geiger-mode at 1.2V excess bias (18.7V) and 150ns dead time. The PDE of [8], a 130nm CMOS SPAD, measured at the same time is plotted for comparison.**

The cumulative distribution of the DCR population for the 25 available devices of each device diameter is illustrated in Fig. 6. Devices which failed due to ESD damage are not included. The median DCR reduces from 132Hz to 0.8Hz as device diameter scales from 8µm to 2µm at a total bias voltage of 17.8V at 293K. Interestingly, the proportion of devices with close to the median DCR increases as the device diameter reduces. This is consistent with a model of localised traps being responsible for the high DCR devices, and the smaller the device volume, the lower the probability of finding a trap in the high field junction. This provides some justification for further scaling of SPAD geometries in advanced CMOS as improved yield can be expected with ≈70% of 2µm devices achieving less than 1Hz DCR.

Fig. 7 illustrates the DCR dependence on bias voltage

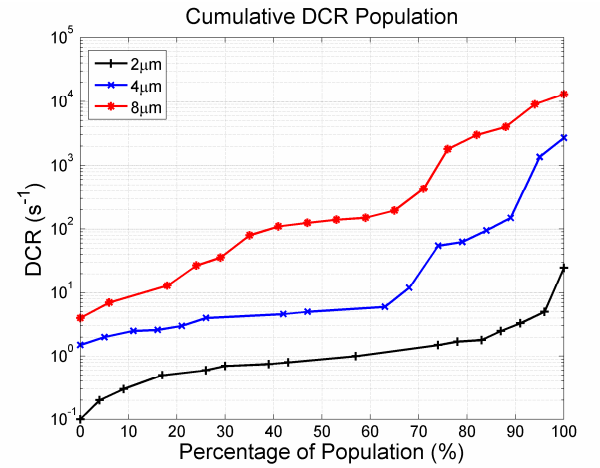

Fig. 6. **Cumulative DCR for population of 25 devices at 17.8V.**

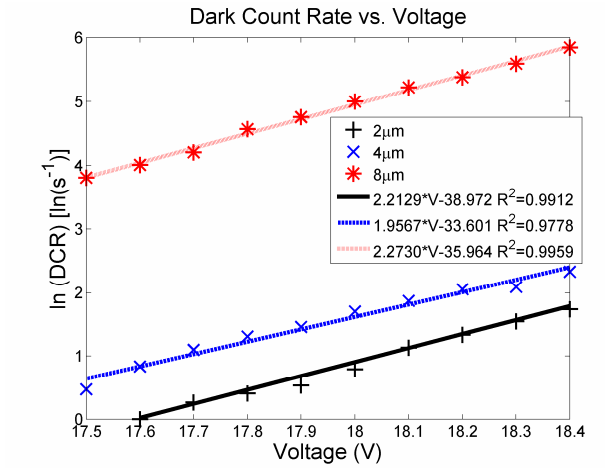

Fig. 7. **DCR vs. voltage for typical 2, 4 and 8μm diameter SPADs**

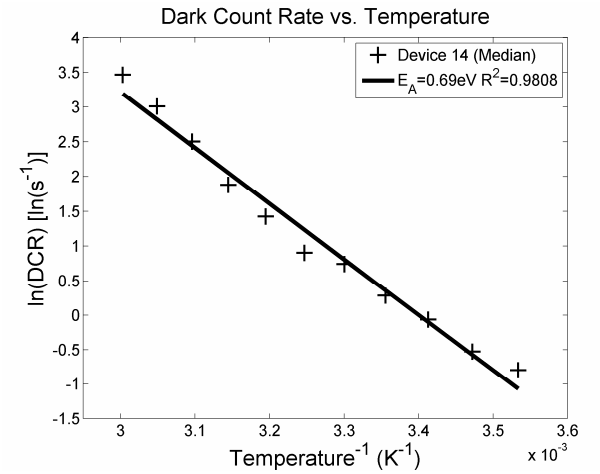

Fig. 8. **DCR vs. temperature for a median 2μm device.**

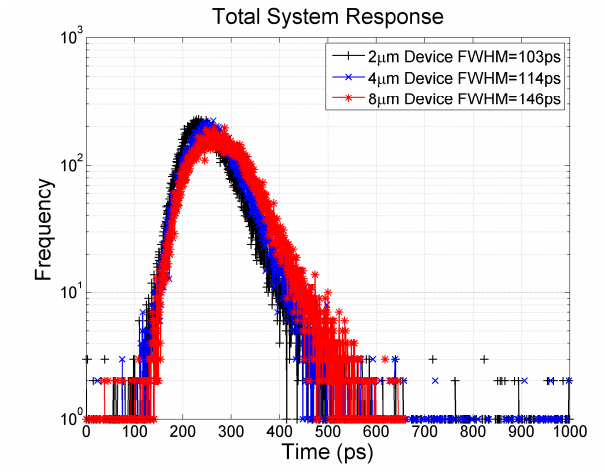

Fig. 9. **Timing jitter for 2, 4 and 8μm diameter SPADs at 17.8V.**

for median DCR devices of each size. The voltage gradient for each device diameter is similar and, combined with the yield apparent from Fig. 6, this suggests that median DCR devices do not suffer from DCR due to traps.

The exponential dependence of DCR on temperature for a median 2μm 0.8Hz device is illustrated in Fig. 8 on an Arrhenius plot. The resulting 0.69eV activation energy is consistent with thermal generation and diffusion currents. Compared to the results presented in [9], the activation energy suggests that band-to-band tunnelling is not the dominant DCR mechanism in these devices. This is consistent with a V_{BD} of around 17.5V, compared to [9] with a V_{BD} of ≈14.9V. Moreover, the median DCR is so low that this suggests that traps are not responsible for the obtained activation energy. These results highlight the importance of using a high breakdown voltage junction to achieve low noise. The temperature dependence of V_{BD} was evaluated as 13.1mV/K and was accounted for in the measurements.

The jitter of each detector was measured with a Picoquant LDH-D-C 470nm pulsed laser with a PDL800D driver. The laser was attenuated to avoid photon pile-up distorting the measurement. Fifty thousand breakdown events were accumulated and the results are plotted in Fig. 9 which includes the estimated ≈60ps laser and ≈30ps output buffer chain jitters. The results show that total timing resolution improves as the detector diameter is scaled from 8μm to 2μm from ≈130ps to ≈78ps FWHM

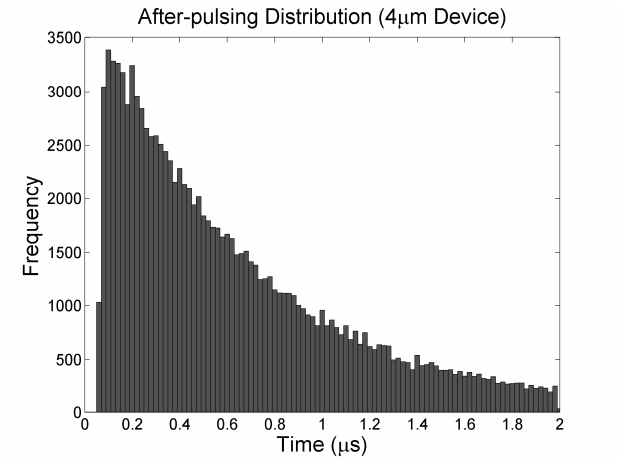

Fig. 10. **After-pulsing distribution for a 4μm diameter SPAD at 17.8V total bias illustrating 3.725% after-pulsing probability and a ≈330ns lifetime.**

by performing subtraction in quadrature. This is consistent with the lateral avalanche spreading theory proposed by Lacaita [10].

The after-pulsing of the 4μm device was measured by first determining the time-scale of the after-pulsing phenomenon by analysing the inter-arrival times of dark count events. The observation time was steadily reduced to more accurately observe the deviation from the ideal exponentially distributed inter-arrival times. It was found that the majority of after-pulsing was contained within 2μs of the primary pulse. With a median DCR of 5Hz, the

probability of two dark count events in 2µs is $\approx 1\times10^{-5}$ and therefore any secondary pulse probability higher than this would be due to after-pulsing.

The oscilloscope was set to measure the time between a primary pulse and a secondary pulse, if one occurred, and left to accumulate 3,042,472 primary pulses overnight. This yielded 113,335 secondary pulses, giving a total after-pulsing probability of 3.725%. This after-pulsing probability is significantly less than previously reported for 90nm SPADs [5]. The exponentially distributed after-pulsing probability obtained with this technique is illustrated in Fig. 10 showing a ≈330ns lifetime. Finally, Table I summarises the performance of all the devices.

IV. Conclusion

A family of SPADs was reported in 90nm CMOS imaging technology ranging from 2 to 8µm in size. The devices utilise relatively low doped well implants available in the imaging process to reverse the trend of reduced V_{BD} with process node shrink apparent from the literature to mitigate band-to-band tunnelling and achieve low DCR. The 2µm device is especially promising for future large scale SPAD integration as it achieves high yield and good timing performance.

The results suggest that the main impediment to future implementation of low DCR SPADs in more advanced nanometre processes is the reduced V_{BD} and high noise rate arising from low breakdown voltages resulting from the opposing objectives of MOSFET and SPAD design. A move to custom junctions in the future is therefore required to maintain noise performance because even the well doping concentrations start to become too high at nanometre nodes to form good low noise SPADs.

Acknowledgment

The authors would like to thank ST Microelectronics, Crolles, France, for fabricating the devices.

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TABLE I: SPAD Performance Summary

Metric	2µm	4µm	8µm	Unit
Breakdown Voltage	-17.57	-17.5	-17.4	V
Max Photon Detection Efficiency	No Data	No Data	33 (470nm, V_{EB}=1.2V)	%
Timing Resolution (17.8V)	103 (FWHM)	114 (FWHM)	146 (FWHM)	ps
Median DCR (17.8V, ≈295K)	0.8	5	132.5	Hz
After-pulsing at $1.2V_{EB}$	No Data	3.725	No Data	%
Active Area	3.14	12.56	50.24	μm^2
Dead Time	60	90	150	ns