

A 1080 HD Ready 1/2.33-type 12M Pixel CCD Image Sensor With Dual Channel Horizontal CCD

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Abstract

We have developed a 1/2.33-type 12M pixel CCD image sensor with dual channel horizontal CCD for a Digital Still Camera (DSC) that could take 1920(H) x 1080(V) a High Definition (HD) movie. We minimized the width of horizontal CCD (HCCD) by adopting the horizontal interlace output and horizontal four phases drive. And we applied the fixed color-to-channel assignment with symmetrical parallel HCCD to avoid inequality of performance between the two channels of HCCDs. As a result, this device could be realized to avoid the generation of the fixed pattern noise (FPN) and very high image quality for HD with a very low driving voltage of 2.0V in HCCD at 49.5MHz.

1. Introduction

In the DSC market, the movie shooting function is one of the most important options. 1080 HD movie already has been realized with CMOS sensor, but regarding CCD which has a high image quality and is suitable for miniaturization, 720 HD movie has been a boundary due to the practical limit of the pixels data rate. In order to realize 1080 HD movie with CCD, dual channel output CCD was developed. Figure 1 shows the structure in the conventional dual channel HCCD. The HCCD in the device is performed by a horizontal 2 phases drive, and the horizontal electrodes pitch is quite short, the same as a half of the pixel size. The width of HCCD is very large in order to increase the HCCD saturation signal. In the case of small-pixel sizes, it is especially needed.

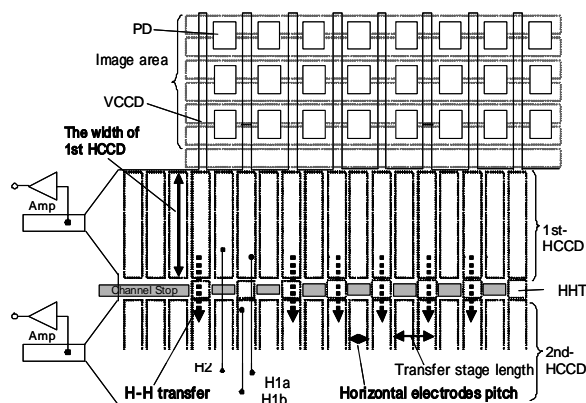


Figure 1. Structure in conventional dual channel HCCD.

Thus, the conventional dual channel CCD has two main problems. One is a necessity of high drive voltage to avoid the FPN due to poor

transfer efficiency from 1st-HCCD to 2nd-HCCD. Another is an inequality of performance between the two channels of HCCDs because of structural asymmetry. Consequently, conventional dual channel CCD has large power consumption and the degradation of the image quality. Those problems are due to the extremely large width of HCCD, therefore, we performed to minimize the width of HCCD by adopting the interlace output and 4 phases drive.

2. Device parameters

Table 1 shows the device parameters of the dual channel 1/2.33-type 12M pixel CCD image sensor. Total number of pixels is 4,108 (H) x 3,038 (V) = 12,480,104. Charge level signal mixing of 2(H) x 2(V) = 4 pixels enable to 1,920(H) x 1,080(V) = 2,073,600 pixels in full HD motion pictures mode with 30fps.

Table 1. Device parameters

Parameters	Values
Color-filters type	RGB
Optical format	1/2.33 type
Total number of pixels	4,108(H) x 3,038(V)=12,480,104
Number of effective pixels	4,016(H) x 3,020(V)=12,128,320
Unit pixels size (um x um)	1.540 (H) x 1.540 (V)
Actual imaging area dimensions (mm x mm)	6.160 (H) X 4.624 (V)
Image size (mm)	7.704
Package size (mm x mm)	9.4(H) x 8.3(V)
Frame rate in still mode (frames/s)	5.0
Frame rate in Full HD mode (frames/s)	30.0

3. Device structure

(1). Minimization of the width of HCCD

Figure 2 shows the structure in newly developed dual channel HCCD. There is a HCCD-to-HCCD transfer gate (HHT) between the two HCCD channels.

This structure is optimized for the motion pictures mode. In the full HD motion pictures mode, two signals of pixels in columns are mixed. For this purpose, HCCD transfer stages have a 1/2 of vertical CCD (VCCD) column density. Moreover, considering the dual channel structure, 1/4 of VCCD column density is suitable for each HCCD transfer stage density. That is to say, the dual channels 4:1 interlace HCCD structure is suitable for full HD motion pictures in this device.

Four VCCD columns are bundled at the last stage of VCCD, which is directly connected to 1st-HCCD. Horizontal 4:1 interlace output which means charge transfer from VCCD to HCCD in 4 times per single horizontal line, i.e. HCCD could have a transfer stage per 4 columns of VCCDs. One transfer stage length becomes 4 times longer, and HCCD width could be 1/4 shorter to conventional progressive output structure if keeping the HCCD saturation. And also, by 4 phases drive, which performs to accumulate charge with 2 gates, could ensure a large charge handling capability of HCCD in comparison with horizontal 2 phases drive. Consequently, we could reduce the width of HCCD to 15% of conventional, and could suppress the generation of FPN.

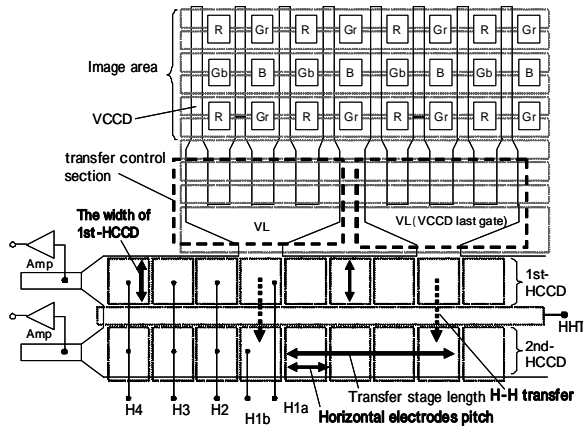


Figure 2. Structure in newly developed dual channel HCCD.

(2). Fixed color-to-channel assignment

In addition, we applied the fixed color-to-channel assignment. Figures 3 and 4 show the schematic diagram of VCCD-to-HCCD unit structure to describe the transfer sequence in still image mode and motion

pictures mode respectively. The unit is constructed with four VCCDs, a transfer control section, two HCCD transfer stages and HHT. In the case of still image mode, one signal charges are transferred from VCCD to 1st or 2nd HCCD without mixing by holding the other signal charges at the transfer control section. In the readout of R-Gr line, first, the left R signal is transferred to 2nd-HCCD transfer stage via 1st-HCCD, second, the left Gr signal is transferred to 1st-HCCD transfer stage. Then the signal charges in both HCCDs are transferred toward the amplifier at the same HD period. The rest R and Gr signals are readout at the next HD period.

In the case of motion pictures mode, the signal charges in the same color are mixed at the last stage of VCCD and transferred from VCCD to 2nd-HCCD via 1st-HCCD. During this period, the charges in the other color have been held at the transfer control section. Next, the charges in the other color which have been held are mixed and transferred in the same way to 1st-HCCD. After that, the charges in both HCCDs are transferred toward the amplifier at the same HD period. Thus, in the case of both modes, Gr and B are output from 1st-HCCD, R and Gb are from 2nd-HCCD.

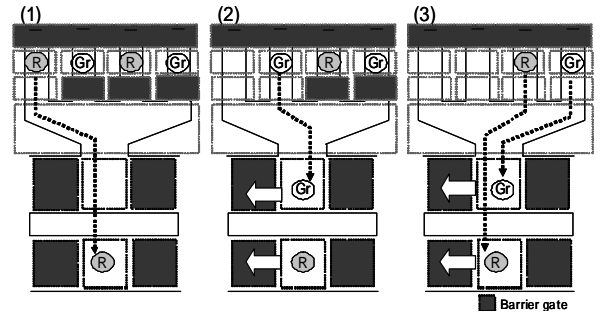


Figure 3. Schematic diagram of charge transfer sequence in still image mode.

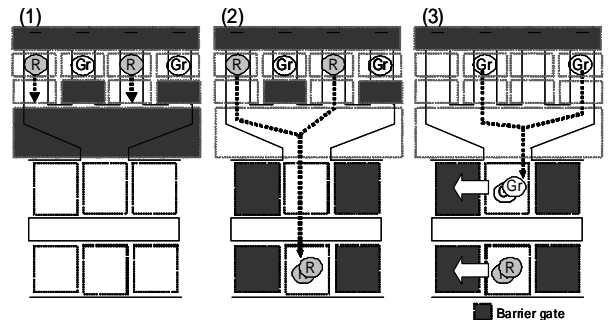


Figure 4. Schematic diagram of charge transfer sequence in motion pictures mode.

Figure 5 shows the schematic diagram of charge transfer sequence in HCCD while horizontal transfer period. Conventional single channel CCD has the mixed color-to-channel assignment, for example in R-Gr line, R and Gr signals are alternately transferred and output. The fixed color-to-channel assignment is free from mixture of different color signals due to the degradation of HCCD transfer efficiency. Therefore, horizontal color-shading is expected to be suppressed in spite of very low driving voltage, due to the charge transfer in the same color. Figure 6 shows the experimental results of horizontal color-shading rate at horizontal driving voltage. Thus the system is robust to the fluctuation in driving voltage. And also, fixed color-to-channel assignment enables to renormalize gain difference between channels by white balance procedure. For the Analogue Front End (AFE), it only processes correlative input signal level in sequence, advantage of Analog-to-Digital Converter (ADC) accuracy is also expected in this assignment.

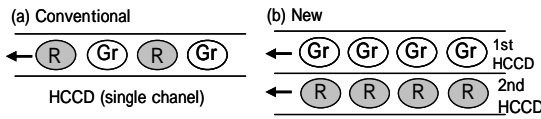


Figure 5. Schematic diagram of charge transfer sequence in HCCD while horizontal transfer period.

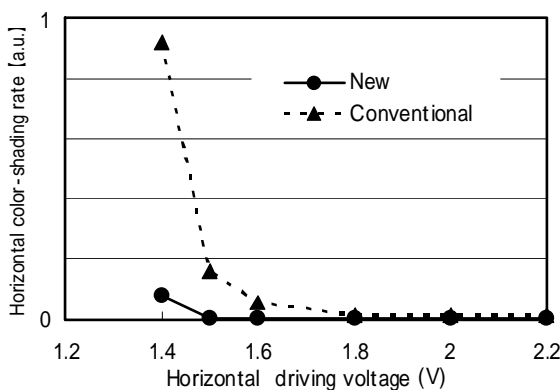


Figure 6. Experimental results of horizontal color-shading rate at horizontal driving voltage. (By horizontal 4 phases drive)

(3). Symmetrical structure of parallel HCCD

The new dual HCCD is formed by having the same width and potential of channel. Figure 7 shows the potential profile of HCCD in the case of vertical transfer from 1st-HCCD to

2nd-HCCD (H-H transfer). Figure 8 shows the schematic diagram of charge transfer sequence in HCCD in the case of both H-H transfer and horizontal transfer. In conventional structure, there are extreme potential slopes in 1st-HCCD to prevent the generation of FPN caused by transfer inefficiency in the case of H-H transfer, but those potential slopes are also formed in the case of horizontal transfer. This causes the degradation of the charge handling capability and transfer inefficiency of 1st-HCCD due to the meandering of the signal charges while horizontal transfer period. Therefore, there is the necessity of high driving voltage in HCCD to prevent those problems.

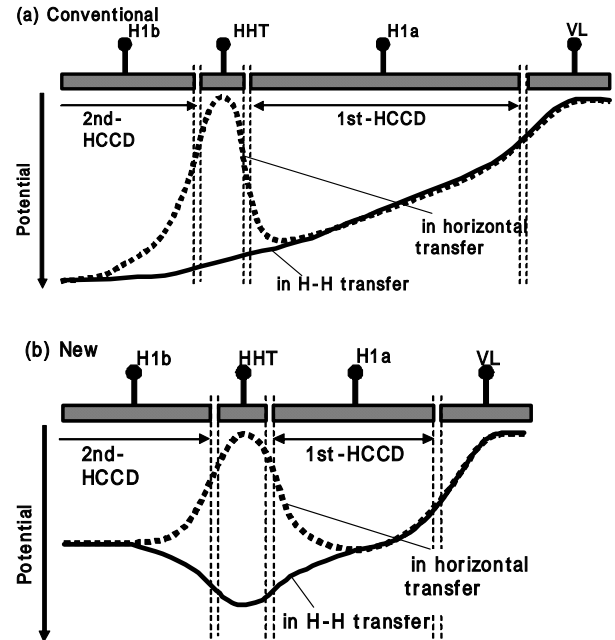


Figure 7. Potential profile of HCCD in the case of vertical transfer from 1st-HCCD to 2nd-HCCD (H-H transfer) and horizontal transfer. In H-H transfer, H1a/b and HHT are high voltage level. In horizontal transfer, HHT is low voltage level, H1a/b are high voltage level.

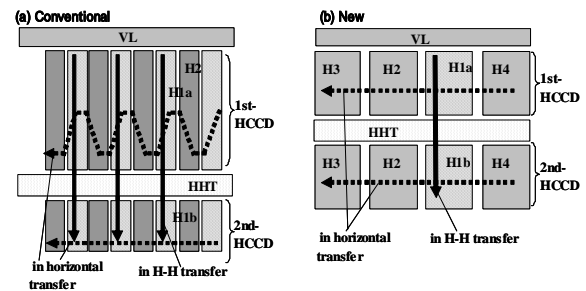


Figure 8. Schematic diagram of charge transfer sequence in HCCD in the case of both H-H transfer and horizontal transfer. New HCCD is suppressed the meandering of the signal charges while horizontal transfer period.

In the new structure, it is not needed to form additional potential slopes because of the very short H-H transfer distance by adopting the horizontal interlace output and horizontal four phases drive. By optimizing the potential under the HHT gate and using the HHT gate with relatively high voltage swing, compared with that in HCCD, is the same as that in VCCD. HHT potential and voltage swing could strengthen the transfer fields to completely eliminate FPN caused by the transfer inefficiency nearly HHT gate in 1st-HCCD during H-H transfer period. H-H transfer is completed by changing the voltage level of HHT gate from high to low, the barrier is formed between the two channels of HCCDs.

On the other hand, it could be formed equal potential in 1st-HCCD as the same 2nd-HCCD during horizontal transfer period. Despite a very low driving voltage, it enables sufficient and equal horizontal transfer efficiency between the two channels of HCCDs.

As a result, we realized to avoid the FPN by complete transfer efficiency from a HCCD to another HCCD compatible with sufficient horizontal transfer efficiency by symmetrical narrow dual channel HCCD. We have achieved a very low driving voltage of 2.0V and reduced power consumption in dual channel HCCD by 55% compared with conventional single channel HCCD. Triple or quad channel HCCD is possible by this system.

5. Device performance

We have developed a 1/2.33-type 12M pixel CCD image sensor with dual channel horizontal CCD that could take a Full HD movie. This device consists of a single-layer electrode structure by a poly-Si material, with three-layer metal wiring. [1] Moreover, this device is designed for high sensitivity and could be used for very high image quality in Full HD. Table 2 summarizes the characteristics of the device. Figure 9 shows the reproduced image of a resolution chart in Full HD motion pictures mode. Figure 10 shows the overview of this device.

6. Conclusion

In this paper, we described key technology to overcome conventional problems in dual channel horizontal CCD which are the necessity of high drive voltage to avoid the FPN and inequality of performance between two channels of HCCDs. Those advantages are especially suitable for DSC with Full HD movie and for CCD with small-pixel sizes. Our technologies are expandable to smaller pixel size or multi channel structure for further high resolution or high readout pixel rate.

Table 2. Device Characteristics

Parameters	Values
Pixels size (um x um)	1.54 x 1.54
HCCD driving frequency (MHz)	49.5
HCCD driving clock	4 phase
HCCD driving voltage (V)	2.0
Power consumption in Full HD mode (mW)	360
Sensitivity (mV)	240
/7.5fps, illuminance(at the CCD surface) :1.9 lux	
Saturation output (mV)	600
Smear 1/10V (dB)	-83

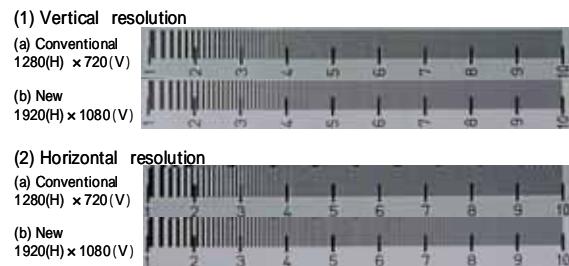


Figure 9. Reproduced image of the resolution chart in HD motion pictures mode.

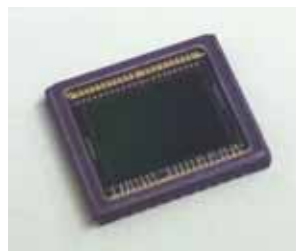


Figure 10. Overview of this device.

7. Acknowledgement

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8. References

- [1] S.Suzuki, et. al. "A 2/3-in. 2200k-pixel FIT-CCD for DTV 1080i", IEEE Workshop on CCDs and Advanced Image Sensors, Nagano, Japan(1999)