

Process Integration aspects of back illuminated CMOS Imagers using Smart StackingTM technology with best in class direct bonding

Ruth Shima Edelstein¹, Omer Katz¹, Becky Lavi¹, Ishai Aberman¹, Sagee Rosenthal¹, Michal Shadmi¹, Shay Arad¹, Nili Golan¹, Michal Shach Caplan¹, and Morad Massalha¹.

Chrystelle Lagahe-Blanchard², Laurent Marinier², Richard Fontanière², Arnaud Castex², Marcel Broekaaart², Muriel Martinez², Nathalie Milhet², Arnaud Rigny², Christine Pelissier²

- (1) TowerJazz, Ramat Gavriel Industrial Area, P.O. Box 619, Migdal Haemek, Israel 23105, Tel: +972-4-650-6611, Fax: 972-4-6547788, E-mail: ruthsh@towersemi.com
- (2) SOITEC, Parc technologique des Fontaines, Bernin 38926 Crolles Cedex, France Tel: +33 (0)4 76 92 96 31, Fax: +33 (0)4 76 92 94 31, Email: chrystelle.lagahe@soitec.fr

Over recent years, the concept of backside illuminated (BSI) sensors has become one of the leading solutions to optical challenges such as improved quantum efficiency, and angular dependence. It has been shown advantageous for small pixels [1-6] with limited number of transistors, but is becoming appealing also for high end sensors which require more transistors, fast routing, and large chief ray angles. A 5.4µm pixel for cinematography/DSLR with state of the art performance has been fully integrated (0.18 technology) using SOI wafers and Smart StackingTM technology to form a BSI sensor.

The choice of SOI substrates over bulk material is strongly driven by integration considerations. The buried oxide of the SOI acts as a built-in etch stop [1-4] as well as protection to the active Si layer during the thinning process, making the process less complex and more robust due to highly uniform thinning (fig 1). In addition, the buried layer can be tailored to have anti reflective (AR) properties for various applications (fig 2). In contrast to AR layers which are formed ex situ over back thinned bulk material, wherein the inherent across wafer thickness variation and Si roughness are relatively large, this method uniquely enables very high control over thickness uniformity, and minimizes post processing steps.

Another significant novel component of our integration is the ability to perform backside alignment of a color filter array, and contacts to pads with lithography tools which are commonly used for front side processing. This achievement is obtained by the formation of deep trenches at the initial steps of processing which land on the buried insulator (fig 3) and are visible from wafer backside (fig 4). These trenches can be customized to the desired Si thickness and therefore a variety of applications. The processed SOI wafer, with CMOS sensor circuitry is then bonded and thinned by the Smart StackingTM technology enabling the transfer of the processed layer onto a handle silicon wafer [7,8].

Direct bonding of two wafers requires stringent control of surface properties: micro-roughness, flatness, contamination and surface chemistry in order to achieve high quality bonding in terms of defectiveness, edge exclusion, strength and reliability. Figure 5 compares bonded structures resulting from non optimized and optimized process integration, including adaptation and tuning of alignment marks design (which impose large topography) and fabrication, surface planarization and pre-bonding surface preparation. A defect free bonding interface is achieved with a regular <1.5mm peripheral non bonded width [9,10]. To address thermal budget constraints (i.e.<400°C), specific pre-bonding surface conditioning (CMP, plasma activation,...), and post-bonding thermal treatment were developed to control and increase the bonding strengths. High bonding energies compatible with subsequent processes (thinning, etching, metal deposition, dicing...) were achieved (fig 6), as well as minimized stress. Reducing process-induced distortion is key to avoid impairing devices performance, yield and reliability.

To conclude, we successfully produced a back thinned cinematography/DSLR CMOS image sensor, overcoming integration challenges related to backside processing such as incorporation of a buried AR layer, and backside alignment, by use of SOI substrates and Smart Stacking™ technology with best in class direct bonding.

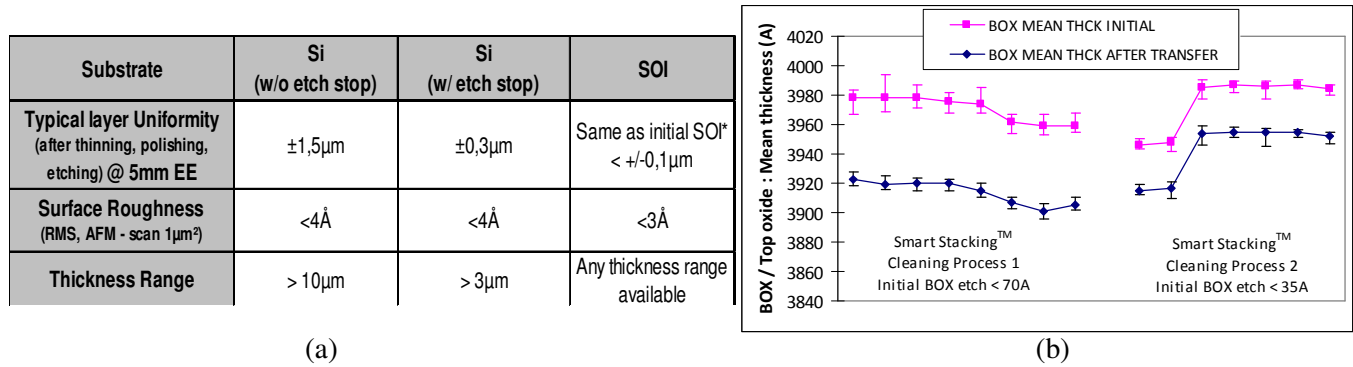


Fig 1: a) Silicon thickness and uniformity performance after layer transfer, depending on initial substrate choice; b) BOX thickness and uniformity after layer transfer based on circuits built on SOI substrates.

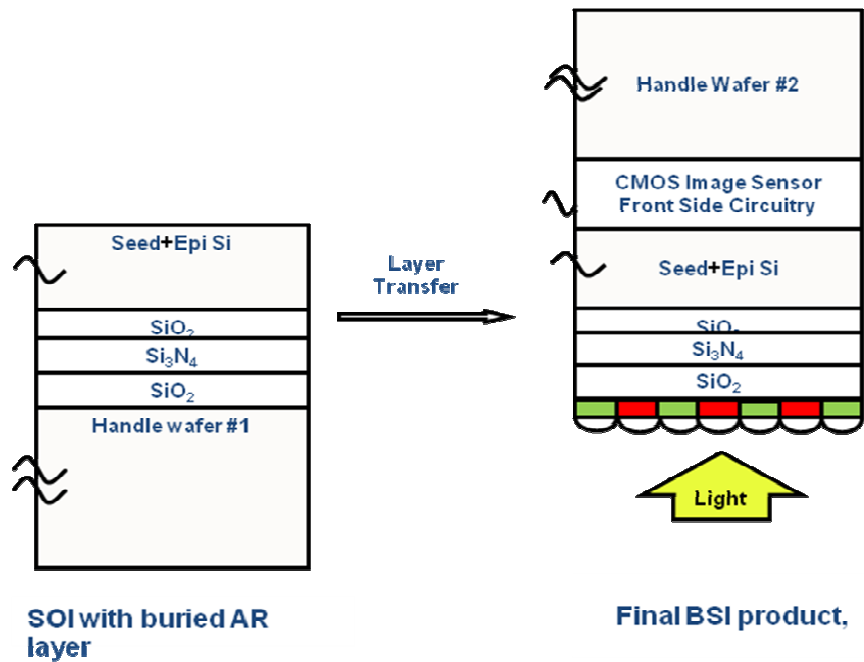


Fig 2: Using SOI wafers with buried AR layer to form a BSI sensor.

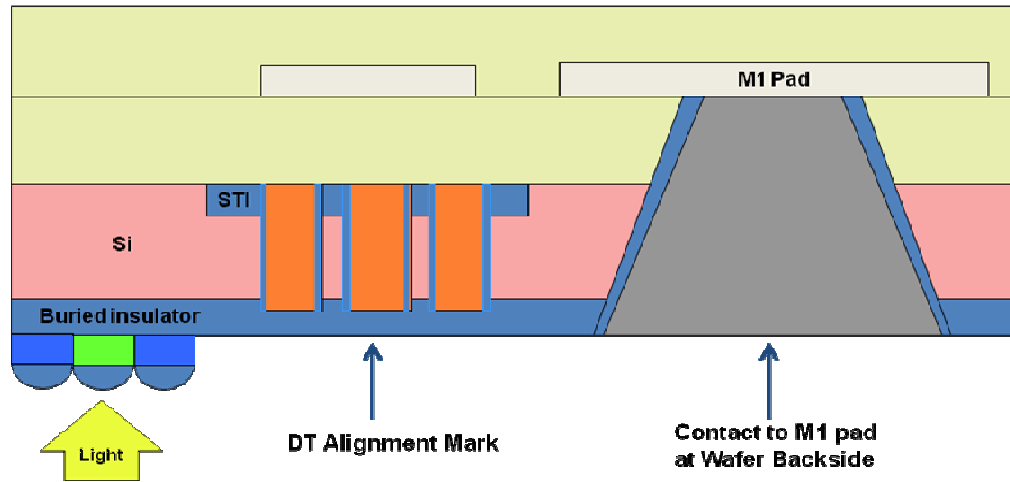


Fig 3: Schematic of integration showing deep trench alignment marks reaching wafer backside.

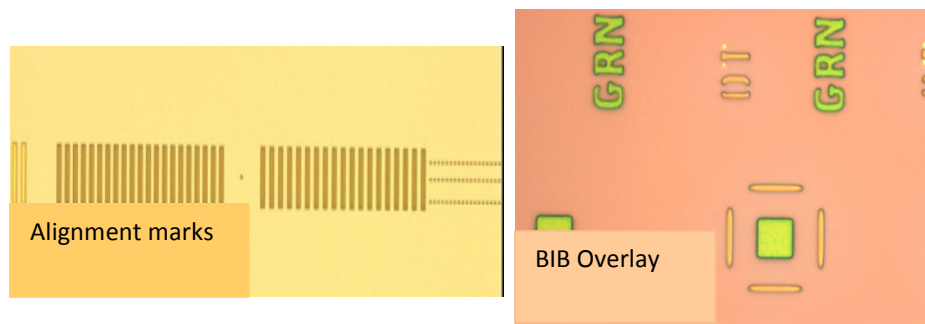


Fig 4: Alignment marks and overlay measurement structures visible at wafer backside by optical microscope.

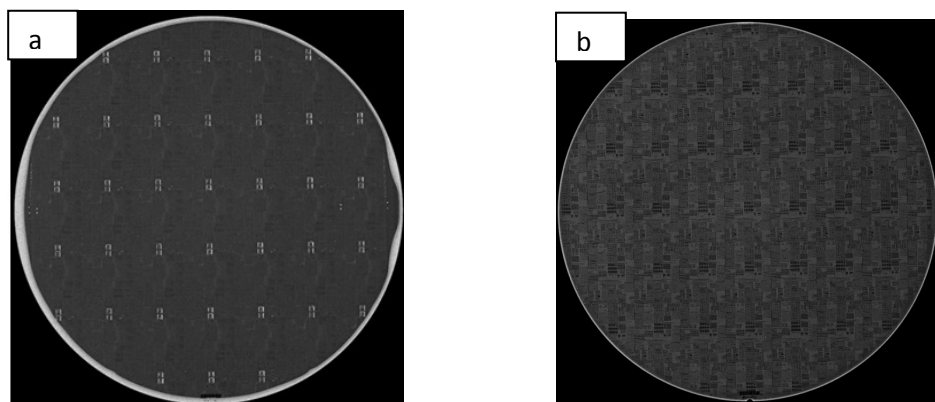


Fig 5: a) Non optimized alignment marks design and planarization process, leading to residual local bonding defects on alignment marks and irregular peripheral non bonded width; b) Optimized process integration.

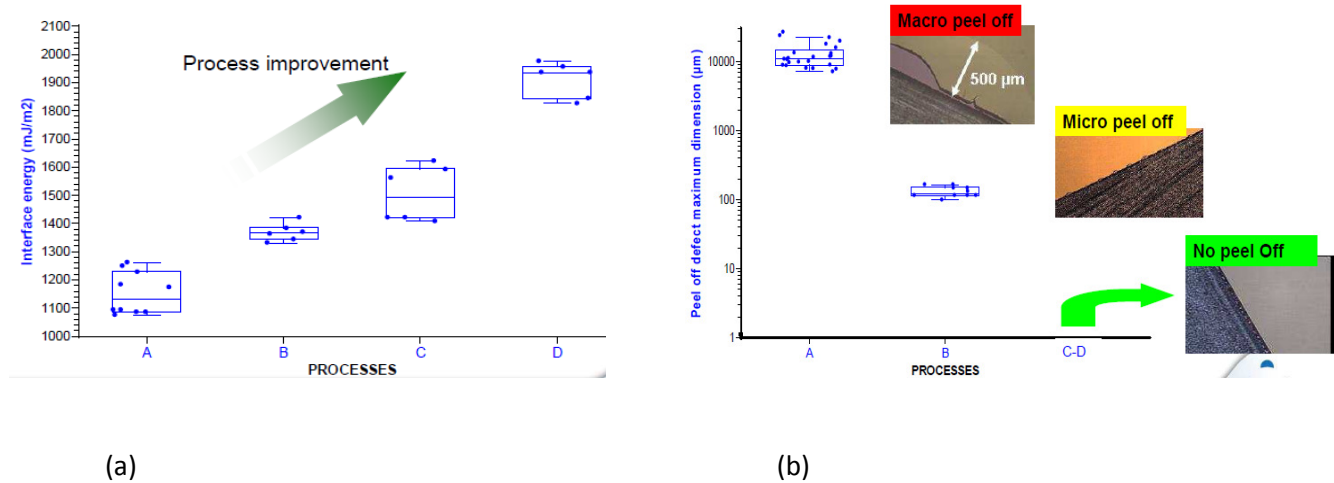


Fig 6: Best in class direct bonding: a) Various bonding processes and associated interface energies; b) Transferred layer edge quality versus bonding processes [9].

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